CMOS Digital Integrated Circuits Silicon Monolithic

# 74VHCT574AFT

## 1. Functional Description

- Octal D-Type Flip Flop with 3-State Outputs

## 2. General

The 74VHCT574AFT is an advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This 8-bit D-type flip-flop is controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The input voltage is compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, hot board insertion, etc.

Note: Output in off-state

## 3. Features

(1) AEC-Q100 (Rev. H) (Note 1)

(2) Wide operating temperature range: $T_{opr}$ = -40 to 125 °C

(3) High speed: $f_{MAX}$ = 140MHz (typ.) at $V_{CC}$ = 5.0 V

(4) Low power dissipation: $I_{CC}$ = 4.0 μA (max) at $T_a$ = 25°C

(5) Compatible with TTL inputs: $V_{IL}$ = 0.8V (max)
$V_{IH}$ = 2.0V (min)

(6) Power-down protection is provided on all inputs and outputs.

(7) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$

(8) Low noise: $V_{OLP}$ = 1.5 V (max)

(9) Pin and function compatible with the 74 series (74ACT/HCT/AHCT etc.) 574 type.

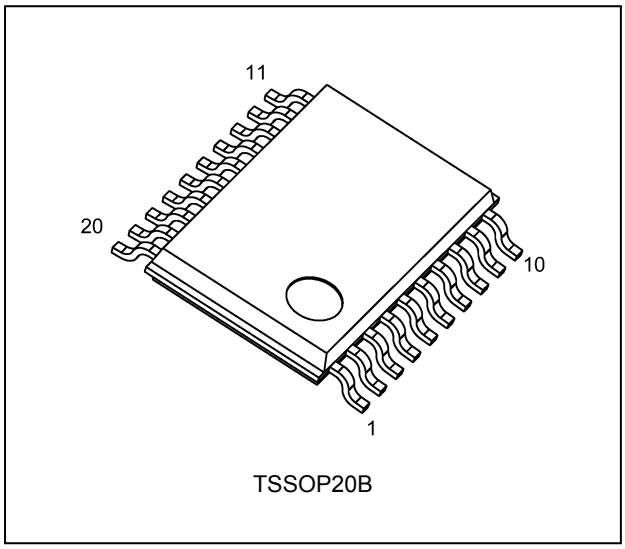
Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

Start of commercial production
2013-04



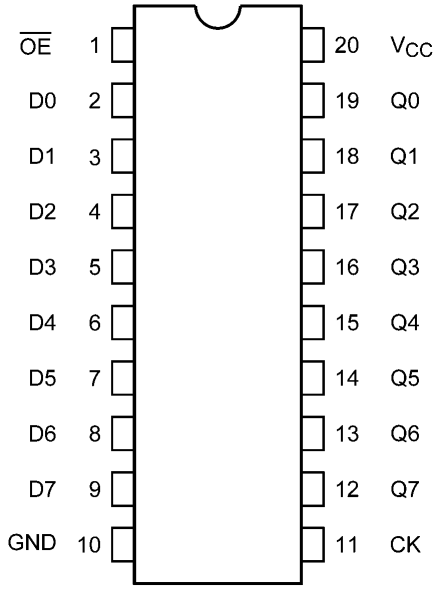
2016-08-04
Rev.3.0

## 4. Packaging



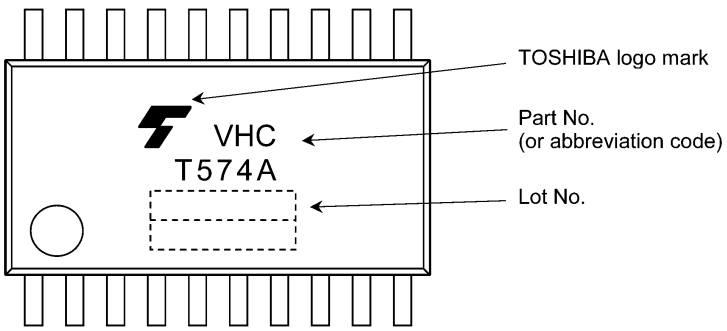

TSSOP20B

## 5. Pin Assignment

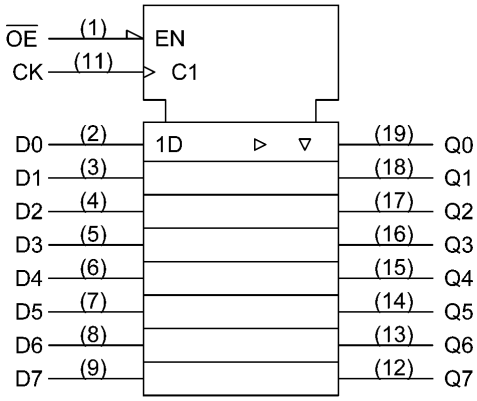



(top view)

## 6. Marking



## 7. IEC Logic Symbol

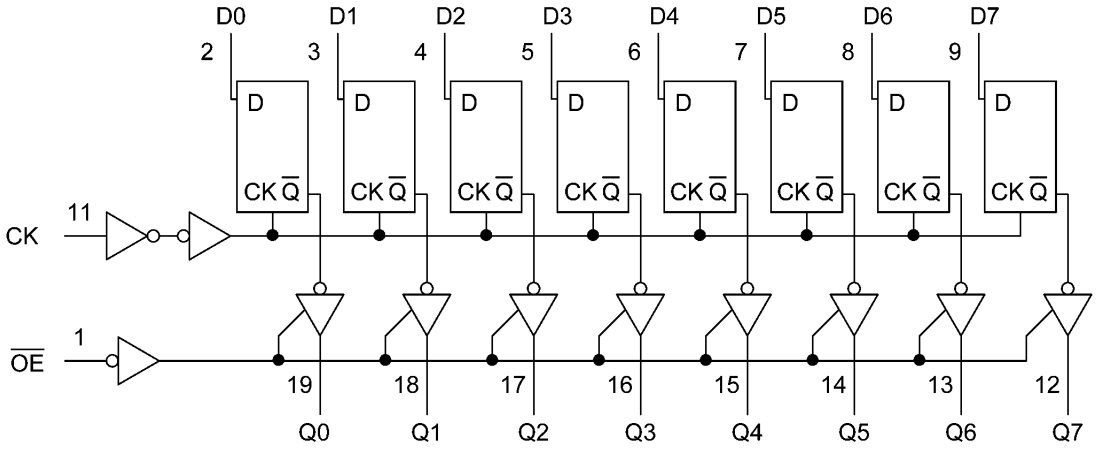



## 8. Truth Table

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OE}$ | CK | D | |
| H | X | X | Z |
| L | ↓ | X | Qn |
| L | ↑ | L | L |
| L | ↑ | H | H |

X: Don't care
Z: High impedance
Qn: No change

## 9. System Diagram



## 10. Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Note | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | -0.5 to 7.0 | V |
| Input voltage | $V_{IN}$ | | -0.5 to 7.0 | V |
| Output voltage | $V_{OUT}$ | (Note 1) | -0.5 to 7.0 | V |
| | | (Note 2) | -0.5 to $V_{CC}$ + 0.5 | |
| Input diode current | $I_{IK}$ | | -20 | mA |
| Output diode current | $I_{OK}$ | (Note 3) | ±20 | mA |
| Output current | $I_{OUT}$ | | ±25 | mA |
| $V_{CC}$/ground current | $I_{CC}$ | | ±75 | mA |
| Power dissipation | $P_D$ | (Note 4) | 180 | mW |
| Storage temperature | $T_{stg}$ | | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in off-state.

Note 2: High (H) or Low (L) state. $I_{OUT}$ absolute maximum rating must be observed.

Note 3: $V_{OUT}$ < GND, $V_{OUT}$ > $V_{CC}$

Note 4: 180 mW in the range of $T_a$ = -40 to 85 °C. From $T_a$ = 85 to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

## 11. Operating Ranges (Note)

| Characteristics | Symbol | Note | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 4.5 to 5.5 | V |
| Input voltage | $V_{IN}$ | | 0 to 5.5 | V |
| Output voltage | $V_{OUT}$ | (Note 1) | 0 to 5.5 | V |
| | | (Note 2) | 0 to $V_{CC}$ | |
| Operating temperature | $T_{opr}$ | | -40 to 125 | °C |
| Input rise and fall times | dt/dv | | 0 to 20 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either $V_{CC}$ or GND.

Note 1: Output in Off-state.

Note 2: High (H) or Low (L) state.

## 12. Electrical Characteristics

### 12.1. DC Characteristics (Unless otherwise specified, $T_a$ = 25 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 4.5 to 5.5 | 2.0 | — | — | V |
| Low-level input voltage | $V_{IL}$ | — | | 4.5 to 5.5 | — | — | 0.8 | V |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50 μA | 4.5 | 4.40 | 4.50 | — | V |
| | | | $I_{OH}$ = -8 mA | 4.5 | 3.94 | — | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 | — | 0.0 | 0.10 | V |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | — | 0.36 | |
| 3-state output OFF-state leakage current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | — | ±0.25 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | — | ±0.1 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 4.0 | μA |
| | $I_{CCT}$ | Per input: $V_{IN}$ = 3.4 V<br>Other input: $V_{CC}$ or GND | | 5.5 | — | — | 1.35 | mA |
| Output leakage current (Power-OFF) | $I_{OPD}$ | $V_{OUT}$ = 5.5 V | | 0 | — | — | 0.5 | μA |

### 12.2. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 4.5 to 5.5 | 2.0 | — | V |
| Low-level input voltage | $V_{IL}$ | — | | 4.5 to 5.5 | — | 0.8 | V |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50 μA | 4.5 | 4.40 | — | V |
| | | | $I_{OH}$ = -8 mA | 4.5 | 3.80 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 | — | 0.10 | V |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | 0.44 | |
| 3-state output OFF-state leakage current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | ±2.50 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | 40.0 | μA |
| | $I_{CCT}$ | Per input: $V_{IN}$ = 3.4 V<br>Other input: $V_{CC}$ or GND | | 5.5 | — | 1.50 | mA |
| Output leakage current (Power-OFF) | $I_{OPD}$ | $V_{OUT}$ = 5.5 V | | 0 | — | 5.0 | μA |

### 12.3. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 125 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 4.5 to 5.5 | 2.0 | — | V |
| Low-level input voltage | $V_{IL}$ | — | | 4.5 to 5.5 | — | 0.8 | V |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -50 μA | 4.5 | 4.40 | — | V |
| | | | $I_{OH}$ = -8 mA | 4.5 | 3.70 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 4.5 | — | 0.10 | V |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | 0.55 | |
| 3-state output OFF-state leakage current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{OUT}$ = $V_{CC}$ or GND | | 5.5 | — | ±10.0 | μA |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | ±2.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | 80.0 | μA |
| | $I_{CCT}$ | Per input: $V_{IN}$ = 3.4 V<br>Other input: $V_{CC}$ or GND | | 5.5 | — | 1.50 | mA |
| Output leakage current (Power-OFF) | $I_{OPD}$ | $V_{OUT}$ = 5.5 V | | 0 | — | 20.0 | μA |

### 12.4. Timing Requirements (Unless otherwise specified, $T_a$ = 25°C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | $V_{CC}$ (V) | Typ. | Limit | Unit |
|---|---|---|---|---|---|
| Minimum pulse width (CK) | $t_{w(L)}$,$t_{w(H)}$ | 5.0 ± 0.5 | — | 6.5 | ns |
| Minimum setup time | $t_s$ | 5.0 ± 0.5 | — | 2.5 | ns |
| Minimum hold time | $t_h$ | 5.0 ± 0.5 | — | 2.5 | ns |

### 12.5. Timing Requirements (Unless otherwise specified, $T_a$ = -40 to 85°C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | $V_{CC}$ (V) | Limit | Unit |
|---|---|---|---|---|
| Minimum pulse width (CK) | $t_{w(L)}$,$t_{w(H)}$ | 5.0 ± 0.5 | 8.5 | ns |
| Minimum setup time | $t_s$ | 5.0 ± 0.5 | 2.5 | ns |
| Minimum hold time | $t_h$ | 5.0 ± 0.5 | 2.5 | ns |

### 12.6. Timing Requirements (Unless otherwise specified, $T_a$ = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | $V_{CC}$ (V) | Limit | Unit |
|---|---|---|---|---|
| Minimum pulse width (CK) | $t_{w(L)}$,$t_{w(H)}$ | 5.0 ± 0.5 | 8.5 | ns |
| Minimum setup time | $t_s$ | 5.0 ± 0.5 | 3.0 | ns |
| Minimum hold time | $t_h$ | 5.0 ± 0.5 | 2.5 | ns |

### 12.7. AC Characteristics (Unless otherwise specified, $T_a$ = 25 °C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | $C_L$ (pF) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Propagation delay time (CK-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 5.0 ± 0.5 | 15 | — | 4.1 | 9.4 | ns |
| | | | | | 50 | — | 5.6 | 10.4 | |
| 3-state output enable time | $t_{PZL}$,$t_{PZH}$ | | $R_L$ = 1 kΩ | 5.0 ± 0.5 | 15 | — | 6.5 | 10.2 | ns |
| | | | | | 50 | — | 7.3 | 11.2 | |
| 3-state output disable time | $t_{PLZ}$,$t_{PHZ}$ | | $R_L$ = 1 kΩ | 5.0 ± 0.5 | 50 | — | 7.0 | 11.2 | ns |
| Maximum clock frequency | $f_{MAX}$ | | — | 5.0 ± 0.5 | 15 | 90 | 140 | — | MHz |
| | | | | | 50 | 85 | 130 | — | |
| Output skew | $t_{osLH}$,$t_{osHL}$ | (Note 1) | — | 5.0 ± 0.5 | 50 | — | — | 1.0 | ns |
| Input capacitance | $C_{IN}$ | | — | | | — | 4 | 10 | pF |
| Output capacitance | $C_{OUT}$ | | — | | | — | 9 | — | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note 2) | — | | | — | 25 | — | pF |

Note 1: Parameter guaranteed by design. ($t_{osLH}$ = $|t_{PLH}m - t_{PLH}n|$, $t_{osHL}$ = $|t_{PHL}m - t_{PHL}n|$)

Note 2: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per F/F)

And the total $C_{PD}$ when n pcs of F/F operate can be gained by the following equation.

$C_{PD}$ (total) = 14 + 11 × n

## 12.8. AC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | $C_L$ (pF) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time (CK-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 5.0 ± 0.5 | 15 | 1.0 | 10.5 | ns |
| | | | | | 50 | 1.0 | 11.5 | |
| 3-state output enable time | $t_{PZL}$,$t_{PZH}$ | | $R_L$ = 1 kΩ | 5.0 ± 0.5 | 15 | 1.0 | 11.5 | ns |
| | | | | | 50 | 1.0 | 12.5 | |
| 3-state output disable time | $t_{PLZ}$,$t_{PHZ}$ | | $R_L$ = 1 kΩ | 5.0 ± 0.5 | 50 | 1.0 | 12.0 | ns |
| Maximum clock frequency | $f_{MAX}$ | | — | 5.0 ± 0.5 | 15 | 80 | — | MHz |
| | | | | | 50 | 75 | — | |
| Output skew | $t_{osLH}$,$t_{osHL}$ | (Note 1) | — | 5.0 ± 0.5 | 50 | — | 1.0 | ns |
| Input capacitance | $C_{IN}$ | | — | | | — | 10 | pF |

Note 1: Parameter guaranteed by design. ($t_{osLH}$ = $|t_{PLH}m-t_{PLH}n|$, $t_{osHL}$ = $|t_{PHL}m-t_{PHL}n|$)

## 12.9. AC Characteristics (Unless otherwise specified, $T_a$ = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | $C_L$ (pF) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Propagation delay time (CK-Q) | $t_{PLH}$,$t_{PHL}$ | | — | 5.0 ± 0.5 | 15 | 1.0 | 12.0 | ns |
| | | | | | 50 | 1.0 | 13.0 | |
| 3-state output enable time | $t_{PZL}$,$t_{PZH}$ | | $R_L$ = 1 kΩ | 5.0 ± 0.5 | 15 | 1.0 | 13.0 | ns |
| | | | | | 50 | 1.0 | 14.0 | |
| 3-state output disable time | $t_{PLZ}$,$t_{PHZ}$ | | $R_L$ = 1 kΩ | 5.0 ± 0.5 | 50 | 1.0 | 14.0 | ns |
| Maximum clock frequency | $f_{MAX}$ | | — | 5.0 ± 0.5 | 15 | 70 | — | MHz |
| | | | | 5.0 ± 0.5 | 50 | 65 | — | |
| Output skew | $t_{osLH}$,$t_{osHL}$ | (Note 1) | — | 5.0 ± 0.5 | 50 | — | 1.0 | ns |
| Input capacitance | $C_{IN}$ | | — | | | — | 10 | pF |

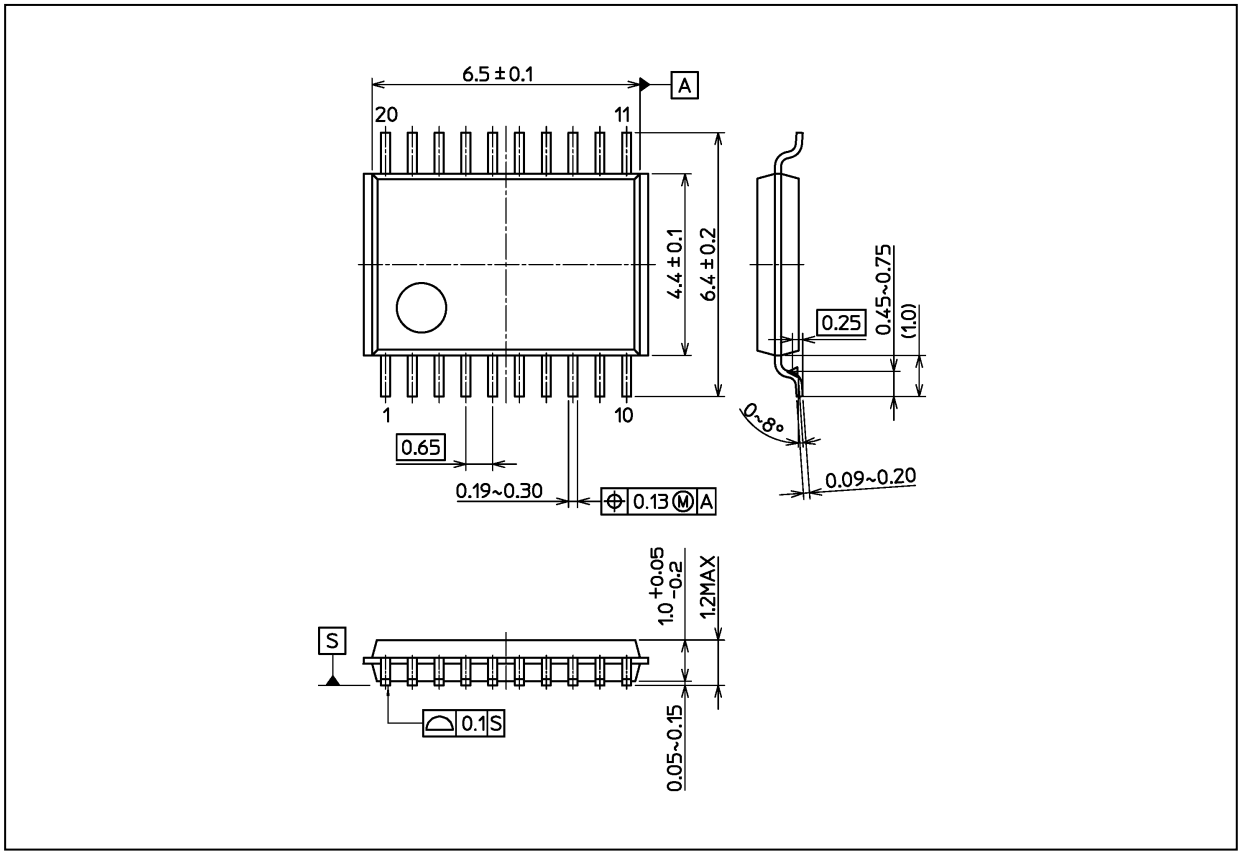
Note 1: Parameter guaranteed by design. ($t_{osLH}$ = $|t_{PLH}m-t_{PLH}n|$, $t_{osHL}$ = $|t_{PHL}m-t_{PHL}n|$)

## 12.10. Noise Characteristics (Unless otherwise specified, $T_a$ = 25°C, Input: $t_r = t_f$ = 3 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Typ. | Limit | Unit |
|---|---|---|---|---|---|---|
| Quiet output maximum dynamic $V_{OL}$ | $V_{OLP}$ | $C_L$ = 50 pF | 5.0 | 1.1 | 1.5 | V |
| Quiet output minimum dynamic $V_{OL}$ | $V_{OLV}$ | $C_L$ = 50 pF | 5.0 | -1.1 | -1.5 | V |
| Minimum high-level dynamic input voltage | $V_{IHD}$ | $C_L$ = 50 pF | 5.0 | — | 2.0 | V |
| Maximum low-level dynamic input voltage | $V_{ILD}$ | $C_L$ = 50 pF | 5.0 | — | 0.8 | V |

## Package Dimensions

Unit: mm




Weight: 0.071 g (typ.)

| Package Name(s) |
| --- |
| Nickname: TSSOP20B |

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