

TLP7820

1. Applications

- Motor phase and rail current sensing
- Power inverter current and voltage sensing

2. General

The TLP7820 of isolation amplifiers is designed for current sensing in electronic motor drives. In a typical implementation, motor currents flow through an external resistor and the resulting analog voltage drop is sensed by the TLP7820.

3. Features

- (1) Gain accuracy: $\pm 0.5\%$ (Gain rank B)
- (2) Gain drift: $0.00012\text{ V/V/}^\circ\text{C}$ (typ.)
- (3) Nonlinearity ($V_{IN} = \pm 200\text{ mV}$): 0.02% (typ.)
- (4) Input offset voltage: 0.9 mV (typ.)
- (5) V_{OUT} bandwidth (-3 dB): 230 kHz (typ.)
- (6) Operating temperature range: -40 to $105\text{ }^\circ\text{C}$
- (7) Common-mode transient immunity: $15\text{ kV}/\mu\text{s}$ (min)
- (8) Safety standards

UL-recognized: UL 1577, File No.E67349

cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349

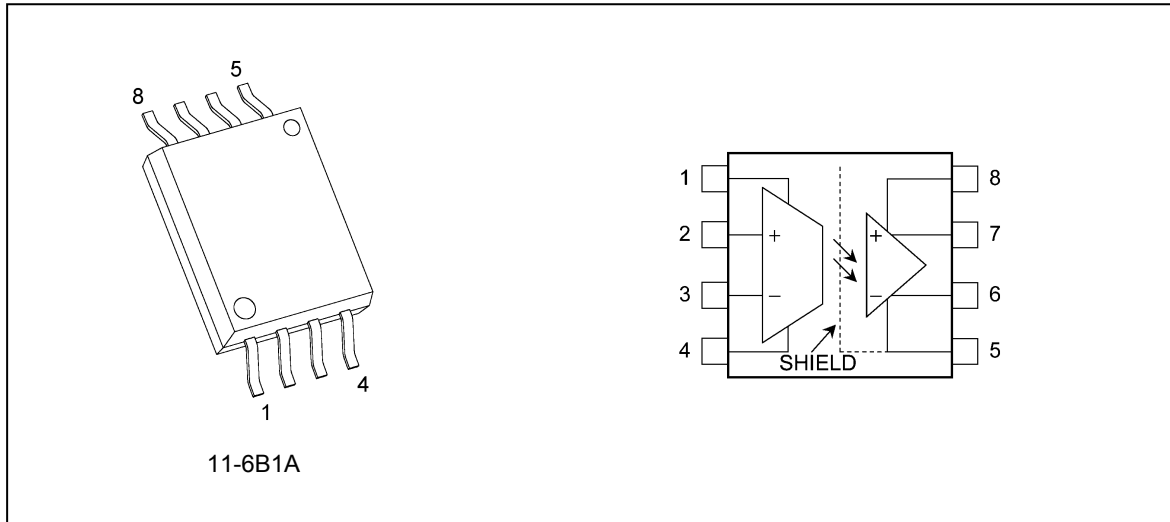
VDE-approved: EN 60747-5-5, EN 62368-1 (**Note 1**)

CQC-approved: GB4943.1, GB8898 Japan Factory

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

Start of commercial production
2015-09

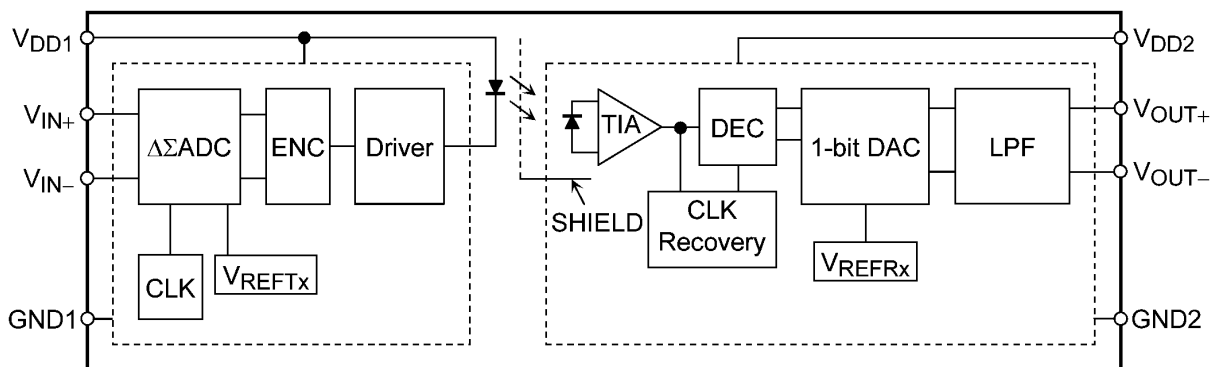
4. Packaging and Pin Assignment



4.1. Pin Assignment

| Pin No. | Symbol | Description |
|---------|------------|----------------------------|
| 1 | V_{DD1} | Input side supply voltage |
| 2 | V_{IN+} | Positive input |
| 3 | V_{IN-} | Negative input |
| 4 | GND1 | Input side ground |
| 5 | GND2 | Output side ground |
| 6 | V_{OUT-} | Negative output |
| 7 | V_{OUT+} | Positive output |
| 8 | V_{DD2} | Output side supply voltage |

5. Internal Circuit (Note)



Note: A 0.1- μ F bypass capacitor must be connected between 1 and 4 pins and between 5 and 8 pins.

6. Principle of Operation

6.1. Mechanical Parameters

| Characteristics | Size | Unit |
|------------------------------|-----------|------|
| Height | 2.3 (max) | mm |
| Creepage distances | 8.0 (min) | |
| Clearance | 8.0 (min) | |
| Internal isolation thickness | 0.4 (min) | |

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ °C}$)

| Characteristics | Symbol | Note | Rating | Unit |
|--|-------------------------|----------|-------------------------|-------|
| Supply voltages | V_{DD1}, V_{DD2} | | -0.5 to 6 | V |
| Steady-state input voltages | V_{IN+}, V_{IN-} | | -0.5 to $V_{DD1} + 0.5$ | V |
| Two-second transient input voltages | V_{IN+}, V_{IN-} | | -6 to $V_{DD1} + 0.5$ | V |
| Input power dissipation | P_D | | 72 | mW |
| Input power dissipation derating ($T_a \geq 110.6\text{ °C}$) | $\Delta P_D/\Delta T_a$ | | -5.0 | mW/°C |
| Output voltages | V_{OUT+}, V_{OUT-} | | -0.5 to $V_{DD2} + 0.5$ | V |
| Output power dissipation | P_O | | 60 | mW |
| Output power dissipation derating ($T_a \geq 113.0\text{ °C}$) | $\Delta P_O/\Delta T_a$ | | -5.0 | mW/°C |
| Operating temperature | T_{opr} | | -40 to 105 | °C |
| Storage temperature | T_{stg} | | -55 to 125 | °C |
| Lead soldering temperature (10 s) | T_{sol} | (Note 1) | 260 | °C |
| Isolation voltage (AC, 60 s, R.H. $\leq 60\%$) | BV_S | (Note 2) | 5000 | Vrms |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note: Ceramic capacitors (0.1 μF) should be connected between 1 and 4 pins and between 5 and 8 pins to stabilize the operation. Otherwise, this photocoupler may not switch properly. The bypass capacitors should be placed as close as possible to each pin.

Note 1: $\geq 2\text{ mm}$ below seating plane.

Note 2: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

8. Recommended Operating Conditions (Note)

| Characteristics | Symbol | Note | Min | Typ. | Max | Unit |
|----------------------------|--------------------|--------------------|------|------|-----|------|
| Input side supply voltage | V_{DD1} | | 4.5 | 5 | 5.5 | V |
| Output side supply voltage | V_{DD2} | | 3 | — | 5.5 | |
| Analog input voltage | V_{IN+}, V_{IN-} | (Note 1), (Note 2) | -200 | — | 200 | mV |
| Ambient temperature | T_a | | -40 | — | 105 | °C |

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this data sheet should also be considered.

Note 1: Full-Scale Differential Voltage Input Range(FSR) = $\pm 300\text{ mV}$ (typ.)

Note 2: When either V_{IN+} or V_{IN-} or both are equal to or greater than $V_{DD1} - 2\text{ V}$ (e.g., if $V_{DD1} = 5\text{ V}$, when V_{IN+} and/or V_{IN-} are equal to or greater than $5\text{ V} - 2\text{ V} = 3\text{ V}$), isolation amplifiers go into one of the test modes. Do not raise either V_{IN+} or V_{IN-} above this voltage to keep the device in functional mode.

9. Electrical Characteristics

9.1. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $105\text{ }^\circ\text{C}$, $V_{DD1} = 4.5$ to 5.5 V , $V_{DD2} = 3$ to 5.5 V , $V_{IN+} = -200$ to 200 mV , $V_{IN-} = 0\text{ V}$)

| Characteristics | Symbol | Note | Test Condition | Min | Typ. | Max | Unit |
|--|----------------------|----------|---|------|---------|------|------------------------------------|
| Input offset voltage | V_{OS} | | $T_a = 25\text{ }^\circ\text{C}$ | -0.6 | 0.9 | 2.4 | mV |
| Input offset voltage drift vs ambient temperature | $ dV_{OS}/dT_a $ | | | — | 2 | 6 | $\mu\text{V}/^\circ\text{C}$ |
| Input offset voltage drift vs input side supply voltage | $ dV_{OS}/dV_{DD1} $ | | | — | 120 | — | $\mu\text{V}/\text{V}$ |
| Gain (Rank B) | G_0 | (Note 1) | $T_a = 25\text{ }^\circ\text{C}$ | 8.16 | 8.2 | 8.24 | V/V |
| Gain (Rank A) | G_1 | (Note 1) | $T_a = 25\text{ }^\circ\text{C}$ | 8.12 | 8.2 | 8.28 | |
| Gain (None) | G_3 | (Note 1) | $T_a = 25\text{ }^\circ\text{C}$ | 7.95 | 8.2 | 8.44 | |
| Gain drift vs ambient temperature | $ dG/dT_a $ | | | — | 0.00012 | — | $\text{V}/\text{V}/^\circ\text{C}$ |
| V_{OUT} non-linearity ($\pm 200\text{ mV}$) | NL ₂₀₀ | (Note 2) | $V_{IN+} = -200$ to 200 mV , $T_a = 25\text{ }^\circ\text{C}$ | — | 0.02 | 0.13 | % |
| V_{OUT} non-linearity ($\pm 200\text{ mV}$) drift vs ambient temperature | $ dNL_{200}/dT_a $ | | | — | 0.00007 | — | $\%/^\circ\text{C}$ |
| V_{OUT} non-linearity ($\pm 100\text{ mV}$) | NL ₁₀₀ | (Note 2) | $V_{IN+} = -100$ to 100 mV , $T_a = 25\text{ }^\circ\text{C}$ | — | 0.015 | 0.06 | % |
| High-level output voltage | V_{OH} | | $V_{IN+} = 400\text{ mV}$, $T_a = 25\text{ }^\circ\text{C}$ | — | 2.497 | — | V |
| Low-level output voltage | V_{OL} | | $V_{IN+} = -400\text{ mV}$, $T_a = 25\text{ }^\circ\text{C}$ | — | 0.0009 | — | V |
| Input common-mode rejection ratio | CMRR _{IN} | | | — | 80 | — | dB |
| Equivalent input resistance | R_{IN} | | | — | 80 | — | k Ω |
| Input bias current | I_{IN+} | | $V_{IN+} = 0\text{ V}$, $T_a = 25\text{ }^\circ\text{C}$ | -1 | -0.055 | — | μA |
| Input side supply current (V_{DD1}) | I_{DD1} | | $V_{IN+} = 0\text{ V}$ | — | 8.6 | 12 | mA |
| Output side supply current (V_{DD2}) | I_{DD2} | | $V_{IN+} = 0\text{ V}$ | — | 6.2 | 10 | mA |
| V_{OUT} output resistance | R_{OUT} | | V_{OUT+} or V_{OUT-} | — | 21 | — | Ω |

Note 1: See section 9.1.1. for gain rank values.

Note 2: The slope of the optimum line is derived by the method of least squares between differential input voltage ($V_{IN+} - V_{IN-}$) and differential output voltage ($V_{OUT+} - V_{OUT-}$). Nonlinearity is defined as a fraction of the half of the peak-to-peak value of differential output voltage deviation divided by the full-scale differential output voltage (OVR).

9.1.1. Gain Rank (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

| Rank | Gain Rank Marking | Gain | | | Unit |
|------------------------|-------------------|-------|--------|-------|------|
| | | (Min) | (Typ.) | (Max) | |
| None ($\pm 3\%$) | Blank, A, B | 7.95 | 8.2 | 8.44 | V/V |
| Rank A ($\pm 1\%$) | A, B | 8.12 | 8.2 | 8.28 | |
| Rank B ($\pm 0.5\%$) | B | 8.16 | 8.2 | 8.24 | |

Note: The gain is defined as the slope of the optimum line derived by the method of least squares between differential input voltage ($V_{IN+} - V_{IN-}$) and differential output voltage ($V_{OUT+} - V_{OUT-}$) in the recommended voltage range.

Note: Specify both the part number and a rank in this format when ordering.

Example: Rank B: TLP7820(B)

10. AC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 105 °C, $V_{DD1} = 4.5$ to 5.5 V, $V_{DD2} = 3$ to 5.5 V)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--|------------|--|-----|------|-----|-------------|
| V_{OUT} bandwidth (-3 dB) | f_{-3dB} | $V_{IN+} = 400$ mV _{p-p} , sine wave | 140 | 230 | — | kHz |
| V_{IN} to V_{OUT} propagation delay time (10 %-10 %) | t_{pD10} | $V_{IN+} = 0$ to 200 mV/ μ s step $C_L = 15$ pF | — | 1.9 | 2.3 | μ s |
| V_{IN} to V_{OUT} propagation delay time (50 %-50 %) | t_{pD50} | | — | 2.3 | 2.6 | |
| V_{IN} to V_{OUT} propagation delay time (90 %-90 %) | t_{pD90} | | — | 2.8 | 3.3 | |
| V_{OUT} rise time | t_r | | — | 1.7 | — | |
| V_{OUT} fall time | t_f | | — | 1.7 | — | |
| Common-mode transient immunity | CMTI | $V_{CM} = 1$ kV, $T_a = 25$ °C | 15 | 20 | — | kV/ μ s |

Note: All typical values are at $T_a = 25$ °C.

C_L is less than 15 pF which includes probe and stray wiring capacitance.

11. Isolation Characteristics (Unless otherwise specified, $T_a = 25$ °C)

| Characteristics | Symbol | Note | Test Condition | Min | Typ. | Max | Unit |
|-------------------------------------|--------|----------|---------------------------------|-----------|-----------|-----|------------------|
| Total capacitance (input to output) | C_S | (Note 1) | $V_S = 0$ V, $f = 1$ MHz | — | 1.0 | — | pF |
| Isolation resistance | R_S | (Note 1) | $V_S = 500$ V, R.H. ≤ 60 % | 10^{12} | 10^{14} | — | Ω |
| Isolation voltage | BV_S | (Note 1) | AC, 60 s | 5000 | — | — | V _{rms} |

Note 1: This device is considered as a two-terminal device: Pins 1, 2, 3 and 4 are shorted together, and pins 5, 6, 7 and 8 are shorted together.

12. Characteristics Curves (Note)

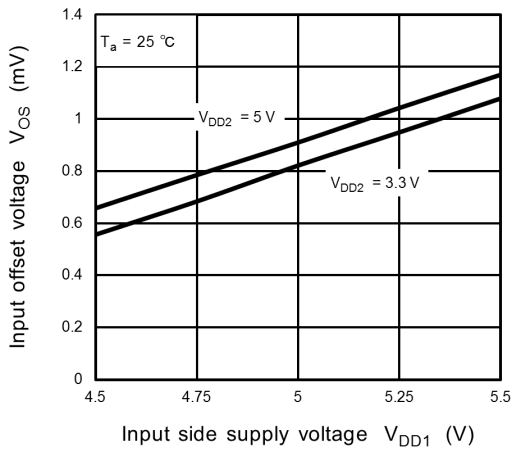


Fig. 12.1 $V_{OS} - V_{DD1}$

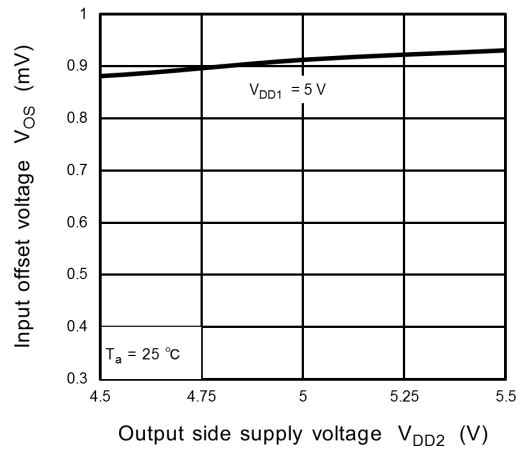


Fig. 12.2 $V_{OS} - V_{DD2}$

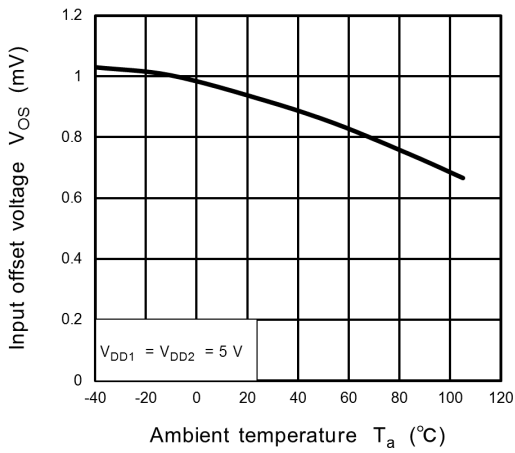


Fig. 12.3 $V_{OS} - T_a$

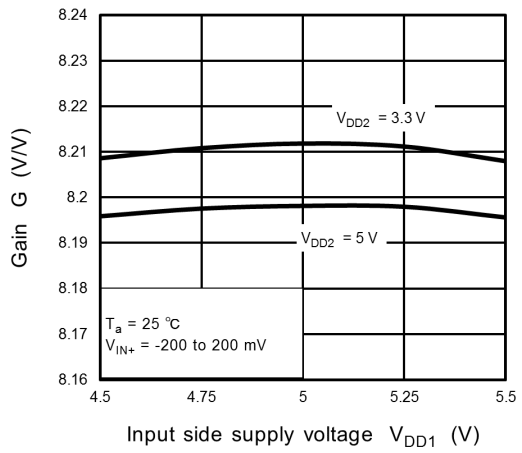


Fig. 12.4 $G - V_{DD1}$

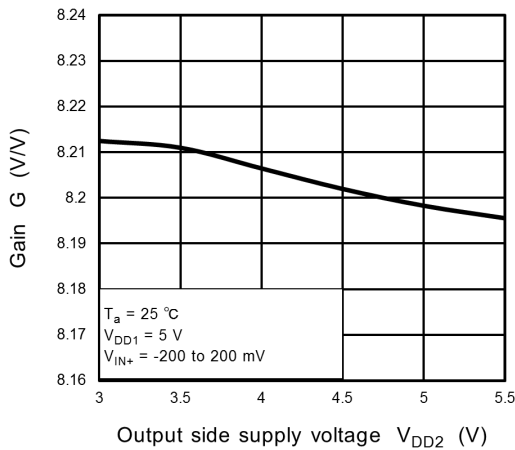


Fig. 12.5 $G - V_{DD2}$

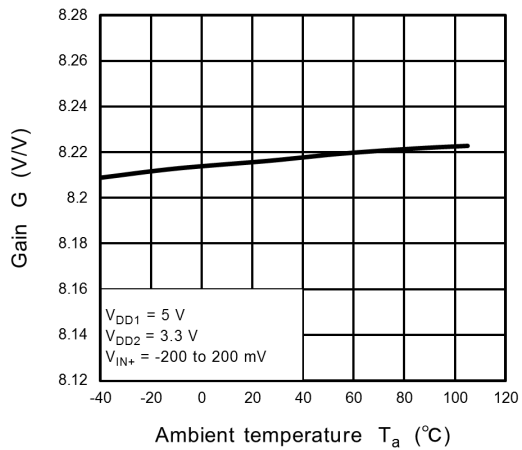


Fig. 12.6 $G - T_a$

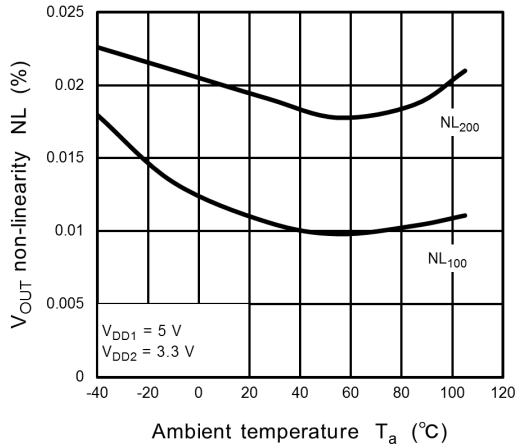


Fig. 12.7 NL - T_a

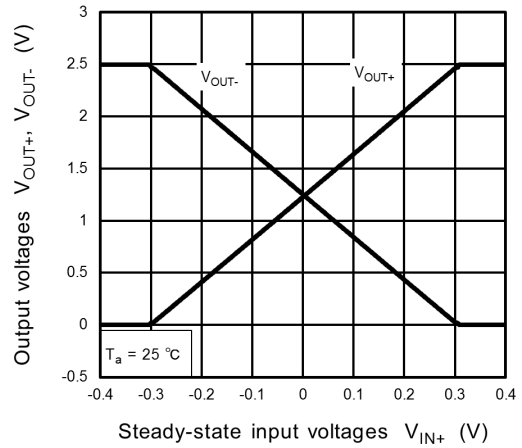


Fig. 12.8 $V_{OUT} - V_{IN+}$

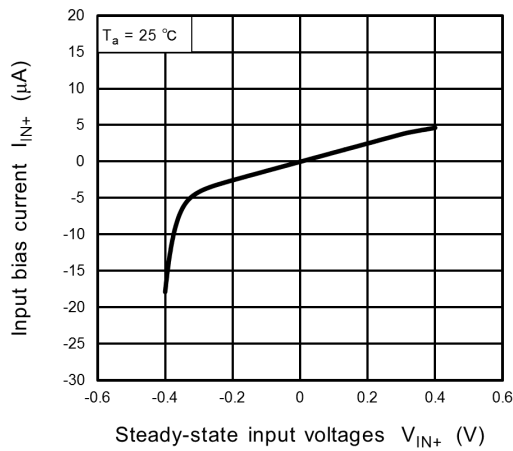


Fig. 12.9 $I_{IN+} - V_{IN+}$

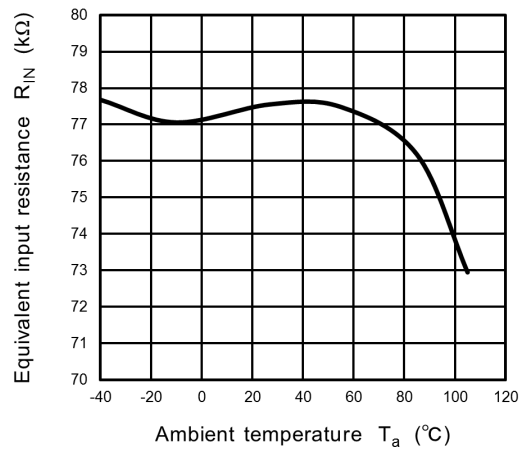


Fig. 12.10 $R_{IN} - T_a$

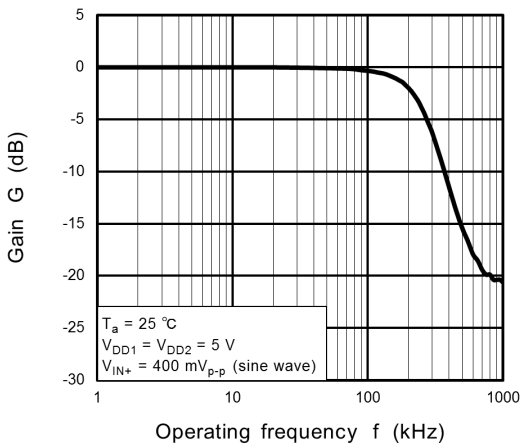


Fig. 12.11 $G[dB] - f$

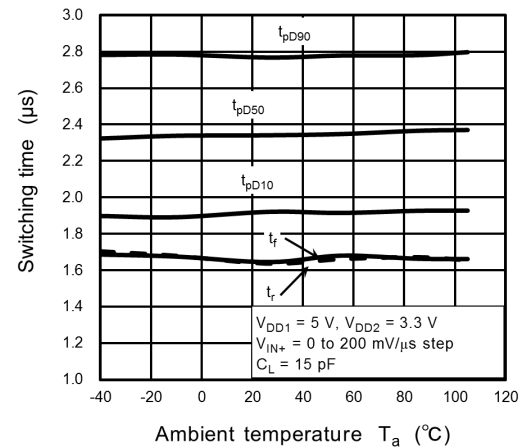


Fig. 12.12 Switching Time - T_a

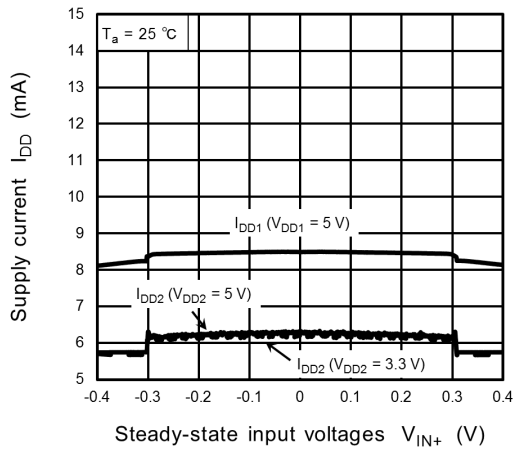


Fig. 12.13 $I_{DD} - V_{IN+}$

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

13. Soldering and Storage

13.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

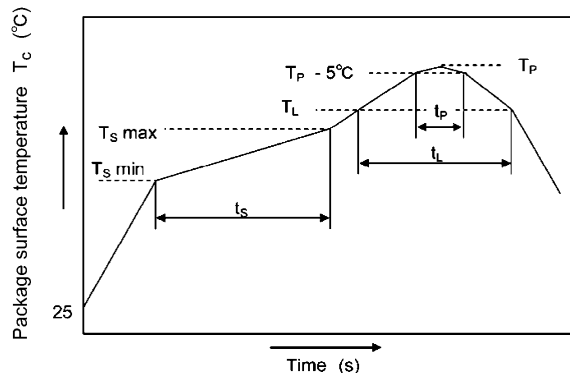
- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.

(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



| | Symbol | Min | Max | Unit |
|--|--------|-----|-----|------|
| Preheat temperature | T_S | 150 | 200 | °C |
| Preheat time | t_s | 60 | 120 | s |
| Ramp-up rate (T_L to T_P) | | | 3 | °C/s |
| Liquidus temperature | T_L | 217 | | °C |
| Time above T_L | t_L | 60 | 150 | s |
| Peak temperature | T_P | | 260 | °C |
| Time during which T_c is between ($T_P - 5$) and T_P | t_p | | 30 | s |
| Ramp-down rate (T_P to T_L) | | | 6 | °C/s |

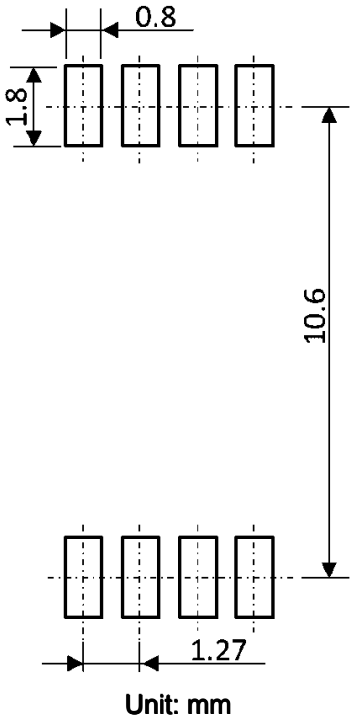
An Example of a Temperature Profile When Lead(Pb)-Free Solder Is Used

- When using soldering flow
Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
Mounting condition of 260 °C within 10 seconds is recommended.
Flow soldering must be performed once.
- When using soldering Iron
Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
Heating by soldering iron must be done only once per lead.

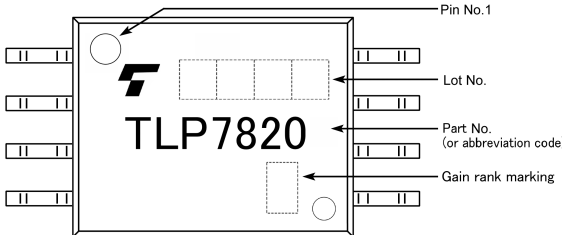
13.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

14. Land Pattern Dimensions (for reference only)



15. Marking



16. EN 60747-5-5 Option (D4) Specification

- Part number: TLP7820 (**Note 1**)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN 60747.

Example: TLP7820(D4ATP4,E)

D4 : EN 60747 option

A : Gain rank

TP4 : Tape type

E : [[G]]/RoHS COMPATIBLE (**Note 2**)

Note 1: Use TOSHIBA standard type number for safety standard application.

e.g., TLP7820(D4ATP4,E → TLP7820

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

| Description | Symbol | Rating | Unit |
|--|--|---|----------------|
| Application classification for rated mains voltage ≤ 600 Vrms for rated mains voltage ≤ 1000 Vrms | | I-IV I-III | — |
| Climatic classification | | 40 / 105 / 21 | — |
| Pollution degree | | 2 | — |
| Maximum operating insulation voltage | VIORM | 1414 | Vpeak |
| Input to output test voltage, Method A $V_{pr} = 1.6 \times VIORM$, type and sample test $t_p = 10$ s, partial discharge < 5 pC | Vpr | 2262 | Vpeak |
| Input to output test voltage, Method B $V_{pr} = 1.875 \times VIORM$, 100 % production test $t_p = 1$ s, partial discharge < 5 pC | Vpr | 2652 | Vpeak |
| Highest permissible overvoltage (transient overvoltage, $t_{pr} = 60$ s) | VTR | 8000 | Vpeak |
| Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F , $P_{so} = 0$) power (output or total power dissipation) temperature | I _{si} P _{so} T _s | 300 700 150 | mA mW °C |
| Insulation resistance VIO = 500 V, Ta = 25 °C VIO = 500 V, Ta = 100 °C VIO = 500 V, Ta = Ts | Rsi | $\geq 10^{12}$ $\geq 10^{11}$ $\geq 10^9$ | Ω |

Fig. 16.1 EN 60747 Insulation Characteristics

| | | |
|------------------------------|-----|--------|
| Minimum creepage distance | Cr | 8.0 mm |
| Minimum clearance | Cl | 8.0 mm |
| Minimum insulation thickness | ti | 0.4 mm |
| Comparative tracking index | CTI | 500 |

Fig. 16.2 Insulation Related Specifications (Note)

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.



Fig. 16.3 Marking on Packing

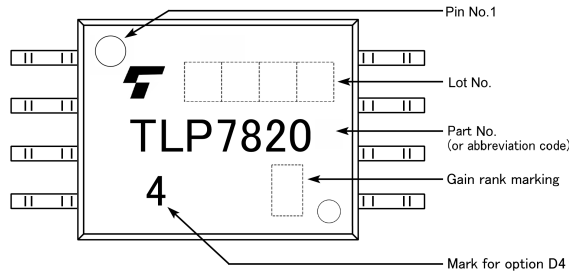


Fig. 16.4 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.

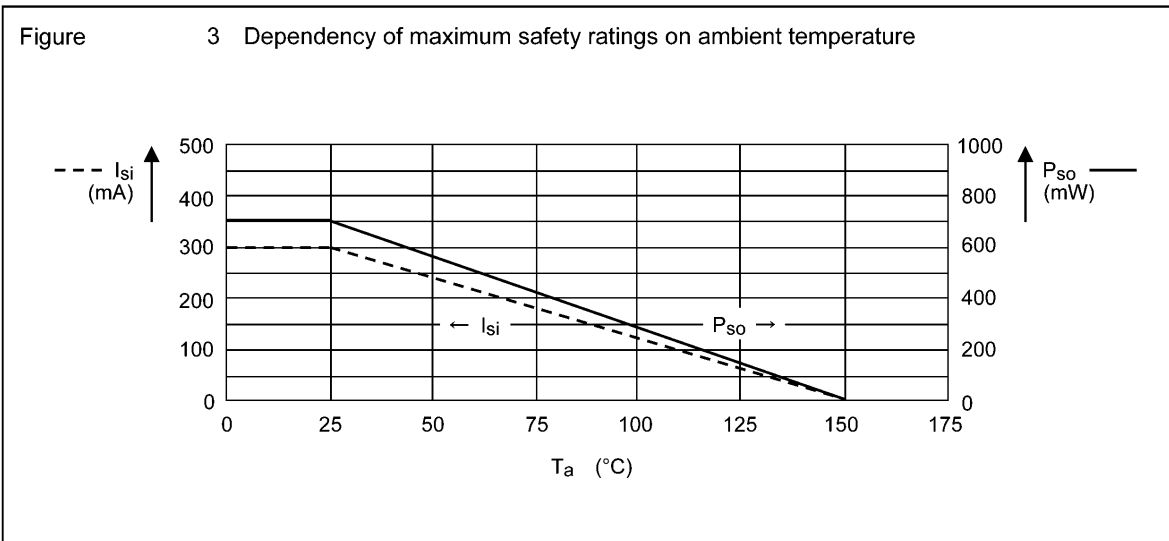
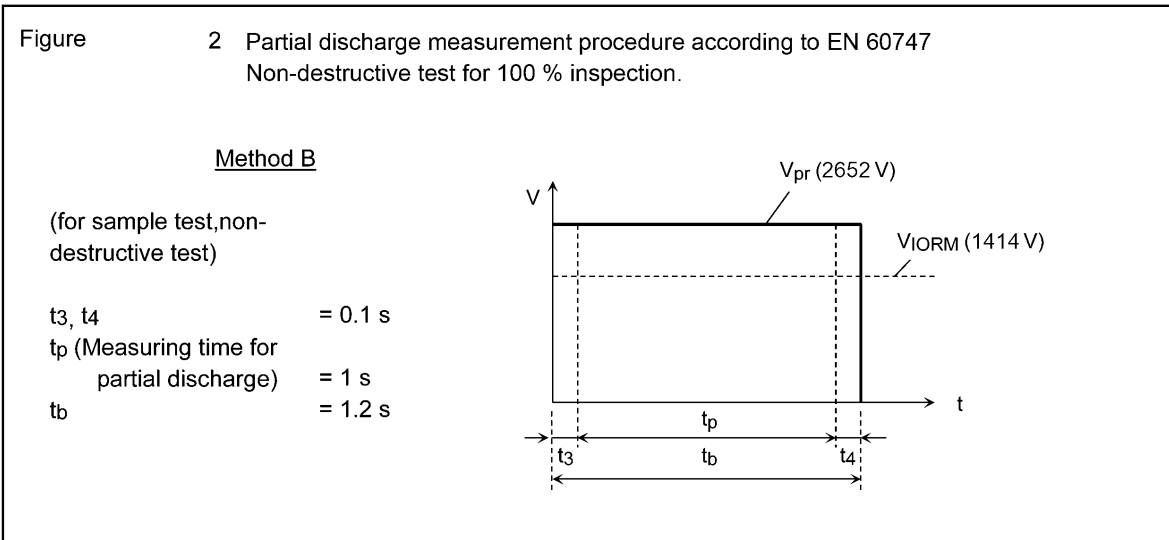
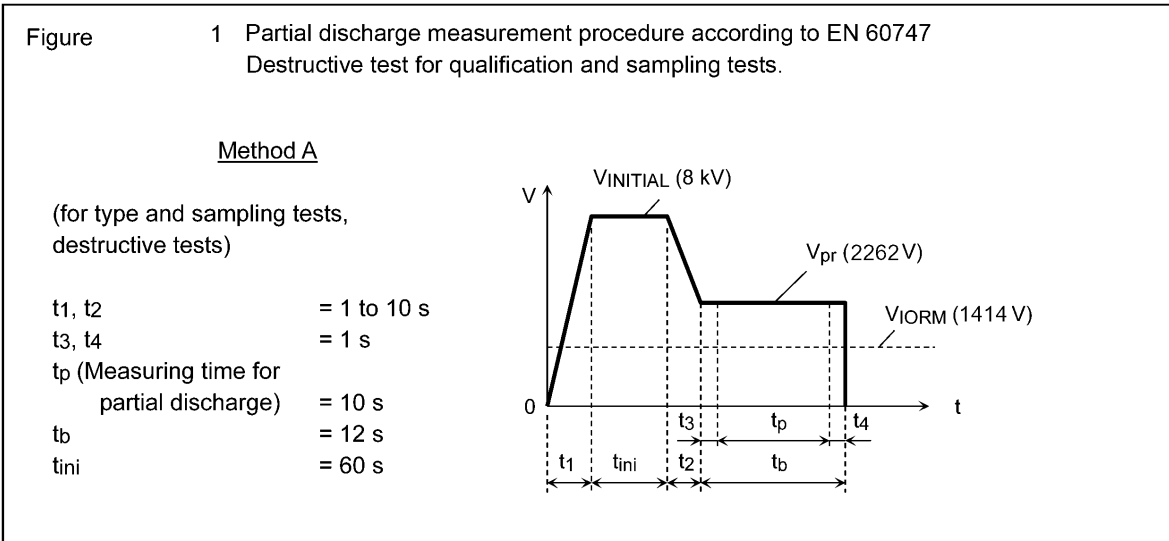
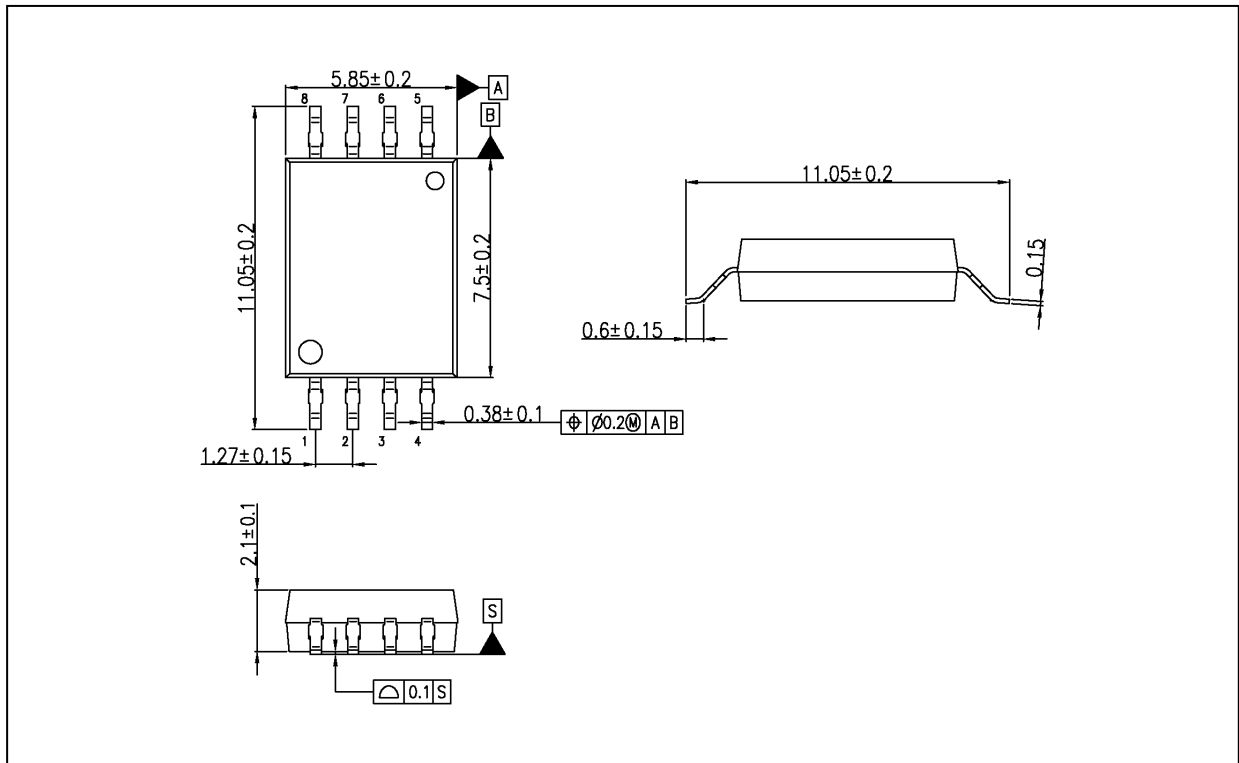


Fig. 16.5 Measurement Procedure

Package Dimensions

Unit: mm



Weight: 0.205 g (typ.)

| Package Name(s) |
|------------------|
| TOSHIBA: 11-6B1A |

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