TOSHIBA Field Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

SSM3J133TU

O Power Management Switch Applications

1.5V drive
 Low ON-resistance: R_{DS(ON)} = 88.4 mΩ (max) (@V_{GS} = -1.5 V)

 $R_{DS(ON)} = 56.0 \text{ m}\Omega \text{ (max) (@V_{GS} = -1.8 V)}$

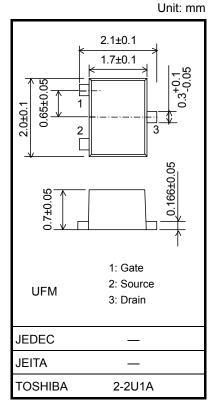
 $R_{DS(ON)} = 39.7 \text{ m}\Omega \text{ (max) (@V_{GS} = -2.5 V)}$

 $R_{DS(ON)} = 29.8 \text{ m}\Omega \text{ (max) (@V_{GS} = -4.5 V)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol		Rating	Unit	
Drain-source voltage		V_{DSS}		-20	V	
Gate-source voltage		V _{GSS}		± 8	V	
Drain current	DC	I _D (Note1)		-5.5	Α	
	Pulse	I _{DP} (Note1)		-11.0		
power dissipation		P _D (Note2)		500	mW	
			t<1s	1000	IIIVV	
Channel temperature		T _{ch}		150	°C	
Storage temperature range		T _{stg}		-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.



weight: 6.6 mg (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

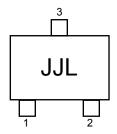
Note1: The channel temperature should not exceed 150°C during use.

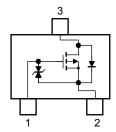
Note2: Mounted on FR4 board

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{Cu Pad: } 645 \text{ mm}^2)$

Marking

Equivalent Circuit (Top view)





Start of commercial production 2011-02

Electrical Characteristics (Ta = 25°C)

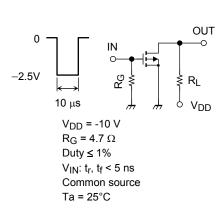
Chara	cteristics	Symbol	Test Conditions		Min	Тур.	Max	Unit
Drain-source breakdown voltage		V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$		-20	_	_	V
		V (BR) DSX	I _D = -1 mA, V _{GS} = 5 V	(Note 4)	-15	_		V
Drain cut-off current		I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V		_	_	-1	μΑ
Gate leakage current		I _{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±1	μΑ
Gate threshold voltage		V _{th}	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ mA}$		-0.3	_	-1.0	V
Forward transfer admittance		Y _{fs}	V _{DS} = -3 V, I _D = -1.0 A	(Note 3)	5.2	10.4	_	S
Drain-source ON-resistance	R _{DS} (ON)	I _D = -3.0 A, V _{GS} = -4.5 V	(Note 3)	_	24.9	29.8	· mΩ	
		I _D = -2.5 A, V _{GS} = -2.5 V	(Note 3)	_	31.1	39.7		
		I _D = -1.5 A, V _{GS} = -1.8 V	(Note 3)	_	38.8	56.0		
		I _D = -0.5 A, V _{GS} = -1.5 V	(Note 3)	_	47.4	88.4		
Input capacitance		C _{iss}	V - 40 V V - 0 V		_	840		pF
Output capacitance		Coss	V _{DS} = -10 V, V _{GS} = 0 V f = 1 MHz		_	118	_	
Reverse transfer capacitance		C _{rss}	11 - 1 IVIDZ		_	99		
Switching time	Turn-on time	t _{on}	V _{DD} = -10 V, I _D = -2.0 A		_	32	_	ns
	Turn-off time	t _{off}	V_{GS} = 0 to -2.5 V, R_{G} = 4.7 Ω		_	107	_	
Total gate charge		Qg	\/ 40\/ I 40A		_	12.8	_	nC
Gate-source charge		Q _{gs1}	$V_{DD} = -10 \text{ V}, I_D = -4.0 \text{ A},$		_	1.4	_	
Gate-drain charge		Q _{gd}	V _{GS} = -4.5 V		_	3.0	_	
Drain-Source forward voltage		V _{DSF}	I _D = 5.5A, V _{GS} = 0 V	(Note3)	_	0.83	1.2	V

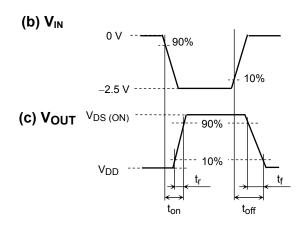
Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

(a) Test Circuit





Notice on Usage

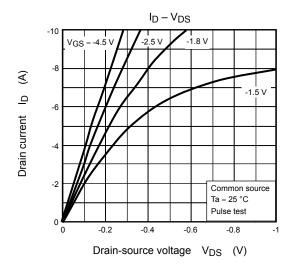
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (-1 mA for the SSM3J133TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

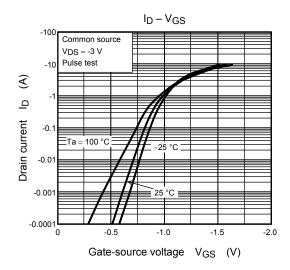
Take this into consideration when using the device.

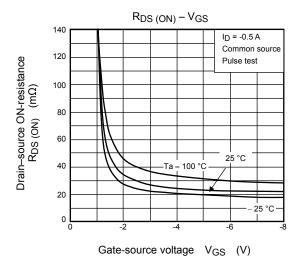
Handling Precaution

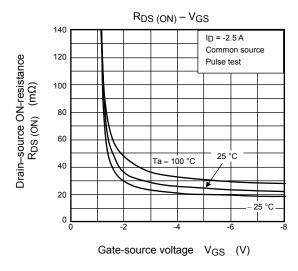
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

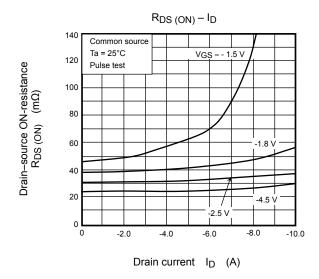
Thermal resistance $R_{th\ (ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

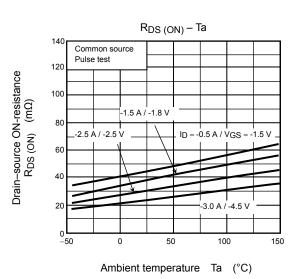




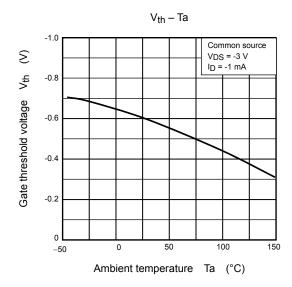


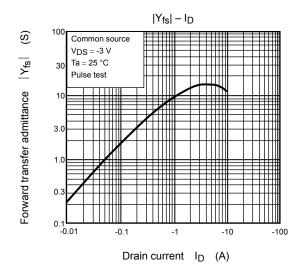


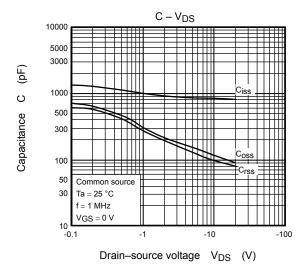


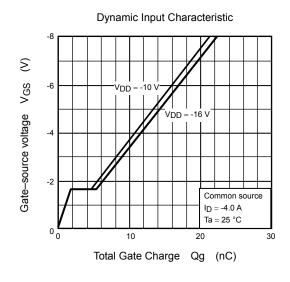


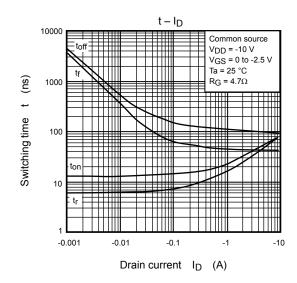
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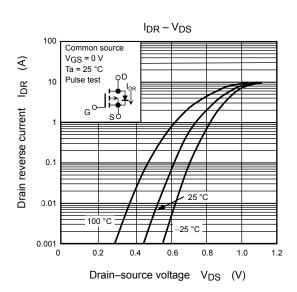


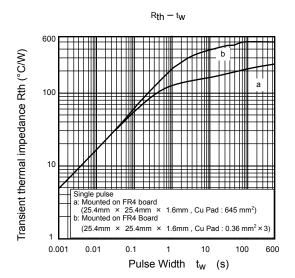


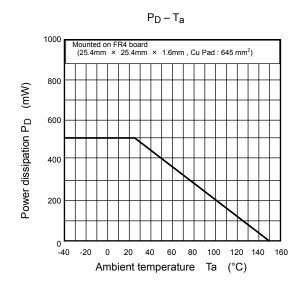












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