TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

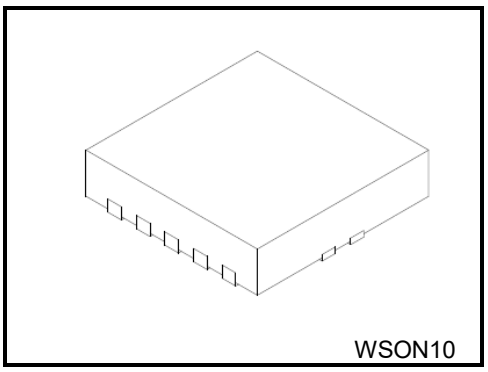
TCKE712BNL

13.2 V, eFuse with Adjustable Over Current Protection Over Voltage Protection and Slew Rate Control

The TCKE712BNL is 13.2 V high input voltage Single Inputs－Single Output eFuse IC. It can be used as a reusable fuse, and other protection features like adjustable over current limit by an external resistor, short circuit protection, adjustable slew rate control by an external capacitance, adjustable over voltage protection, under voltage protection, thermal shutdown and FLAG function.

Switch ON resistance is only 53 mΩ, Wide input voltage operation characteristics makes this product ideal for power management such as in the Power Stage of Hard disk drive and Battery Charge applications.

This device is available in 0.5 mm pitch ultra small package WSON10 (3.0 mm x 3.0 mm, t: 0.7 mm (typ)) .Thus this device is ideal for various application such as portable applications that require high-density board.



Weight : 19.7 mg (typ.)

Feature

- High input voltage: $V_{IN\ max}$ = 13.2 V
- Low ON resistance : R_{ON} = 53 mΩ (typ.)
- Adjustable over current protection
- Adjustable over voltage protection
- Programmable Slew rate control by External Capacitance for Inrush current reduction
- FLAG indicates
- Reverse current blocking (SW OFF state)
- Thermal Shutdown
- Small package:WSON10 (3.0 mm x 3.0 mm, t: 0.7 mm (typ))
- IEC62368-1 Certified

Start of commercial production
2020-11

Absolute Maximum Ratings (Ta = 25 °C)

Characteristics	Symbol	Rating	Unit
Input voltage	V_{IN}	-0.3 to 18	V
ILIM voltage	V_{ILIM}	-0.3 to 6	V
dV/dT voltage	$V_{dV/dT}$	-0.3 to 6	V
OVP voltage	V_{OVP}	-0.3 to 6	V
Control voltage	V_{EN}	-0.3 to 18	V
Output voltage	V_{OUT}	-0.3 to 18	V
$\overline{\text{FLAG}}$ voltage	V_{FLAG}	-0.3 to 18	V
$\overline{\text{FLAG}}$ Sink current	I_{SINK_FLAG}	0 to 1	mA
Power dissipation	P_D	2.4 (Note 1)	W
Junction temperature	Tj	150	°C
Storage temperature	T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

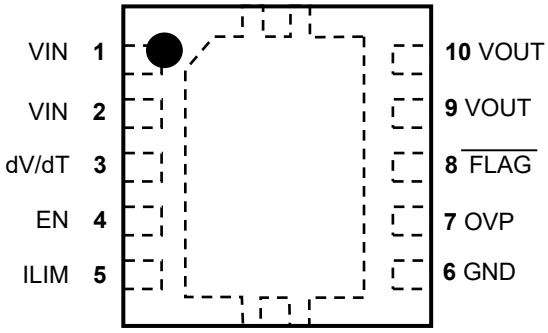
Note1: Rating at mounting on a board: FR4 board. (76.2 mm × 114.3 mm × 1.6 mm, 4 layer)

Operating Ranges

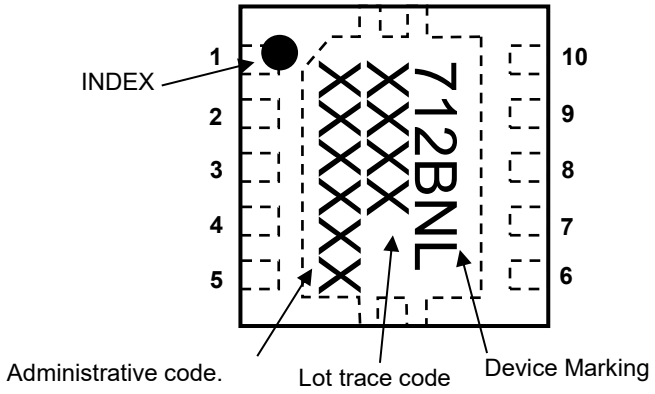
Characteristics	Symbol	Ranges		Unit
Input voltage	V_{IN}	4.4 to 13.2		V
ILIM External resistance	R_{ILIM}	4.4 V ≤ VIN ≤ 5.5 V	1.7 to 12	kΩ
		5.5 V < VIN ≤ 9.9 V	2.4 to 12	
		9.9 V < VIN ≤ 13.2 V	3.1 to 12	
Control voltage	V_{EN}	0 to 18		V
$\overline{\text{FLAG}}$ Voltage	V_{FLAG}	0 to 18		V
$\overline{\text{FLAG}}$ Sink current	I_{SINK_FLAG}	0 to 1		mA
Operating Ambient temperature range	$Ta_{\_opr}$	−40 to 85		°C
External capacitance	$C_{dV/dT}$	1000(max)		nF

Pin Assignment (Top view)

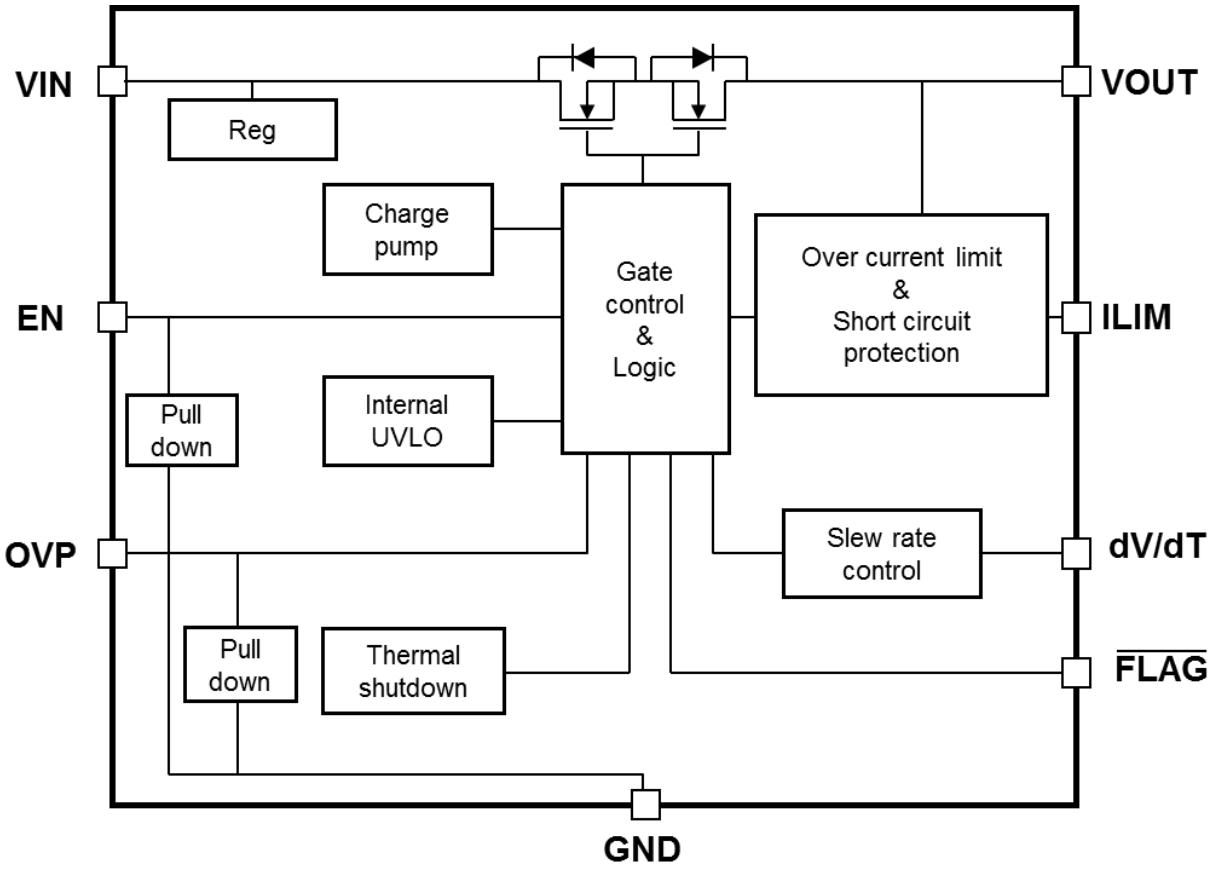
WSON10



Top Marking (Top view)



Block Diagram



PIN Description

PIN Name	Description
VIN	Supply Input. Input to the power switch and the supply voltage for the device.
dV/dT	Rise time set input. A capacitor between dV/dT terminal and GND set the slew rate of V_{OUT}.
EN	Enable input.
ILIM	Current limit set input. A resistor between ILIM terminal and GND set the current limit.
GND	Ground.
OVP	Over voltage protection(OVP) threshold set input.-The threshold voltage of the overvoltage protection function is adjusted by the resistance value connected to the OVP terminal.
$\overline{\text{FLAG}}$	Open drain signal output. Fault condition flag
VOUT	Output. Output of the power switch.

Operation Logic Table

	EN “Low”	EN “High”
Output	OFF	**ON**

TCKE712BNL DC Characteristics
(Unless otherwise specified,Ta = -40 to 85 °C, V_{IN} = 12 V, R_{ILIM} = 3.6 kΩ)

Characteristics	Symbol	Test Condition	Ta = 25℃			Ta = −40 to 85℃ (Note 2)		Unit
			Min.	Typ.	Max.	Min.	Max.	
Basic operation								
VIN under voltage lockout (UVLO) threshold, rising	V_{IN_UVLO}	—	—	4.15	—	4.00	4.4	V
VIN under voltage lockout (UVLO) hysteresis	V_{IN_UVhyst}	—	—	0.2	—	—	—	V
EN threshold voltage, rising	V_{ENR}	—	—	1.1	—	—	1.2	V
EN threshold voltage, falling	V_{ENF}	—	—	0.95	—	0.85	—	V
On resistance	R_{ON}	I_{OUT} = 1 A,	—	53	—	—	80	mΩ
Quiescent current (ON state)	I_Q	V_{EN} = 3 V, I_{OUT} = 0 A	—	690	—	—	852	μA
Quiescent current (OFF state)	$I_{Q(OFF)}$	EN = 0 V	—	46	—	—	80	μA
Reverse blocking current	I_{RB}	V_{OUT} = 5 V, V_{IN} = 0 V, V_{EN} = 0 V	—	0.001	—	—	1.0	μA
EN pull down resistor	R_{EN}	EN = 1.1 V	—	20	—	10	55	MΩ
dV/dT control								
dV/dT Voltage	$V_{dV/dT}$	—	—	3.1	—	2.8	3.4	V
Charging Current	$I_{dV/dT}$	$V_{dV/dT}$ = 0 V	—	5	—	3.5	6.5	μA
dV/dT to OUT gain	$GAIN_{dV/dT}$	$V_{dV/dT}$ = 1V, I_{OUT} = 1A	—	9.0	—	8.5	9.5	—
Over voltage protection								
OVP threshold, rising	V_{OVPR}	—	—	1.2	—	1.14	1.26	V
OVP pull down resistor	R_{OVP}	V_{OVP} = 1.2 V	—	22	—	11	60	MΩ
$\overline{\text{FLAG}}$								
$\overline{\text{FLAG}}$ Output Low Voltage	V_{FLAG_L}	I_{SINK_FLAG} = 1 mA	—	—	—	—	0.1	V
$\overline{\text{FLAG}}$ Output High leakage	I_{FLAG_LEAK}	V_{FLAG} = 18 V	—	—	—	—	1	μA
Over current protection								
Over current limit (Note3)	I_{OUT_CL}	V_{IN} = 5 V, R_{ILIM} = 1.7 kΩ, V_{IN} - V_{OUT} = 2 V	—	3.65	—	3.14	4.14	A
		V_{IN} = 9 V, R_{ILIM} = 2.4 kΩ, V_{IN} - V_{OUT} = 2 V	—	2.58	—	2.21	2.99	A
		V_{IN} = 12 V, R_{ILIM} = 3.1 kΩ, V_{IN} - V_{OUT} = 2 V	—	2.00	—	1.71	2.35	A
		V_{IN} = 12 V, R_{ILIM} = 3.6 kΩ, V_{IN} - V_{OUT} = 2 V	—	1.72	—	1.47	2.04	A
		V_{IN} = 12 V, R_{ILIM} = 6.2 kΩ, V_{IN} - V_{OUT} = 2 V	—	1.00	—	0.78	1.21	A
		V_{IN} = 12 V, R_{ILIM} = 12 kΩ, V_{IN} - V_{OUT} = 2 V	—	0.51	—	0.35	0.64	A
Fast trip comparator level	$I_{FASTTRIP}$	—	—	I_{OUT_CL} × 2.5	—	I_{OUT_CL} × 2.0	—	A
Thermal Protection								
Thermal shut down Threshold	T_{SD}	Tj	—	134	—	—	—	°C

Note2: This parameter is warranted by design.

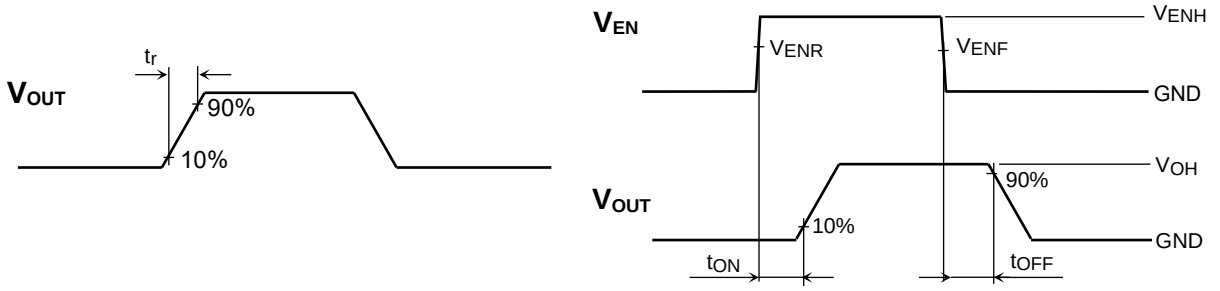
Note3: Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

TCKE712BNL AC Characteristics
(Unless otherwise specified,Ta = -40 to 85 °C, V_{IN} = 12 V, R_{ILIM} = 3.6kΩ, R_{LOAD} = 12 Ω, C_{IN} = C_{OUT} = 1 μF)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Turn on delay	t_{ON}	$C_{dV/dT}$ = OPEN (Note4)	—	370	—	μs
Turn off delay	t_{OFF}	— (Note4)	—	2.2	—	μs
V_{OUT} rise time	tr	$C_{dV/dT}$ = OPEN (Note4)	—	57	—	μs
		$C_{dV/dT}$ = 22nF (Note4)	—	4.7	—	ms
Fast trip time	$t_{FASTTRIP}$	I_{OUT} > $I_{FASTTRIP}$ to I_{OUT} peak (Note4)	—	320	—	ns
Current limit response time	t_{OL}	R_{LOAD} = OPEN to 3.6 Ω	—	175	—	μs
Over current $\overline{FLAG}$ blanking time/Switch off delay under over current	$t_{FLAGblank}$	OCL detection to V_{FLAG} = Low voltage (Note4)	3.3	5.5	—	ms
Short-term (<5ms) over current limit counting time	t_{OCP_COUNT}	Refer to Figure 4 (Note4)	—	176	—	ms

Note4: This parameter is warranted by design.

AC Waveform



V_{ENH} is the input voltage of EN pin larger than V_{ENR}.
V_{OH} is the typical output voltage the occurs with the output load.

Figure 1 t_r, t_{ON}, t_{OFF} Waveforms

Timing chart

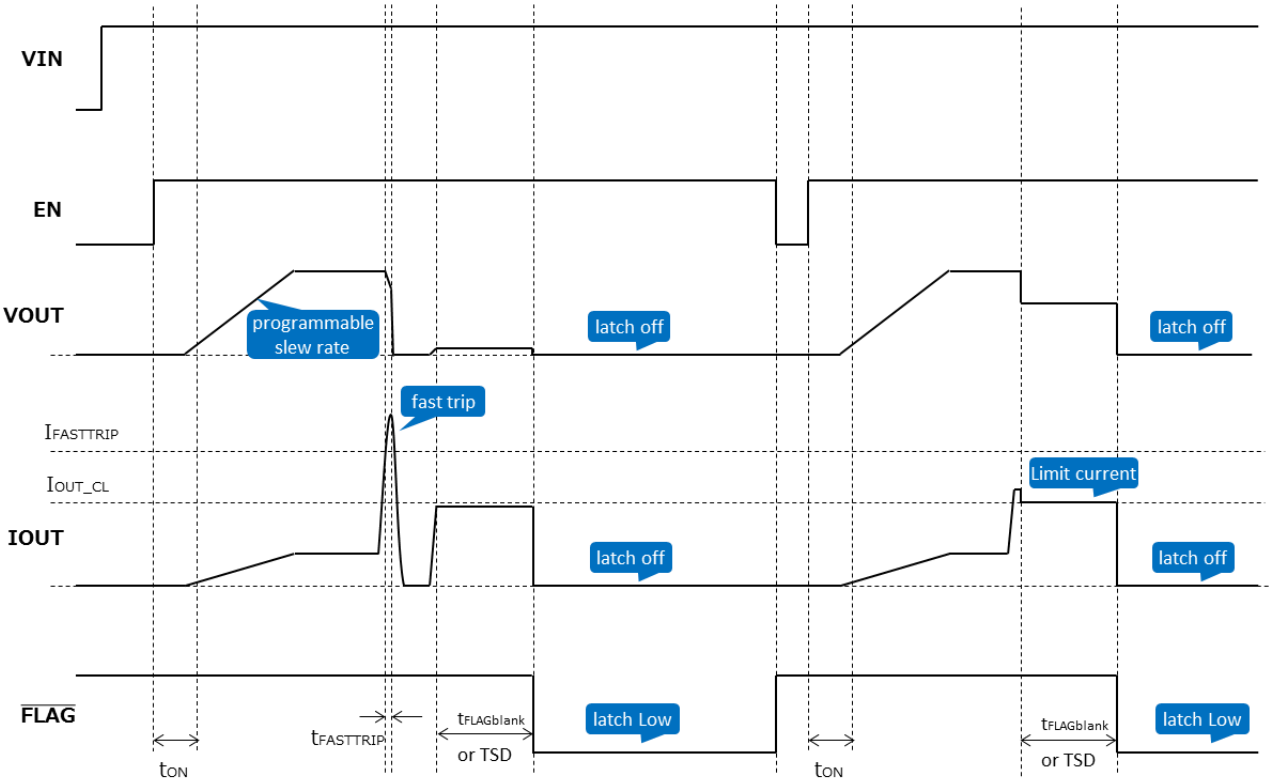
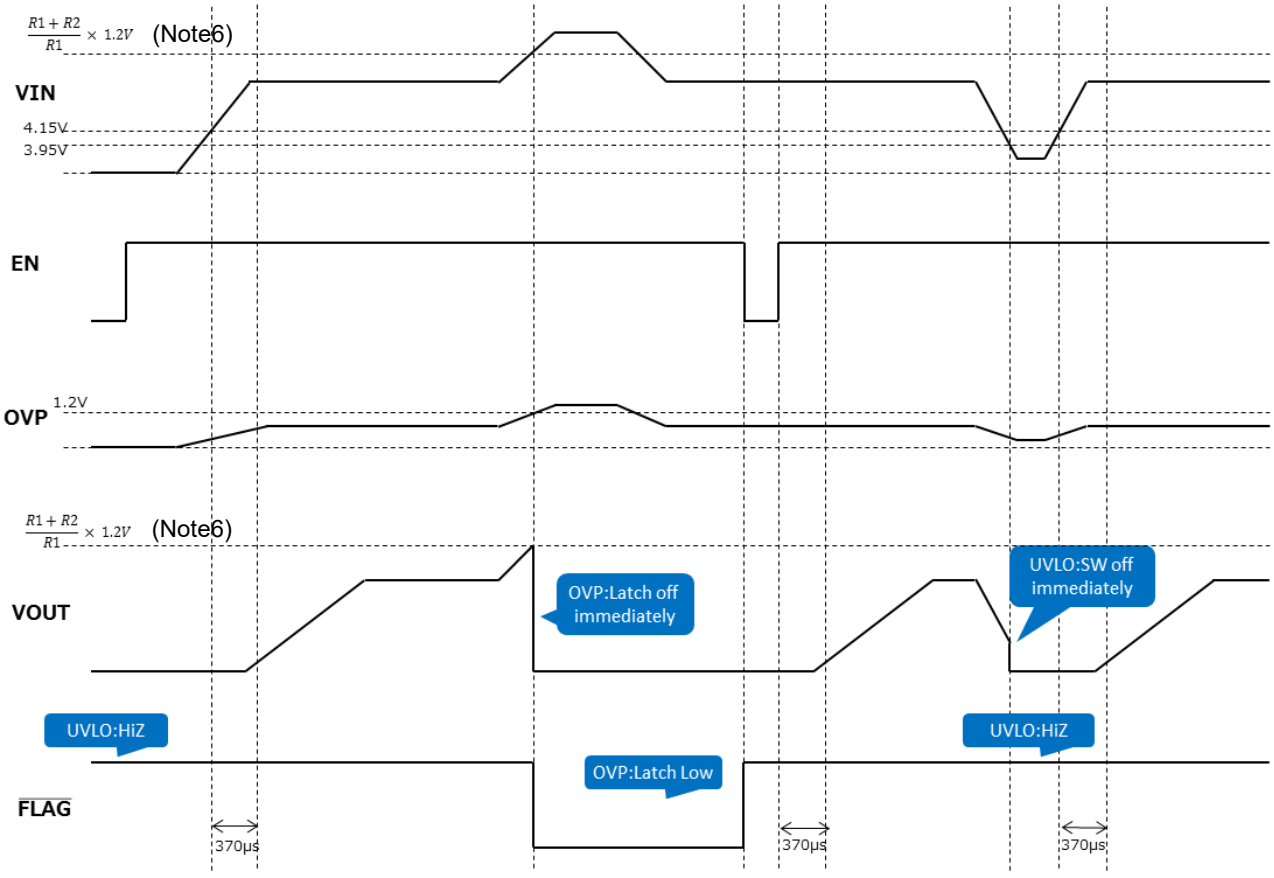


Figure 2 Short Circuit trip and Over current protection



(Note6: Refer to below “Application circuit example in Application Note “)

Figure 3 Under voltage lockout and Over voltage protection

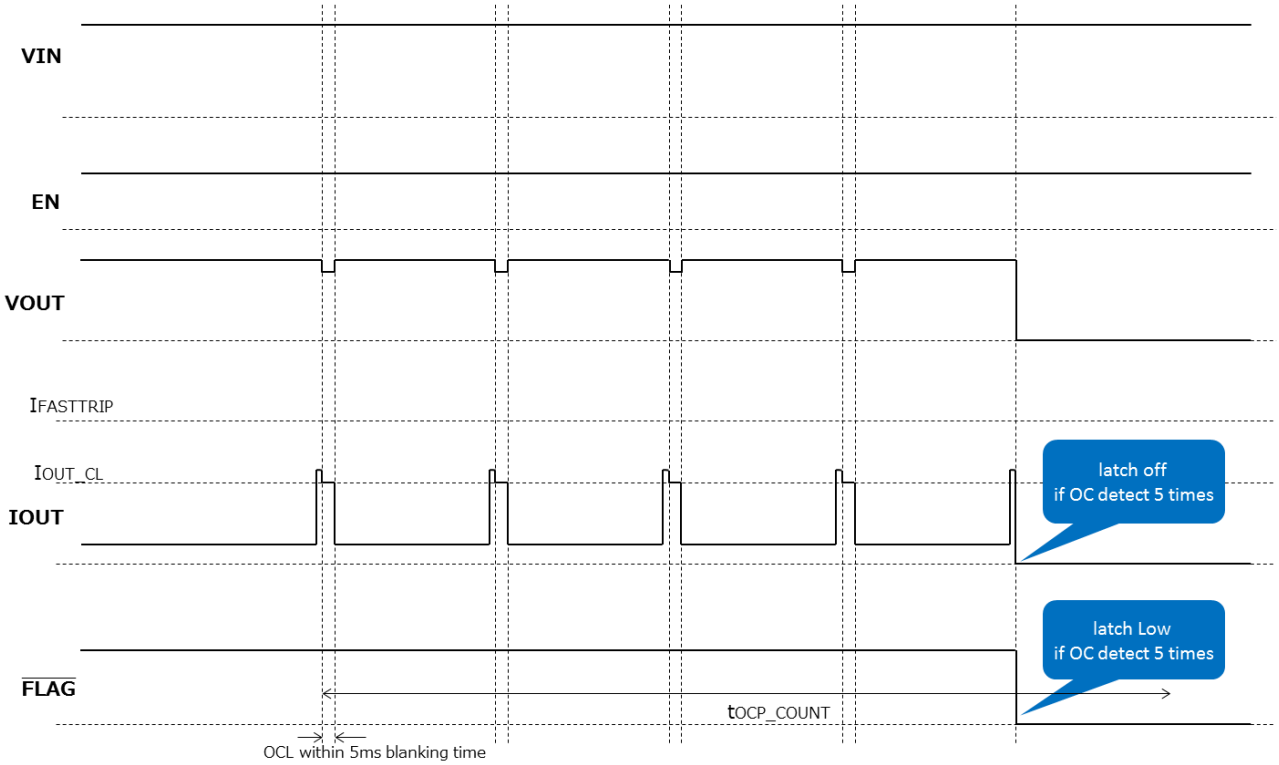
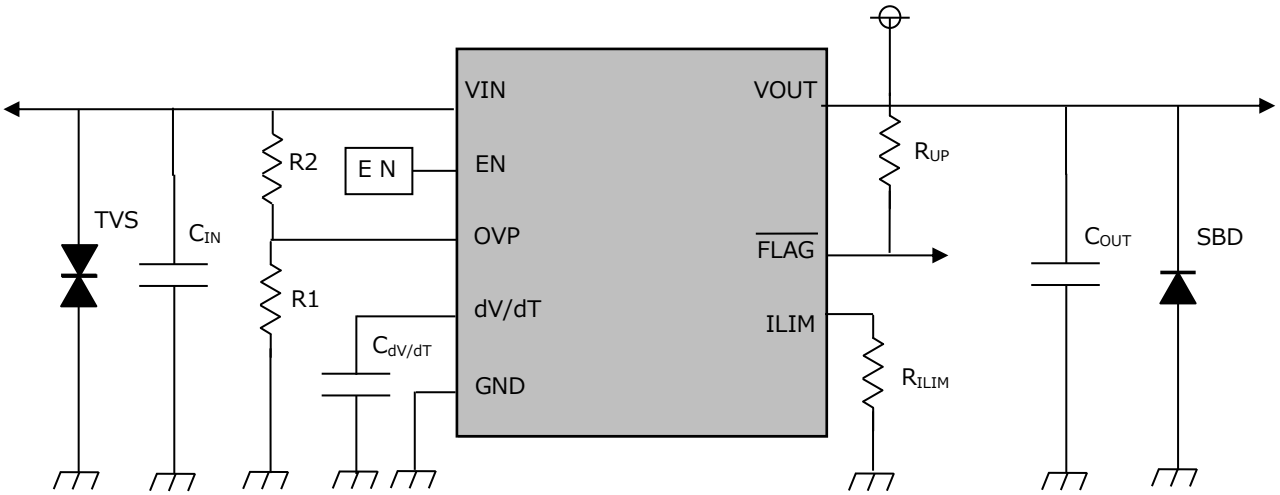


Figure 4 Short term overcurrent operation

Application Note

1. Application circuit example



1) Peripheral circuits

Connect the power supply to the input terminal VIN. During normal operation, almost the same voltage as the VIN voltage is output from the output terminal VOUT through the internal MOSFET.

If the current suddenly decreases, for example, when short-circuiting or overcurrent is protected, high-spike voltages may be generated due to back electromotive force of inductance components such as wirings connected to the input/output terminals of the eFuse IC, causing damage to the eFuse IC and resulting damage. In this case, a positive spike voltage is generated on the input side and a negative spike voltage is generated on the output side.

When designing boards, design patterns so that the length of the wires on the input-side and output-side of the eFuse IC is as short as possible. Also, the GND wiring area should be as wide as possible to reduce the impedance. C_{IN} functions to suppress the peak value against the positive spike voltage generated by the inputs. The peak value V_{SPIKE} of the spike voltage and the capacitance value of the C_{IN} have the following relationships. It can be understood that the spike voltage can be reduced by increasing the C_{IN}.

$$V_{SPIKE}\ (V)\ = V_{IN} + I_{OUT} \times \sqrt{\frac{L_{IN}}{C_{IN}}}$$

L_{IN}: effective inductance component of the input terminal (H), I_{OUT}: output current (A)

V_{SPIKE}: peak value of spiked voltage generated (V), V_{IN}: power supply voltage during normal operation (V)

TCKE712BNL recommends 1μF for C_{IN}, but make sure that V_{SPIKE} does not exceed the absolute maximum rating on the actual PCB board. It is also recommended to connect a TVS diode (ESD protection diode) to the input terminal and a SBD (Schottky barrier diode) to the output terminal.

By connecting a TVS diode to the input side of eFuse IC, you can protect from ESD. For negative spike voltage generated on the output side, an SBD can be connected to prevent the output potential from dropping more than GND. This protects not only the eFuse IC but also the ICs and devices connected as loads. Connect the SBD with the GND as the anode between the output terminal of the eFuse IC and the GND.

2. Setting the overcurrent protection function

Toshiba eFuse IC has a variable current limit. By selecting the external resistor R_{ILIM} of the I_{OUT_CL} terminal appropriately, the current limit can be set to the optimum value for each application. The I_{OUT_CL} calculation formula is shown below. However, the deviation between the theoretical value and the measured value is large when the current is 1A or lower. Be sure to check the resistance value with the actual machine when selecting the resistance value.

$$I_{OUT\_CL}\ (A) = 6200 / R_{ILIM}\ (\Omega)$$

R_{ILIM}: ILIM terminal external resistor (Ω)

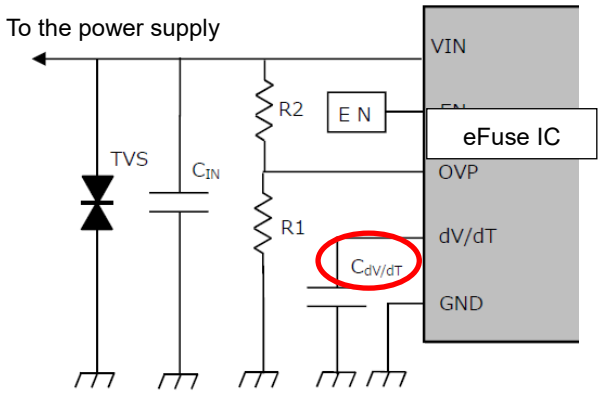
3. Setting of slew rate control for inrush current reduction

Toshiba eFuse IC has a variable inrush current function. The external capacitor at the dV/dT terminal can be used to appropriately set the rise time ($t_{dV/dT}$) of the output voltage. The formula for the rise time is as follows:

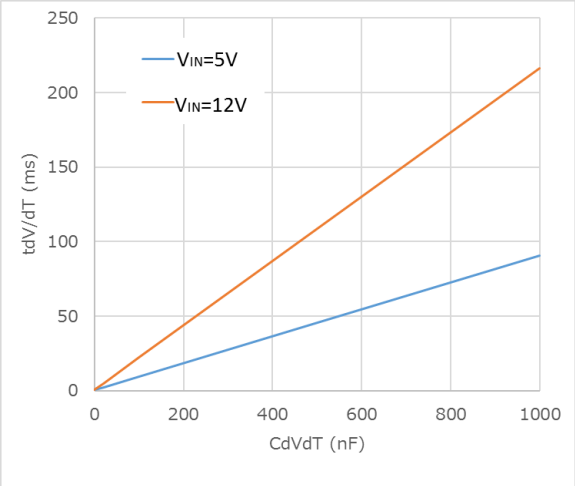
$$t_{dv/dt}\ (s) = 18 \times 10^{3} \times V_{IN} \times C_{dV/dT} + 4 \times 10^{-4}$$

V_{IN}: input voltage (V), $C_{dV/dT}$: external capacitance of dV/dT terminal (F)

The following chart shows the peripheral circuit diagram of the dV/dT terminal and graphs showing the relation between $C_{dV/dT}$ and $t_{dV/dT}$.



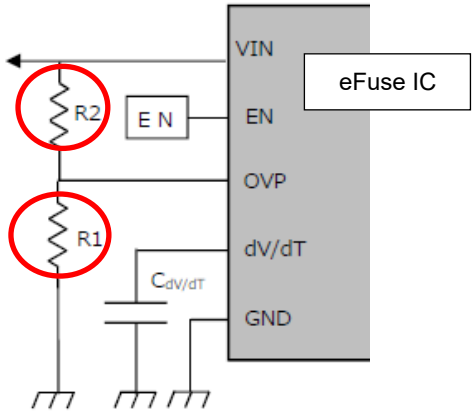
External Circuits around dV/dT Terminal



$C_{dV/dT}$-$t_{dV/dT}$ Characteristics

4. To change the operating voltage of the overvoltage function

Toshiba eFuse IC has an overvoltage function. By adding an external resistor to the OVP terminal, the operating voltage of the overvoltage function can be changed to an optimum value. An example of the circuit is shown in the figure below.



Connections of OVP terminal (VIN resistive division)

As shown in the drawing, operation is stopped when the input voltage drops by controlling the operation of the OVP terminal with the voltage obtained by dividing the input voltage by an external resistor. The operating voltage of the overvoltage function can be set to the optimum value by properly selecting the external resistance.
The equation for setting VIN(OVP) by controlling the external resistors R1 and R2 of the OVP terminal is as follows.

$$V_{IN(OVP)} = \frac{R1 + R2}{R1} \times V_{OVPR}$$

$V_{IN(OVP)}$: Operating voltage for overvoltage protection

5. FLAG function

Toshiba eFuse IC has a flag function. When the overvoltage protection function(OVP), the overcurrent protection function(OCP) and the thermal shutdown(TSD) are activated, the FLAG output circuit changes the FLAG terminal output from "H" to "L" .

This is a diagnostic function that outputs the alert to the outside of the IC when a system error has occurred. It is a. The FLAG terminal has an open drain structure, so pull up with an external resistor before use.

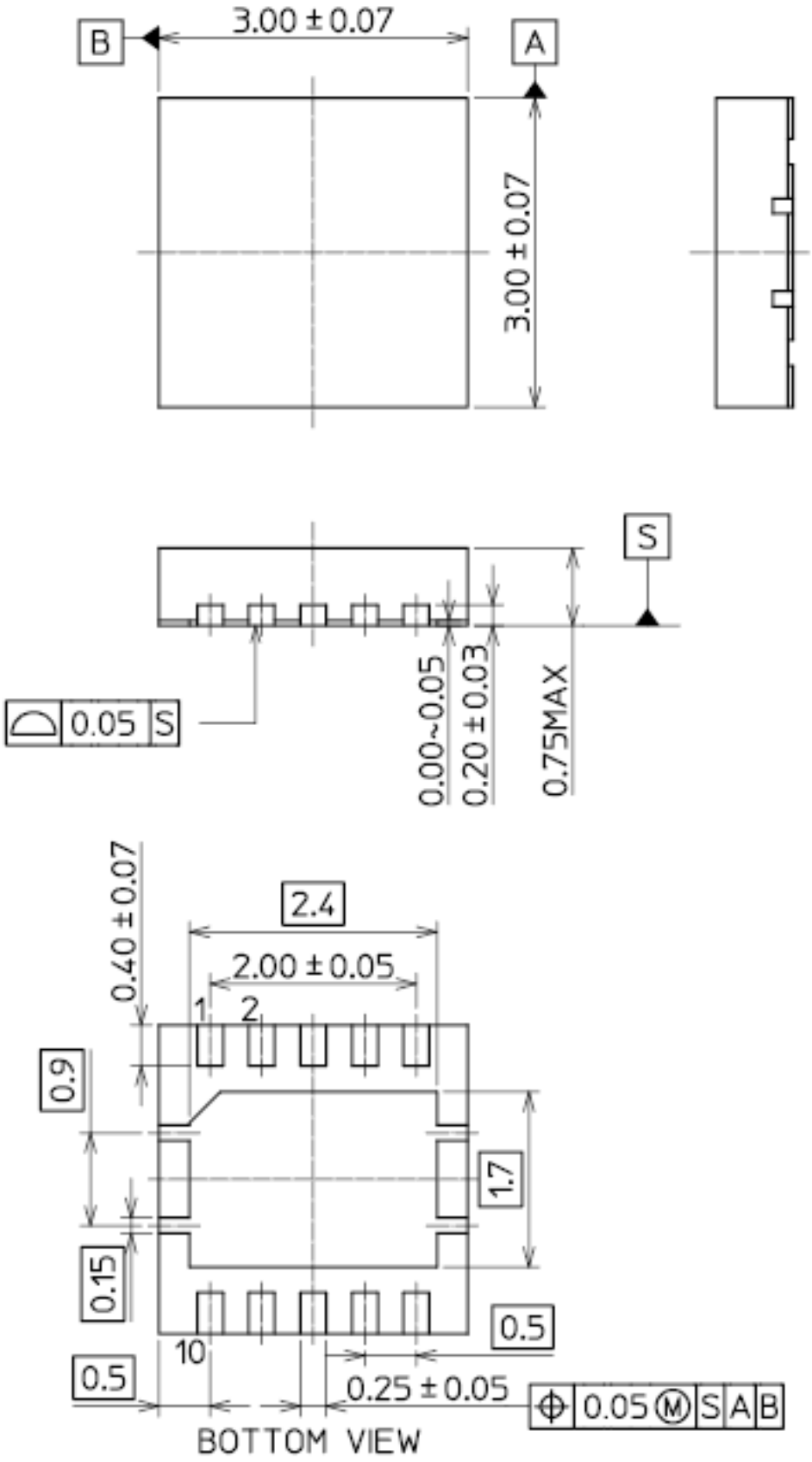
Select the pull-up resistor after fully considering the sink current (maximum rating) of the FLAG terminal (reference for pull-up resistor value: 100 kΩ to 1 MΩ). Also, please check with the actual device to determine the value of the pull-up resistor.

6. Precautions regarding protection functions

Toshiba eFuse IC has various protection functions. Be aware that not every function will cause the eFuse IC to cease functioning. When using these products, please read through and understand the concepts described and follow absolute maximum ratings from the information above or from our ‘Semiconductor Reliability Handbook’. Please operate these products below absolute maximum ratings in all instances. Furthermore, Toshiba highly recommends inserting failsafe systems into the design.

Package Dimensions

WSON10 Unit: mm



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