CMOS Digital Integrated Circuits Silicon Monolithic

TC7LX1108WBG

1. Functional Description

- Low-Voltage, Low-Power 8-Bit Dual-Supply Bus Transceiver with Auto Direction Sensing

2. General

The TC7LX1108WBG is an advanced high-speed dual-supply 8-bit bus transceiver fabricated with silicon-gate CMOS technology.

The TC7LX1108WBG is designed for use as an interface between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage systems.

The voltage translator automatically senses the direction of data transmission, eliminating the need for a direction control input. When the Output Enable (OE) input is low, the device is disabled, effectively isolating the buses.

All inputs and outputs of the TC7LX1108WBG can tolerate overvoltage conditions up to 3.6 V.

3. Features

(1) Voltage translation between arbitrary voltage levels from 1.2 V to 3.6 V.

(2) High-speed operation: t_{pd} = 4.7 ns (max) (V_{CCA} = 1.8 ± 0.15 V, V_{CCB} = 3.3 ± 0.3 V)

(3) Latch-up performance: ±300 mA

(4) ESD performance:

Machine model ≥ ±200 V, Human body model ≥ ±2000 V

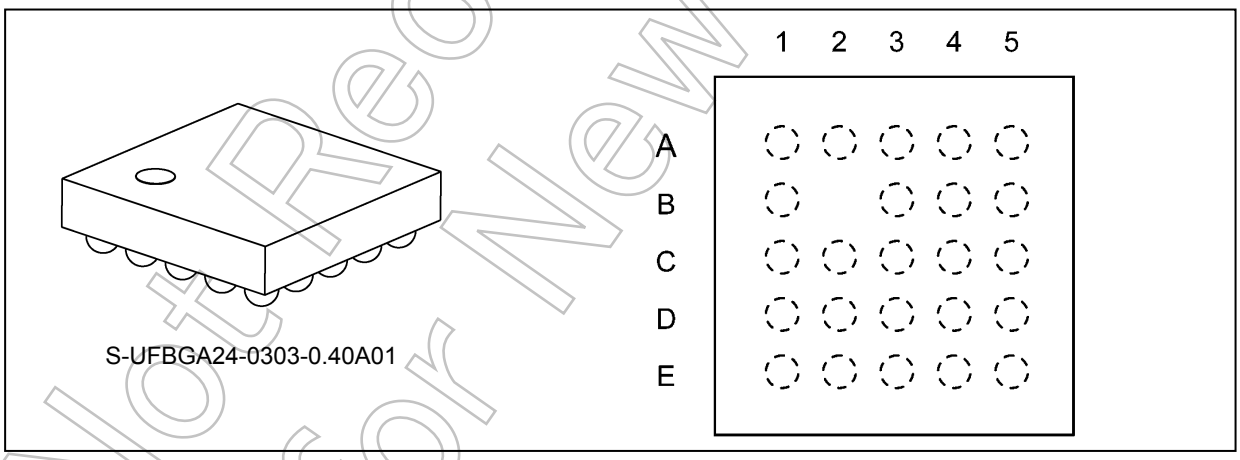
(5) Ultra-small package: WCSP24C

(6) The A-bus and B-bus are allowed to float. (when OE = Low)

(7) 3.6-V tolerant function and power-down protection provided on all inputs and outputs.

(8) All output ports are disabled when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

4. Packaging and Pin Assignment (Top View)



S-UFBGA24-0303-0.40A01

4.1. Pin Assignment

	1	2	3	4	5
A	B8	V_{CCB}	B7	B6	B5
B	A8	—	A7	A6	A5
C	GND	GND	V_{CCA}	GND	V_{CCA}
D	A4	OE	A3	A2	A1
E	B4	V_{CCB}	B3	B2	B1

5. Marking

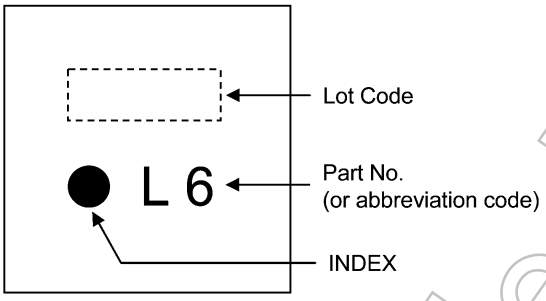


Fig. 5.1 Marking

6. Block Diagram

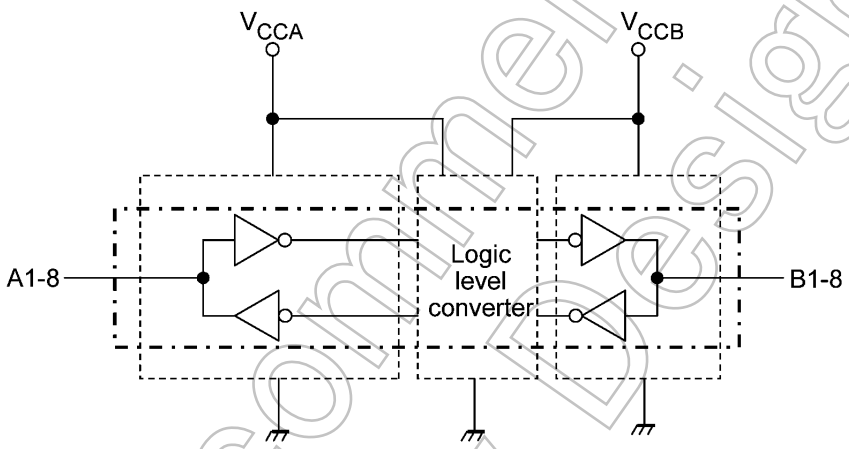


Fig. 6.1 Block Diagram

7. Internal Equivalent Circuit

The TC7LX1108WBG does not have a control signal that controls the direction of data flow between A and B. In a DC state, the output circuit holds either High or Low level, but since it is designed to have a weak drive strength (with a typical output resistance of 5.5 kΩ), an overdrive signal from the external driver can change the direction of data flow.

The output one-shot circuits detect either a rising or falling edge on the A or B port. During the rise time, the output one-shot circuit associated with the PMOS transistors turns it on for a certain period to speed up a transition from Low to High. Likewise, during the fall time, the output one-shot circuit associated with the NMOS transistors turns it on to speed up a transition from High to Low.

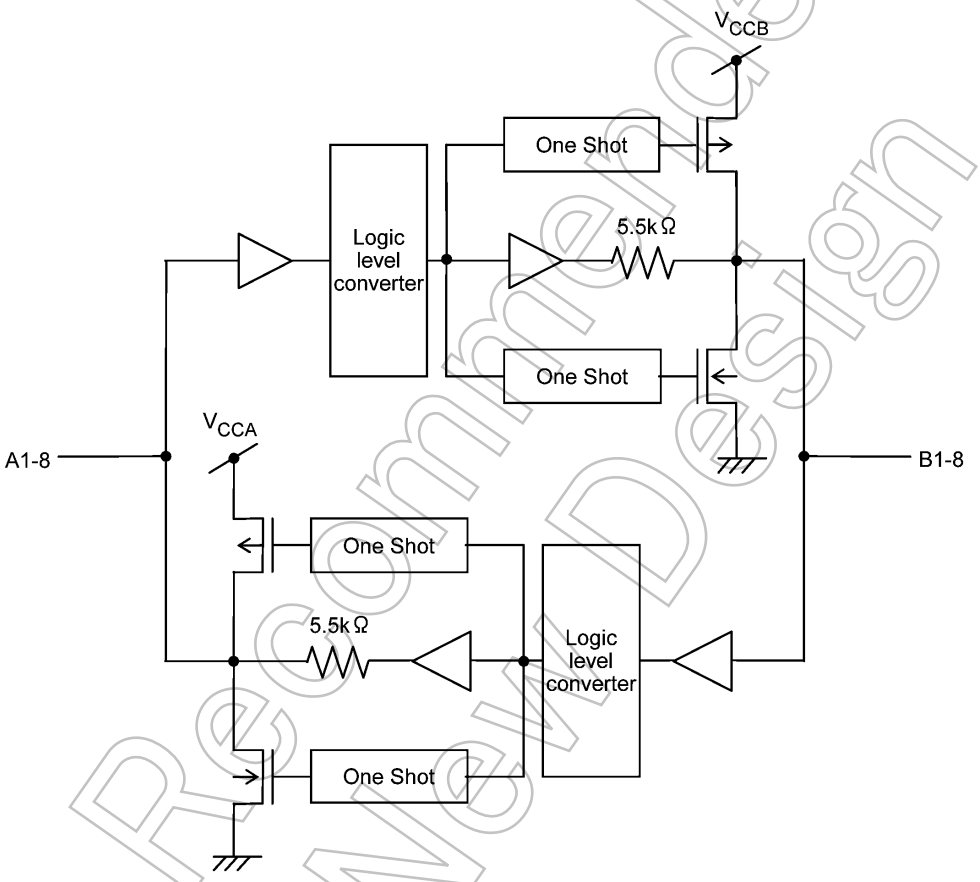


Fig. 7.1 Internal Equivalent Circuit

8. Principle of Operation

8.1. Truth Table

Input OE	Function
H	A port = B port
L	Disconnect

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CCA}		-0.5 to 4.6	V
	V_{CCB}		-0.5 to 4.6	
Input voltage (OE)	V_{IN}		-0.5 to 4.6	
Bus I/O voltage	$V_{I/OA}$	(Note 1)	-0.5 to 4.6	
		(Note 2)	-0.5 to V_{CCA} +0.5	
	$V_{I/OB}$	(Note 1)	-0.5 to 4.6	
		(Note 2)	-0.5 to V_{CCB} +0.5	
Input diode current	I_{IK}		-50	mA
I/O diode current	$I_{I/OK}$	(Note 3)	±50	
Output current	I_{OUTA}		±25	
	I_{OUTB}		±25	
V_{CC}/ground current per supply pin	I_{CCA}		±50	
	I_{CCB}		±50	
Power dissipation	P_D		400	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Output in OFF state.

Note 2: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 3: V_{OUT} < GND, V_{OUT} > V_{CC}

10. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V_{CCA}		—	1.2 to 3.6	V
	V_{CCB}			1.2 to 3.6	
Input voltage (OE)	V_{IN}			0 to 3.6	
Bus I/O voltage	$V_{I/OA}$	(Note 1)		0 to 3.6	
		(Note 2)		0 to V_{CCA}	
	$V_{I/OB}$	(Note 1)		0 to 3.6	
		(Note 2)		0 to V_{CCB}	
Input rise time	dt/dv		V_{IN} = 0.8 to 2.0 V, V_{CCA} = 2.5 V, V_{CCB} = 3.0 V	0 to 10	ns/V
Input fall time				0 to 10	
Operating temperature	T_{opr}		—	-40 to 85	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 1: Output in OFF state.

Note 2: High or low state

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Min	Max	Unit
High-level input voltage	V_{IHA}	OE, An	1.2	1.2 to 3.6	1.10	—	V
			1.4		1.20	—	
			1.65		1.35	—	
			2.3		1.70	—	
			3.0		2.00	—	
			3.6		2.20	—	
	V_{IHB}	Bn	1.2 to 3.6	1.2	1.10	—	
				1.4	1.20	—	
				1.65	1.35	—	
				2.3	1.70	—	
				3.0	2.00	—	
				3.6	2.20	—	
Low-level input voltage	V_{ILA}	OE, An	1.2	1.2 to 3.6	—	0.10	
			1.4		—	0.20	
			1.65		—	0.30	
			2.3		—	0.50	
			3.0		—	0.70	
			3.6		—	0.80	
	V_{ILB}	Bn	1.2 to 3.6	1.2	—	0.10	
				1.4	—	0.20	
				1.65	—	0.30	
				2.3	—	0.50	
				3.0	—	0.70	
				3.6	—	0.80	
High-level output voltage	V_{OHA}	V_{IN} = V_{IH} or V_{IL}, I_{OHA} = -20 μA	1.2 to 3.6	1.2 to 3.6	V_{CCA} -0.4	—	
	V_{OHB}	V_{IN} = V_{IH} or V_{IL}, I_{OHB} = -20 μA	1.2 to 3.6	1.2 to 3.6	V_{CCB} -0.4	—	
Low-level output voltage	V_{OLA}	V_{IN} = V_{IH} or V_{IL}, I_{OLA} = 20 μA	1.2 to 3.6	1.2 to 3.6	—	0.4	
	V_{OLB}	V_{IN} = V_{IH} or V_{IL}, I_{OLB} = 20 μA	1.2 to 3.6	1.2 to 3.6	—	0.4	
3-state output OFF-state leakage current	I_{OZA}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0 to 3.6 V	1.2 to 3.6	1.2 to 3.6	—	±2.0	μA
	I_{OZB}		1.2 to 3.6	1.2 to 3.6	—	±2.0	
Output resistance	R_{OUT}	—	1.2 to 3.6	1.2 to 3.6	3.85	7.15	kΩ
Input leakage current	I_{IN}	V_{IN} (OE) = 0 to 3.6 V	1.2 to 3.6	1.2 to 3.6	—	±1.0	μA
Power-OFF leakage current	I_{OFF}	V_{IN}, V_{OUT} = 0 to 3.6 V	0	0	—	2.0	
Quiescent supply current	I_{CCA}	V_{INA} = V_{CCA} or GND V_{INB} = V_{CCB} or GND	1.2 to 3.6	1.2 to 3.6	—	5.0	
	I_{CCB}		1.2 to 3.6	1.2 to 3.6	—	5.0	
	I_{CCA}	$V_{CCA} \leq (V_{IN}, V_{OUT}) \leq 3.6$ V	1.2 to 3.6	1.2 to 3.6	—	±5.0	
	I_{CCB}	$V_{CCB} \leq (V_{IN}, V_{OUT}) \leq 3.6$ V	1.2 to 3.6	1.2 to 3.6	—	±5.0	

11.2. AC Characteristics

11.2.1. V_{CCA} = 3.3 ± 0.3 V
(Unless otherwise specified, T_a = -40 to 85°C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	10.7	ns
			1.5 ± 0.1	1.0	6.2	
			1.8 ± 0.15	1.0	4.8	
			2.5 ± 0.2	1.0	3.6	
			3.3 ± 0.3	1.0	3.2	
3-state output enable time (OE → An)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	74.3	
			1.5 ± 0.1	1.0	69.0	
			1.8 ± 0.15	1.0	66.6	
			2.5 ± 0.2	1.0	65.1	
			3.3 ± 0.3	1.0	63.5	
3-state output disable time (OE → An)	t_{PLZ}/t_{PHZ}		1.2	1.0	57.6	
			1.5 ± 0.1	1.0	59.1	
			1.8 ± 0.15	1.0	56.7	
			2.5 ± 0.2	1.0	56.9	
			3.3 ± 0.3	1.0	60.5	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	7.3	
			1.5 ± 0.1	1.0	4.6	
			1.8 ± 0.15	1.0	3.9	
			2.5 ± 0.2	1.0	3.2	
			3.3 ± 0.3	1.0	3.0	
3-state output enable time (OE → Bn)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	120.5	
			1.5 ± 0.1	1.0	111.8	
			1.8 ± 0.15	1.0	109.8	
			2.5 ± 0.2	1.0	112.9	
			3.3 ± 0.3	1.0	113.2	
3-state output disable time (OE → Bn)	t_{PLZ}/t_{PHZ}		1.2	1.0	112.5	
			1.5 ± 0.1	1.0	98.4	
			1.8 ± 0.15	1.0	103.0	
			2.5 ± 0.2	1.0	95.0	
			3.3 ± 0.3	1.0	121.7	
Output skew (Note 1)	t_{osLH}/t_{osHL}	—	1.2	—	0.5	
			1.5 ± 0.1	—	0.5	
			1.8 ± 0.15	—	0.5	
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.2.2. V_{CCA} = 2.5 ± 0.2 V
(Unless otherwise specified, T_a = -40 to 85°C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	10.5	ns
			1.5 ± 0.1	1.0	6.2	
			1.8 ± 0.15	1.0	4.9	
			2.5 ± 0.2	1.0	3.7	
			3.3 ± 0.3	1.0	3.3	
3-state output enable time (OE → An)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	74.7	
			1.5 ± 0.1	1.0	68.8	
			1.8 ± 0.15	1.0	66.6	
			2.5 ± 0.2	1.0	64.6	
			3.3 ± 0.3	1.0	62.1	
3-state output disable time (OE → An)	t_{PLZ}/t_{PHZ}		1.2	1.0	51.0	
			1.5 ± 0.1	1.0	52.0	
			1.8 ± 0.15	1.0	50.7	
			2.5 ± 0.2	1.0	49.8	
			3.3 ± 0.3	1.0	50.0	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	7.5	
			1.5 ± 0.1	1.0	5.0	
			1.8 ± 0.15	1.0	4.3	
			2.5 ± 0.2	1.0	3.7	
			3.3 ± 0.3	1.0	3.5	
3-state output enable time (OE → Bn)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	119.3	
			1.5 ± 0.1	1.0	112.3	
			1.8 ± 0.15	1.0	112.2	
			2.5 ± 0.2	1.0	114.1	
			3.3 ± 0.3	1.0	114.1	
3-state output disable time (OE → Bn)	t_{PLZ}/t_{PHZ}		1.2	1.0	105.9	
			1.5 ± 0.1	1.0	100.0	
			1.8 ± 0.15	1.0	112.5	
			2.5 ± 0.2	1.0	94.8	
			3.3 ± 0.3	1.0	116.7	
Output skew (Note 1)	t_{osLH}/t_{osHL}	—	1.2	—	0.5	
			1.5 ± 0.1	—	0.5	
			1.8 ± 0.15	—	0.5	
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.2.3. V_{CCA} = 1.8 ± 0.15 V
(Unless otherwise specified, T_a = -40 to 85°C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	10.7	ns
			1.5 ± 0.1	1.0	6.4	
			1.8 ± 0.15	1.0	5.1	
			2.5 ± 0.2	1.0	4.0	
			3.3 ± 0.3	1.0	3.6	
3-state output enable time (OE → An)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	77.7	
			1.5 ± 0.1	1.0	72.7	
			1.8 ± 0.15	1.0	67.8	
			2.5 ± 0.2	1.0	66.0	
			3.3 ± 0.3	1.0	68.5	
3-state output disable time (OE → An)	t_{PLZ}/t_{PHZ}		1.2	1.0	64.1	
			1.5 ± 0.1	1.0	61.2	
			1.8 ± 0.15	1.0	64.1	
			2.5 ± 0.2	1.0	59.9	
			3.3 ± 0.3	1.0	56.9	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	8.4	
			1.5 ± 0.1	1.0	6.1	
			1.8 ± 0.15	1.0	5.4	
			2.5 ± 0.2	1.0	4.9	
			3.3 ± 0.3	1.0	4.7	
3-state output enable time (OE → Bn)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	121.5	
			1.5 ± 0.1	1.0	115.8	
			1.8 ± 0.15	1.0	116.1	
			2.5 ± 0.2	1.0	116.4	
			3.3 ± 0.3	1.0	116.3	
3-state output disable time (OE → Bn)	t_{PLZ}/t_{PHZ}		1.2	1.0	115.8	
			1.5 ± 0.1	1.0	99.3	
			1.8 ± 0.15	1.0	111.6	
			2.5 ± 0.2	1.0	95.4	
			3.3 ± 0.3	1.0	122.3	
Output skew (Note 1)	t_{osLH}/t_{osHL}	—	1.2	—	0.5	
			1.5 ± 0.1	—	0.5	
			1.8 ± 0.15	—	0.5	
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.2.4. V_{CCA} = 1.5 ± 0.1 V
(Unless otherwise specified, T_a = -40 to 85°C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	10.9	ns
			1.5 ± 0.1	1.0	6.8	
			1.8 ± 0.15	1.0	5.5	
			2.5 ± 0.2	1.0	4.4	
			3.3 ± 0.3	1.0	4.0	
3-state output enable time (OE → An)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	81.5	
			1.5 ± 0.1	1.0	73.8	
			1.8 ± 0.15	1.0	72.6	
			2.5 ± 0.2	1.0	68.7	
			3.3 ± 0.3	1.0	67.4	
3-state output disable time (OE → An)	t_{PLZ}/t_{PHZ}		1.2	1.0	66.3	
			1.5 ± 0.1	1.0	60.5	
			1.8 ± 0.15	1.0	56.8	
			2.5 ± 0.2	1.0	57.2	
			3.3 ± 0.3	1.0	57.4	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	9.7	
			1.5 ± 0.1	1.0	7.6	
			1.8 ± 0.15	1.0	6.9	
			2.5 ± 0.2	1.0	6.4	
			3.3 ± 0.3	1.0	6.2	
3-state output enable time (OE → Bn)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	125.6	
			1.5 ± 0.1	1.0	120.4	
			1.8 ± 0.15	1.0	119.9	
			2.5 ± 0.2	1.0	122.6	
			3.3 ± 0.3	1.0	119.8	
3-state output disable time (OE → Bn)	t_{PLZ}/t_{PHZ}		1.2	1.0	105.7	
			1.5 ± 0.1	1.0	97.7	
			1.8 ± 0.15	1.0	111.3	
			2.5 ± 0.2	1.0	95.8	
			3.3 ± 0.3	1.0	127.9	
Output skew (Note 1)	t_{osLH}/t_{osHL}	—	1.2	—	0.5	
			1.5 ± 0.1	—	0.5	
			1.8 ± 0.15	—	0.5	
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

11.2.5. V_{CCA} = 1.2 V
(Unless otherwise specified, T_a = -40 to 85°C, Input: $t_r = t_f$ = 2.0 ns)

Characteristics	Symbol	Test Condition	V_{CCB} (V)	Min	Max	Unit
Propagation delay time (Bn → An)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	11.8	ns
			1.5 ± 0.1	1.0	7.9	
			1.8 ± 0.15	1.0	6.4	
			2.5 ± 0.2	1.0	5.3	
			3.3 ± 0.3	1.0	5.0	
3-state output enable time (OE → An)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	93.6	
			1.5 ± 0.1	1.0	84.3	
			1.8 ± 0.15	1.0	80.8	
			2.5 ± 0.2	1.0	79.2	
			3.3 ± 0.3	1.0	79.7	
3-state output disable time (OE → An)	t_{PLZ}/t_{PHZ}		1.2	1.0	79.5	
			1.5 ± 0.1	1.0	72.7	
			1.8 ± 0.15	1.0	69.7	
			2.5 ± 0.2	1.0	82.7	
			3.3 ± 0.3	1.0	73.1	
Propagation delay time (An → Bn)	t_{PLH}/t_{PHL}	Fig. 11.2.1, Fig. 11.2.3, Table 11.2.2	1.2	1.0	13.3	
			1.5 ± 0.1	1.0	12.0	
			1.8 ± 0.15	1.0	11.3	
			2.5 ± 0.2	1.0	10.9	
			3.3 ± 0.3	1.0	10.9	
3-state output enable time (OE → Bn)	t_{PZL}/t_{PZH}	Fig. 11.2.2, Fig. 11.2.4, Table 11.2.1, Table 11.2.2	1.2	1.0	136.7	
			1.5 ± 0.1	1.0	128.4	
			1.8 ± 0.15	1.0	126.1	
			2.5 ± 0.2	1.0	125.0	
			3.3 ± 0.3	1.0	125.0	
3-state output disable time (OE → Bn)	t_{PLZ}/t_{PHZ}		1.2	1.0	114.9	
			1.5 ± 0.1	1.0	100.6	
			1.8 ± 0.15	1.0	109.6	
			2.5 ± 0.2	1.0	97.1	
			3.3 ± 0.3	1.0	127.5	
Output skew (Note 1)	t_{osLH}/t_{osHL}	—	1.2	—	0.5	
			1.5 ± 0.1	—	0.5	
			1.8 ± 0.15	—	0.5	
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: Parameter guaranteed by design.
($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.3. Timing Requirements

11.3.1. V_{CCA} = 3.3 ± 0.3 V (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CCB}	Min	Max	Unit
Pulse duration (data input)	t_w	Fig. 11.2.1	1.2	50	—	ns
			1.5 ± 0.1	17	—	
			1.8 ± 0.15	12	—	
			2.5 ± 0.2	7	—	
			3.3 ± 0.3	5	—	
Data rate	f_D	—	1.2	—	20	Mbps
			1.5 ± 0.1	—	60	
			1.8 ± 0.15	—	90	
			2.5 ± 0.2	—	150	
			3.3 ± 0.3	—	200	

11.3.2. V_{CCA} = 2.5 ± 0.2 V (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CCB}	Min	Max	Unit
Pulse duration (data input)	t_w	Fig. 11.2.1	1.2	50	—	ns
			1.5 ± 0.1	17	—	
			1.8 ± 0.15	12	—	
			2.5 ± 0.2	7	—	
			3.3 ± 0.3	7	—	
Data rate	f_D	—	1.2	—	20	Mbps
			1.5 ± 0.1	—	60	
			1.8 ± 0.15	—	90	
			2.5 ± 0.2	—	150	
			3.3 ± 0.3	—	150	

11.3.3. V_{CCA} = 1.8 ± 0.15 V (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CCB}	Min	Max	Unit
Pulse duration (data input)	t_w	Fig. 11.2.1	1.2	50	—	ns
			1.5 ± 0.1	20	—	
			1.8 ± 0.15	13	—	
			2.5 ± 0.2	12	—	
			3.3 ± 0.3	12	—	
Data rate	f_D	—	1.2	—	20	Mbps
			1.5 ± 0.1	—	50	
			1.8 ± 0.15	—	80	
			2.5 ± 0.2	—	90	
			3.3 ± 0.3	—	90	

11.3.4. V_{CCA} = 1.5 ± 0.1 V (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CCB}	Min	Max	Unit
Pulse duration (data input)	t_w	Fig. 11.2.1	1.2	50	—	ns
			1.5 ± 0.1	20	—	
			1.8 ± 0.15	20	—	
			2.5 ± 0.2	17	—	
			3.3 ± 0.3	17	—	
Data rate	f_D	—	1.2	—	20	Mbps
			1.5 ± 0.1	—	50	
			1.8 ± 0.15	—	50	
			2.5 ± 0.2	—	60	
			3.3 ± 0.3	—	60	

11.3.5. V_{CCA} = 1.2 V (Unless otherwise specified, T_a = -40 to 85°C)

Characteristics	Symbol	Test Condition	V_{CCB}	Min	Max	Unit
Pulse duration (data input)	t_w	Fig. 11.2.1	1.2	50	—	ns
			1.5 ± 0.1	50	—	
			1.8 ± 0.15	50	—	
			2.5 ± 0.2	50	—	
			3.3 ± 0.3	50	—	
Data rate	f_D	—	1.2	—	20	Mbps
			1.5 ± 0.1	—	20	
			1.8 ± 0.15	—	20	
			2.5 ± 0.2	—	20	
			3.3 ± 0.3	—	20	

11.4. Capacitive Characteristics (Unless otherwise specified, T_a = 25°C)

Characteristics	Symbol	Test Condition	V_{CCA} (V)	V_{CCB} (V)	Typ.	Unit
Input capacitance	C_{IN}	OE	2.5	3.3	8	pF
Bus I/O capacitance	$C_{I/O}$	An, Bn			8	
Power dissipation capacitance (Note 1)	C_{PDA}	OE = Low (A → B)			0.01	
		OE = Low (B → A)			0.01	
		OE = High (A → B)			14	
		OE = High (B → A)			20	
	C_{PDB}	OE = Low (A → B)			0.01	
		OE = Low (B → A)			0.01	
		OE = High (A → B)			29	
		OE = High (B → A)			29	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation.
$I_{CC}(opr) = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per bit)

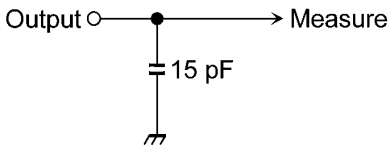


Fig. 11.2.1 AC Test Circuit

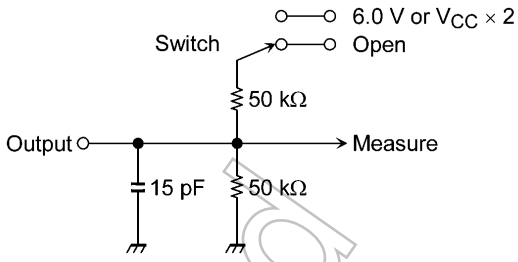


Fig. 11.2.2 AC Test Circuit

Table 11.2.1 Parameter for AC Test Circuit

Parameter	Switch	Test Condition
t_{PLZ}, t_{PZL}	6.0 V	V_{CC} = 3.3 ± 0.3 V
	V_{CC} × 2	V_{CC} = 2.5 ± 0.2 V
		V_{CC} = 1.8 ± 0.15 V
		V_{CC} = 1.5 ± 0.1 V
		V_{CC} = 1.2 V
t_{PHZ}, t_{PZH}	OPEN	—

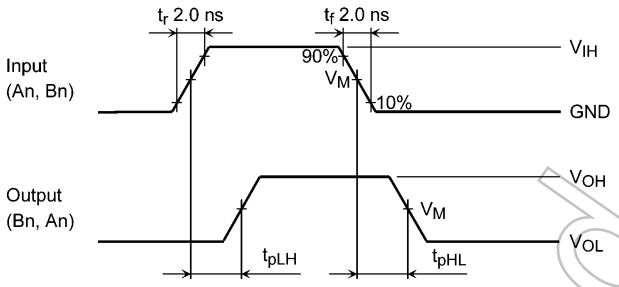


Fig. 11.2.3 AC Waveform of t_{PLH}, t_{PHL}

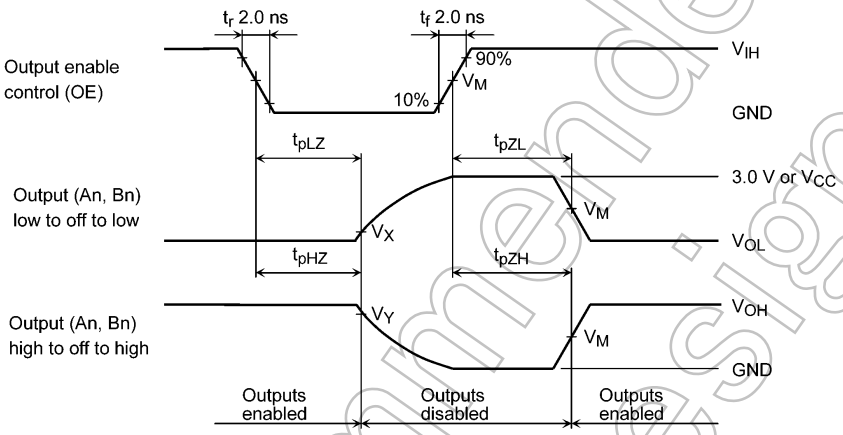


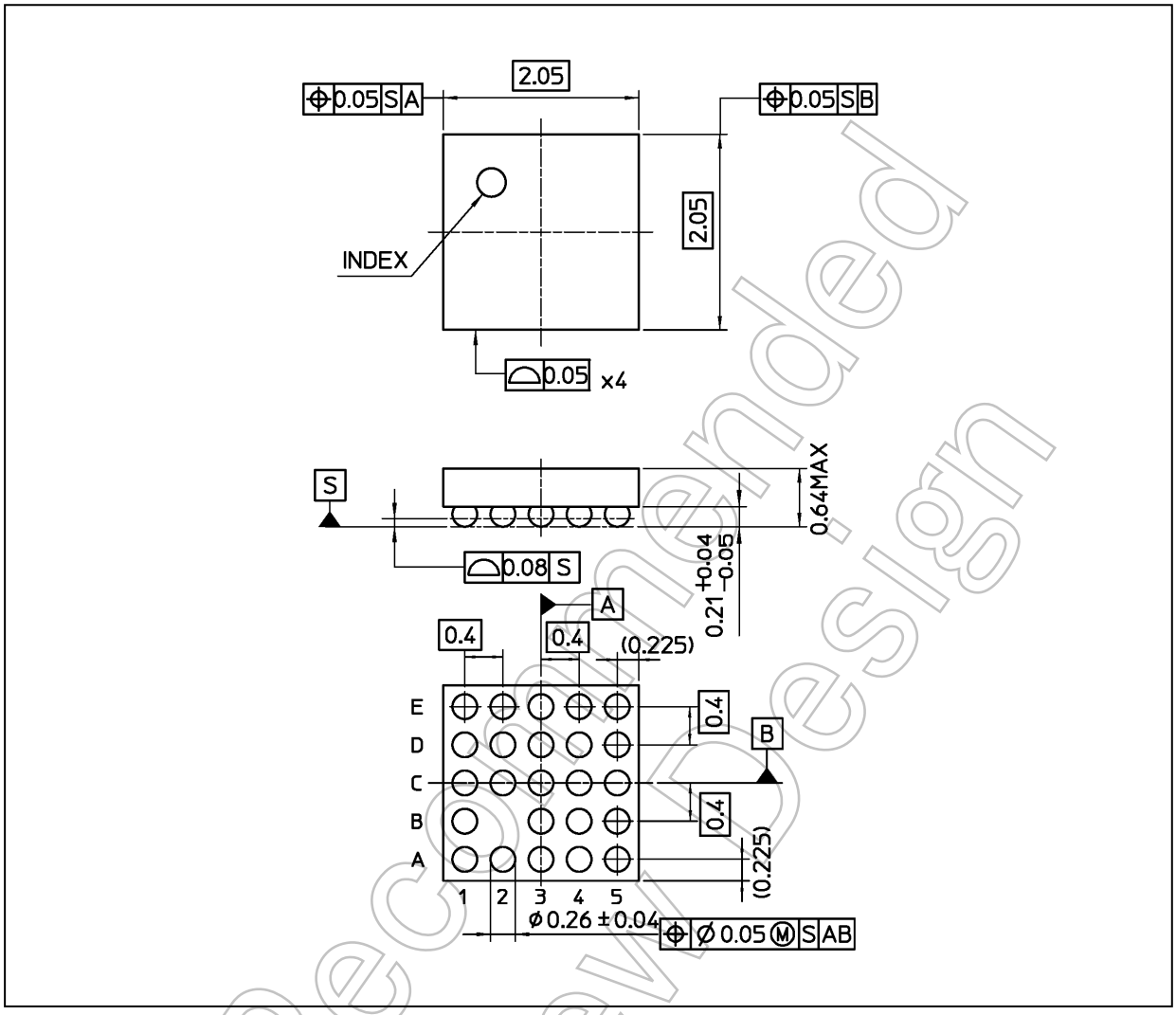
Fig. 11.2.4 AC Waveform of t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}

Table 11.2.2 AC Waveform Symbols

V_{CC}	Symbol	Value
3.3 ± 0.3 V	V_{IH}	2.7 V
	V_M	1.5 V
	V_X	V_{OL} + 0.3 V
	V_Y	V_{OH} - 0.3 V
2.5 ± 0.2 V 1.8 ± 0.15 V	V_{IH}	V_{CC}
	V_M	V_{CC}/2
	V_X	V_{OL} + 0.15 V
	V_Y	V_{OH} - 0.15 V
1.5 ± 0.1 V 1.2 V	V_{IH}	V_{CC}
	V_M	V_{CC}/2
	V_X	V_{OL} + 0.1 V
	V_Y	V_{OH} - 0.1 V

Package Dimensions

Unit: mm



This resins used in this product include no flame retardants.

Weight: 0.006 g (typ.)

Package Name(s)
TOSHIBA: S-UFBGA24-0303-0.40A01
Nickname: WCSP24C

RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- Product is intended for use in general electronics applications (e.g., computers, personal equipment, office equipment, measuring equipment, industrial robots and home electronics appliances) or for specific applications as expressly stated in this document. Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact ("Unintended Use"). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for Unintended Use unless specifically permitted in this document.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. TOSHIBA assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.

单击下面可查看定价，库存，交付和生命周期等信息

>>Toshiba(东芝)