TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(U-MOSⅥ)

SSM6J502NU

Power Management Switch Applications

- 1.5V drive
- Low ON-resistance: $R_{DS(ON)}$ = 60.5 mΩ (max) (@V_{GS} = -1.5 V)
  $R_{DS(ON)}$ = 38.4 mΩ (max) (@V_{GS} = -1.8 V)
  $R_{DS(ON)}$ = 28.3 mΩ (max) (@V_{GS} = -2.5 V)
  $R_{DS(ON)}$ = 23.1 mΩ (max) (@V_{GS} = -4.5 V)

Absolute Maximum Ratings (Ta = 25°C)

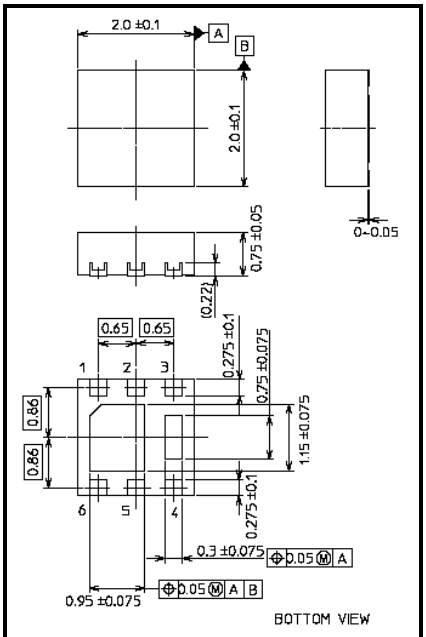
Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	−20	V
Gate-Source voltage		V_{GSS}	±8	V
Drain current	DC	I_D	−6	A
	Pulse	I_{DP} (Note 1)	−24	
Power dissipation		P_D(Note 2)	1	W
		t ≤ 10s	2	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150℃

Note 2: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Unit: mm

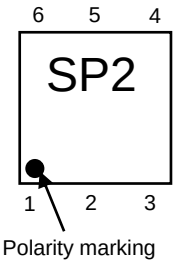


1,2,5,6: Drain
3: Gate
4: Source

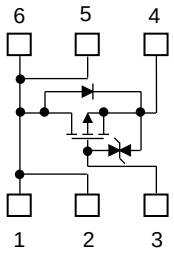
UDFN6B	
JEDEC	—
JEITA	—
TOSHIBA	2-2AA1A

Weight: 8.5 mg (typ.)

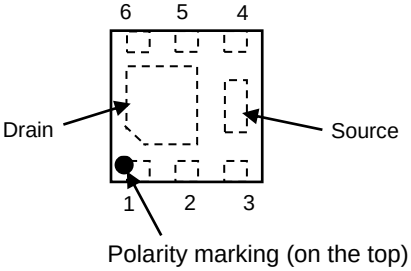
Marking(Top View)



Equivalent Circuit(Top View)



Pin Condition(Top View)



*Electrodes : on the bottom

Start of commercial production
2010-11

Electrical Characteristics (Ta = 25°C)

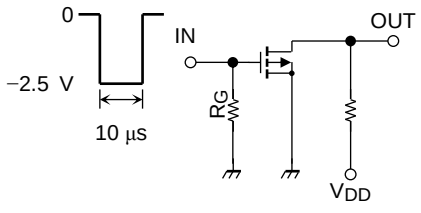
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = -1 mA, V_{GS} = 0 V	-20	—	—	V
		$V_{(BR)\ DSX}$	I_D = -1 mA, V_{GS} = 5 V (Note 4)	-15	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	—	—	-1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = -3 V, I_D = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -2.0 A (Note 3)	8.8	17.5	—	S
Drain–source ON-resistance		$R_{DS\ (ON)}$	I_D = -4.0 A, V_{GS} = -4.5 V (Note 3)	—	18.2	23.1	mΩ
			I_D = -4.0 A, V_{GS} = -2.5 V (Note 3)	—	21.5	28.3	
			I_D = -2.5 A, V_{GS} = -1.8 V (Note 3)	—	26.1	38.4	
			I_D = -1.5 A, V_{GS} = -1.5 V (Note 3)	—	29.7	60.5	
Input capacitance		C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	—	1800	—	pF
Output capacitance		C_{oss}		—	205	—	
Reverse transfer capacitance		C_{rss}		—	190	—	
Total Gate Charge		Q_g	V_{DD} = −10 V, I_D = −4.4 A V_{GS} = −4.5 V	—	24.8	—	nC
Gate-Source Charge		Q_{gs1}		—	0.8	—	
Gate-Drain Charge		Q_{gd}		—	6.8	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -10 V, I_D = -1.5 A, V_{GS} = 0 to -2.5 V, R_G = 4.7 Ω	—	25	—	ns
	Turn-off time	t_{off}		—	133	—	
Drain-Source forward voltage		V_{DSF}	I_D = 4 A, V_{GS} = 0 V (Note 3)	—	0.7	1.2	V

Note 3: Pulse measurement.

Note 4: If a forward bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

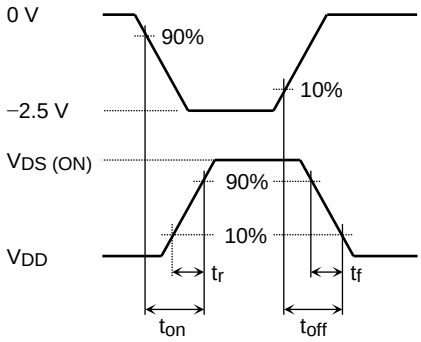
(a) Test circuit



V_{DD} = −10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common source
Ta = 25°C

(b) V_{IN}

(c) V_{out}



Precaution

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (-1 mA for the SSM6J502NU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

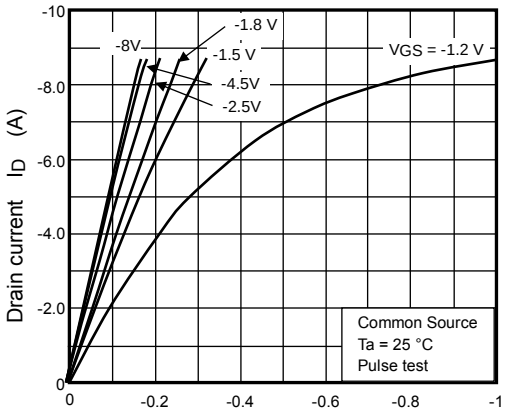
Take this into consideration when using the device.

Handling Precaution

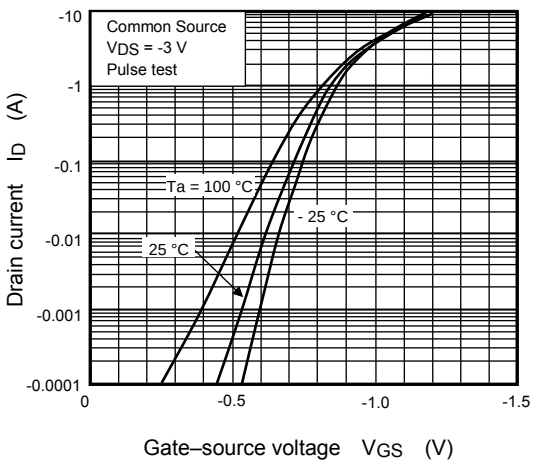
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th\ (ch-a)}$ and power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

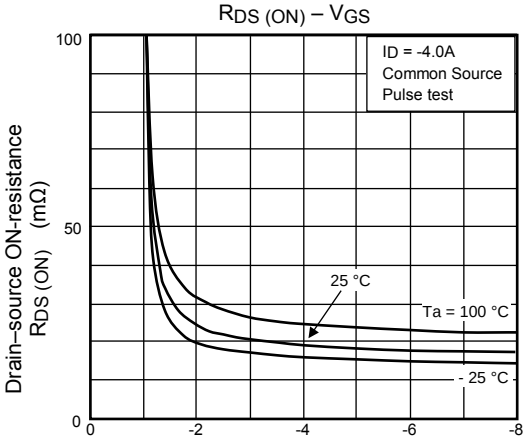
I_D – V_{DS}



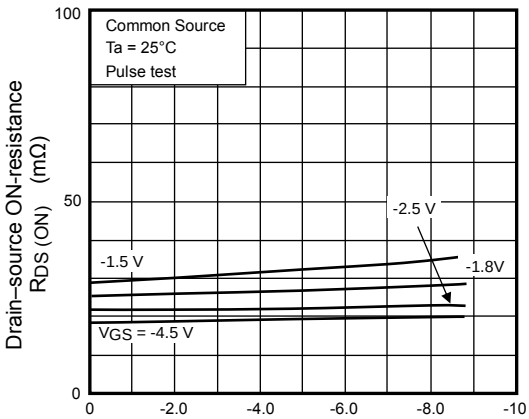
I_D – V_{GS}



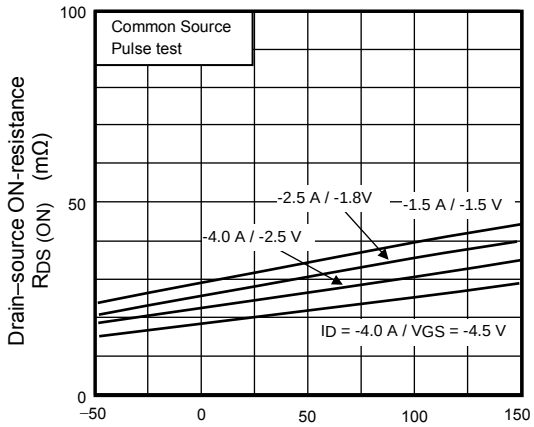
$R_{DS\ (ON)}$ – V_{GS}



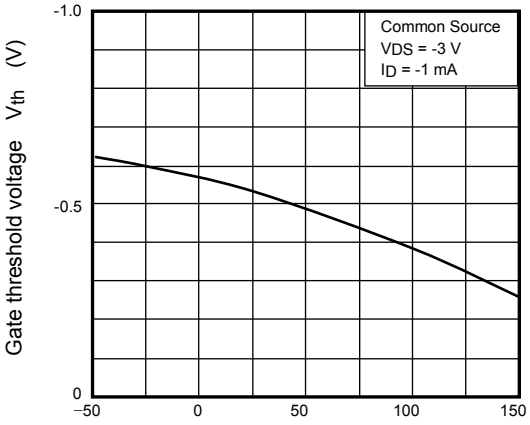
$R_{DS\ (ON)}$ – I_D

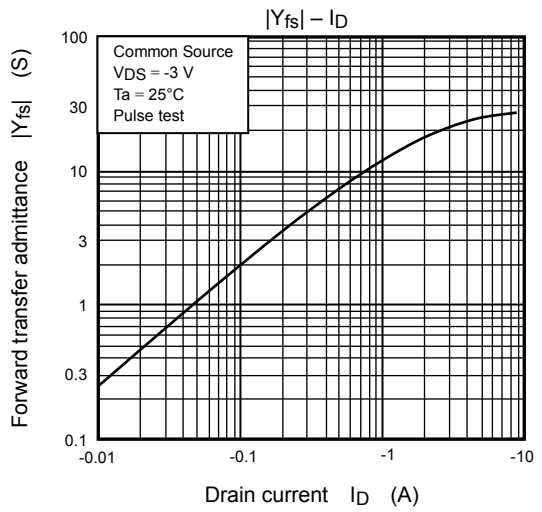


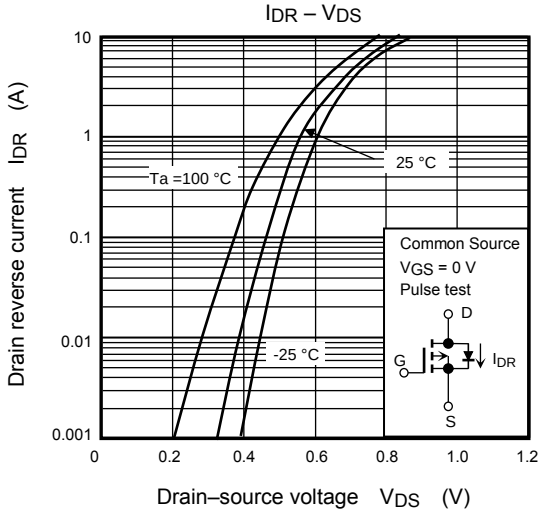
$R_{DS\ (ON)}$ – Ta

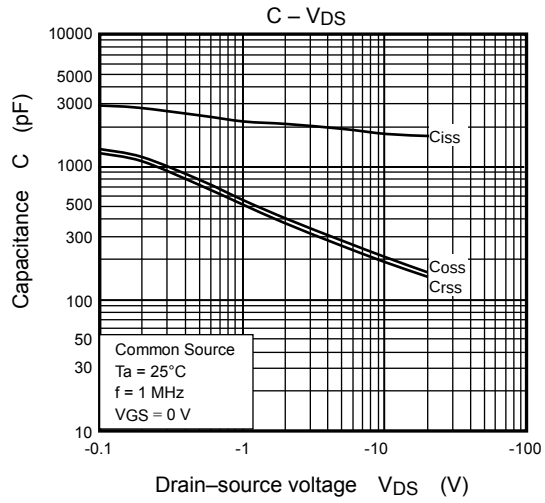


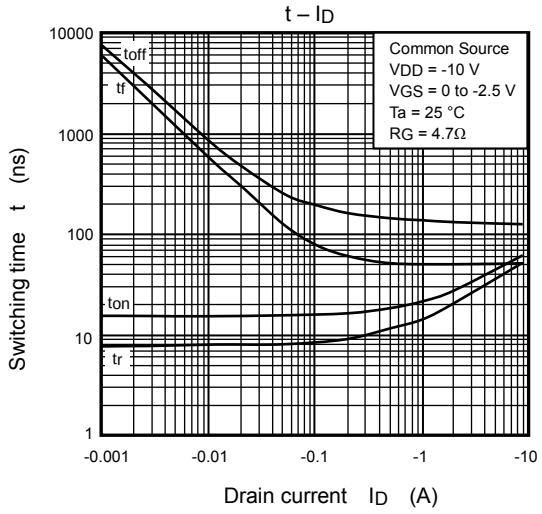
V_{th} – Ta

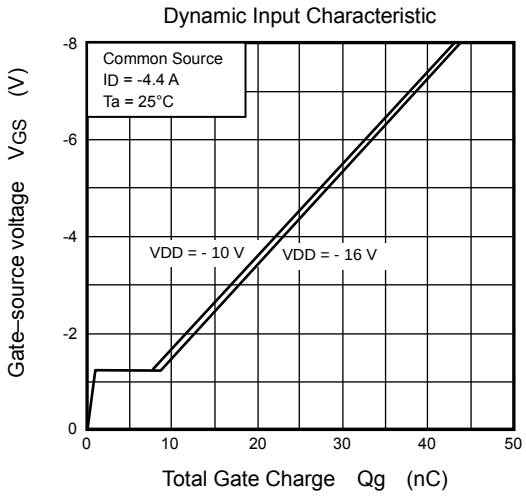




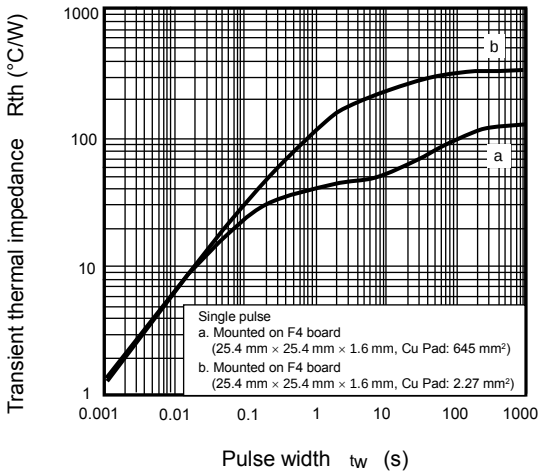




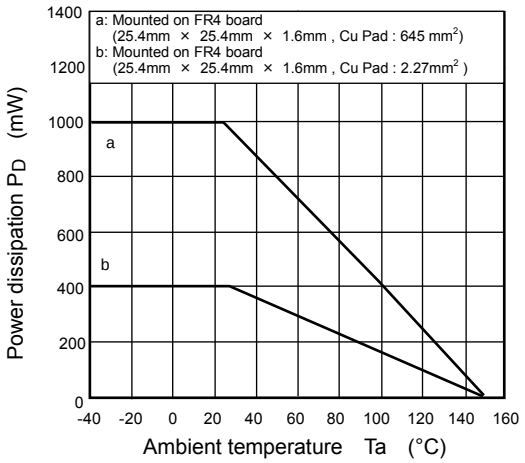




$R_{th} - T_w$



$P_D - T_a$



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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