TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

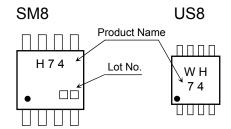
# TC7WH74FU,TC7WH74FK

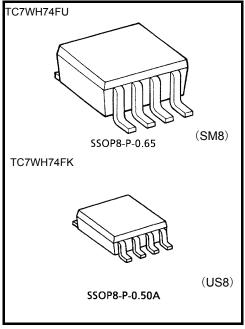
#### D-Type flip flop with preset and clear

#### **Features**

- High speed: f<sub>MAX</sub> = 170 MHz (typ.) at V<sub>CC</sub> = 5V
- Low power dissipation: I<sub>CC</sub> = 2μA (max) at Ta = 25°C
- High noise immunity: V<sub>NIH</sub> = V<sub>NIL</sub> = 28% V<sub>CC</sub> (min)
- 5.5-V tolerant inputs
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V<sub>CC</sub> = 2 to 5.5V

#### Marking



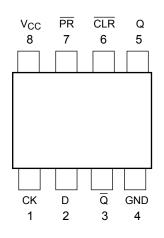


Weight SSOP8-P-0.65: 0.02 g (typ.) SSOP8-P-0.50A: 0.01 g (typ.)

#### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics	Symbol	Rating	Unit	
Supply voltage	V <sub>CC</sub>	-0.5 to 7.0	V	
DC input voltage	V <sub>IN</sub>	–0.5 to 7.0	V	
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V	
Input diode current	I <sub>IK</sub>	-20	mA	
Output diode current	lok	±20 ( Note 1)	mA	
DC output current	lout	±25	mA	
DC V <sub>CC</sub> /ground current	Icc	±50	mA	
Power dissipation	PD	300 (SM8)	mW	
Fower dissipation	۲۵	200 (US8)		
Storage temperature	T <sub>stg</sub>	-65 to 150	°C	
Lead temperature (10 s)	TL	260	°C	

### Pin Assignment (top view)



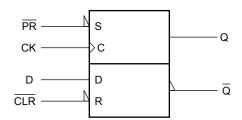
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1:  $V_{OUT} < GND$ ,  $V_{OUT} > V_{CC}$ 



# **IEC Logic Symbol**



## **Truth Table**

Inputs				Out	puts	Function	
CLR	PR	D	CK	Q	Q	Function	
L	Н	Х	Х	L	Н	Clear	
Н	L	Χ	Х	Н	L	Preset	
L	L	X	X	Н	Η	ı	
Н	Н	L	Ļ	L	Η		
Н	Н	Η	Ļη	Н	L		
Н	Н	Х	لخ	Qn	Qn	No Change	

X: Don't care

# **Operating Range**

Characteristics	Symbol	Rating	Unit	
Supply voltage	V <sub>CC</sub>	2.0 to 5.5	V	
Input voltage	V <sub>IN</sub>	0 to 5.5	V	
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V	
Operating temperature	T <sub>opr</sub>	-40 to 85	°C	
Input rise and fall time	dt/dv	0 to 100 (V <sub>CC</sub> = $3.3 \pm 0.3$ V)	ns/V	
imput rise and rail time	ui/uv	0 to 20 (V <sub>CC</sub> = $5.0 \pm 0.5$ V)		

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#### **Electrical Characteristics**

#### **DC Characteristics**

Characteristics Symb		Test Condition			Ta = 25°C				Ta = -40 to 85°C	
Characteristics	Symbol			V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	Unit
				2.0	1.5	_	_	1.5	_	
High-level input voltage	V <sub>IH</sub>		_		V <sub>CC</sub> × 0.7	_	_	V <sub>CC</sub> × 0.7	_	V
			_				0.5	_	0.5	
Low-level input voltage	V <sub>IL</sub>						V <sub>CC</sub> × 0.3	_	V <sub>CC</sub> × 0.3	V
	Voн	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		2.0	1.9	2.0	_	1.9	1	V
			I <sub>OH</sub> = -50 μA	3.0	2.9	3.0	_	2.9	1	
High-level output voltage				4.5	4.4	4.5	_	4.4	1	
			$I_{OH} = -4 \text{ mA}$	3.0	2.58		_	2.48	1	
			$I_{OH} = -8 \text{ mA}$	4.5	3.94		_	3.80	1	
				2.0		0.0	0.1	_	0.1	
			$I_{OL} = 50 \ \mu A$	3.0		0.0	0.1	_	0.1	V
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$		4.5		0.0	0.1	_	0.1	
			I <sub>OL</sub> = 4 mA	3.0			0.36	_	0.44	
			$I_{OL} = 8 \text{ mA}$	4.5			0.36	_	0.44	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5		_	±0.1	_	±1.0	μΑ
Quiescent supply current	Icc	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	_	_	2.0	_	20.0	μΑ

## TIMING REQUIREMENTS (unless otherwise specified, Input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	nbol Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit
Characteristics			V <sub>CC</sub> (V)	Limit	Limit	Onit
Minimum pulse width	t <sub>W</sub> (L)		$3.3\pm0.3$	6.0	7.0	
(CK)	t <sub>W</sub> (H)		5.0 ± 0.5	5.0	5.0	
Minimum pulse width	b(L)		$3.3\pm0.3$	6.0	7.0	
(CLR, PR)	t <sub>W</sub> (L)		5.0 ± 0.5	5.0	5.0	
Minimum setup time	4		$3.3\pm0.3$	6.0	7.0	ns
	t <sub>s</sub>		$5.0 \pm 0.5$	5.0	5.0	113
Minimum hold time	+.	t <sub>h</sub>		0.5	0.5	
	чn			0.5	0.5	
Minimum removal time	t <sub>rem</sub>		$3.3\pm0.3$	5.0	5.0	
(CLR, PR)			$5.0 \pm 0.5$	3.0	3.0	

## AC Characteristics (unless otherwise specified, Input: $t_r = t_f = 3$ ns)

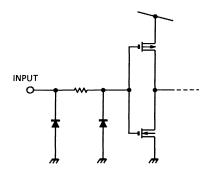
Characteristics	Symbol Test Condition				Ta = 25°C			Ta = -40~85°C		Unit
Characteristics	Symbol	rest Condition	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Тур.	Max	Min	Max	Offic
			2 2 + 0 2	15	_	6.7	11.9	1.0	14.0	
Propagation delay time	t <sub>pLH</sub>		3.3 ± 0.3	3.3 ± 0.3 50	_	9.2	15.4	1.0	17.5	ns
(CK-Q, $\overline{Q}$ )	t <sub>pHL</sub>		F 0 + 0 F	15	_	4.6	7.3	1.0	8.5	
			5.0 ± 0.5	50		6.1	9.3	1.0	10.5	
			2 2 + 0 2	15		7.6	12.3	1.0	14.5	- ns
Propagation delay time	t <sub>pLH</sub>	t <sub>pLH</sub>	$3.3 \pm 0.3$	50	_	10.1	15.8	1.0	18.0	
$(\overline{CLR}, \overline{PR}-Q, \overline{Q})$	t <sub>pHL</sub>		5.0 ± 0.5	15	_	4.8	7.7	1.0	9.0	
			J.U ± 0.5	50		6.3	9.7	1.0	11.0	
		f <sub>MAX</sub>	3.3 ± 0.3	15	80	125		70		
Maximum clock frequency	f			50	50	75		45		MHz
Maximum clock frequency	IMAX		50.05	15	130	170	_	110	_	IVITZ
		$5.0 \pm 0.5$	50	90	115	_	75	_		
Input capacitance	C <sub>IN</sub>					4	10	_	10	pF
Power dissipation capacitance	C <sub>PD</sub>	(N	lote 2)		_	22	_	_		pF

Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

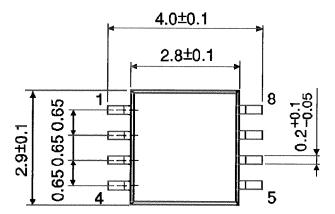
 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$ 

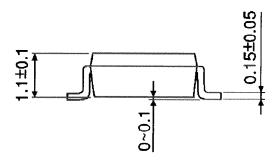
## **Input Equivalent Circuit**



## **Package Dimensions**

SSOP8-P-0.65 Unit: mm

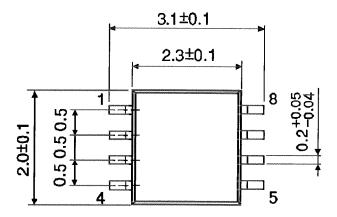


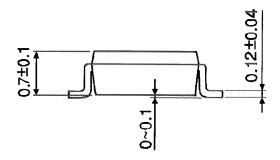


Mass: 0.02 g (typ.)

## **Package Dimensions**

SSOP8-P-0.50A Unit: mm





Mass: 0.01 g (typ.)

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