

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74ACT573P, TC74ACT573F, TC74ACT573FT

Octal D-Type Latch with 3-State Output

The TC74ACT573 is an advanced high speed CMOS OCTAL LATCH fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

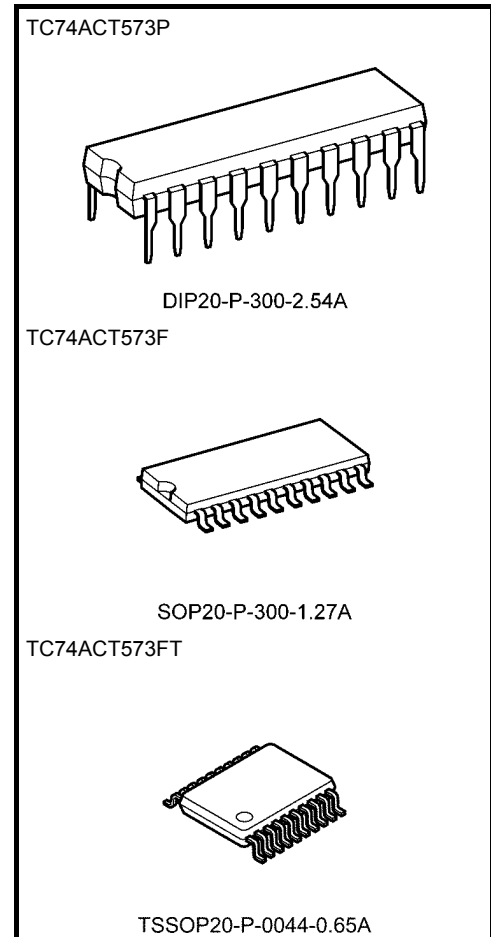
These 8-bit D-type latches are controlled by a latch enable (\overline{LE}) and a output enable input (\overline{OE}).

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $t_{pd} = 5.5 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 8 \mu\text{A (max)}$ at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs: $V_{IL} = 0.8 \text{ V (max)}$
 $V_{IH} = 2.0 \text{ V (min)}$
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24 \text{ mA (min)}$
Capability of driving 50Ω transmission lines.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74F573

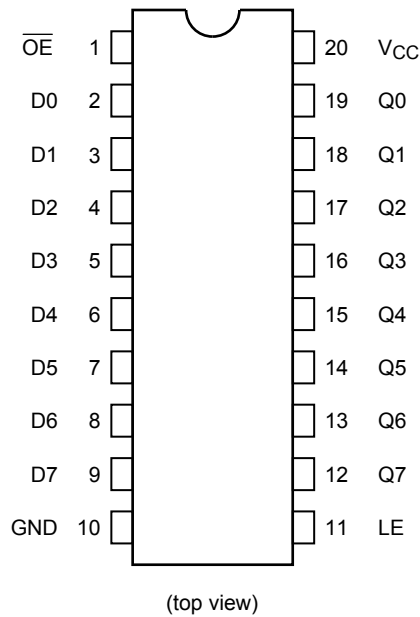


Weight

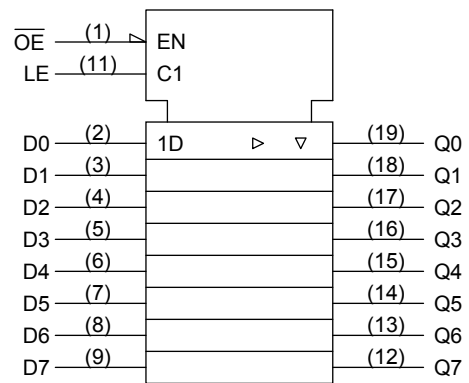
DIP20-P-300-2.54A	: 1.30 g (typ.)
SOP20-P-300-1.27A	: 0.22 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)

Start of commercial production
1988-10

Pin Assignment



IEC Logic Symbol



Truth Table

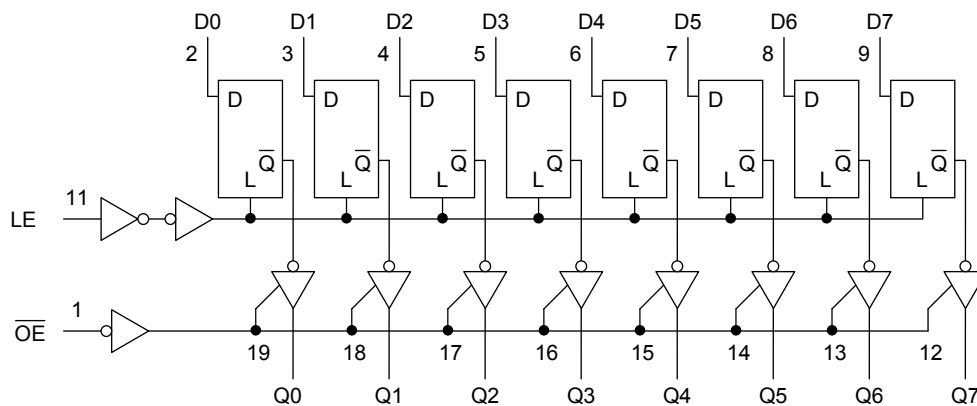
Inputs			Output
\overline{OE}	LE	D	Q
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 200	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of $T_a = -40$ to 65°C . From $T_a = 65$ to 85°C a derating factor of -10 mW/ $^{\circ}\text{C}$ should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	dt/dV	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V _{CC} (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		4.5 to 5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V _{IL}	—		4.5 to 5.5	—	—	0.8	—	0.8	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	4.5	4.4	4.5	—	4.4	—	V
			I _{OH} = -24 mA	4.5	3.94	—	—	3.80	—	
			I _{OH} = -75 mA (Note)	5.5	—	—	—	3.85	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
			I _{OL} = 75 mA (Note)	5.5	—	—	—	—	1.65	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	8.0	—	80.0	μA
	I _C	Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND		5.5	—	—	1.35	—	1.5	mA

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit	
				V _{CC} (V)	Limit		Limit
Minimum pulse width (LE)	t _w (H)	—		5.0 ± 0.5	5.0	5.0	ns
Minimum set-up time	t _s	—		5.0 ± 0.5	3.0	3.0	ns
Minimum hold time	t _h	—		5.0 ± 0.5	2.0	2.0	ns

AC Characteristics (C_L = 50 pF, R_L = 500 Ω, input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit	
			V _{CC} (V)	Min	Typ.	Max	Min		Max
Propagation delay time (LE-Q)	t _{pLH} t _{pHL}	—	5.0 ± 0.5	—	6.3	10.5	1.0	12.0	ns
Propagation delay time (Dn-Q)	t _{pLH} t _{pHL}	—	5.0 ± 0.5	—	6.2	9.6	1.0	11.0	ns
Output enable time	t _{pZL} t _{pZH}	—	5.0 ± 0.5	—	6.5	10.0	1.0	11.5	ns
Output disable time	t _{pLZ} t _{pHZ}	—	5.0 ± 0.5	—	6.5	8.8	1.0	10.0	ns
Input capacitance	C _{IN}	—	—	5	10	—	10	—	pF
Output capacitance	C _{OUT}	—	—	10	—	—	—	—	pF
Power dissipation capacitance	C _{PD}	(Note)	—	22	—	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

And the total C_{PD} when n pcs. of latch operate can be gained by the following equation:

$$C_{PD (total)} = 6 + 16 \cdot n$$

Package Dimensions

DIP20-P-300-2.54A

Unit : mm



Weight: 1.30 g (typ.)

Package Dimensions

SOP20-P-300-1.27A

Unit: mm

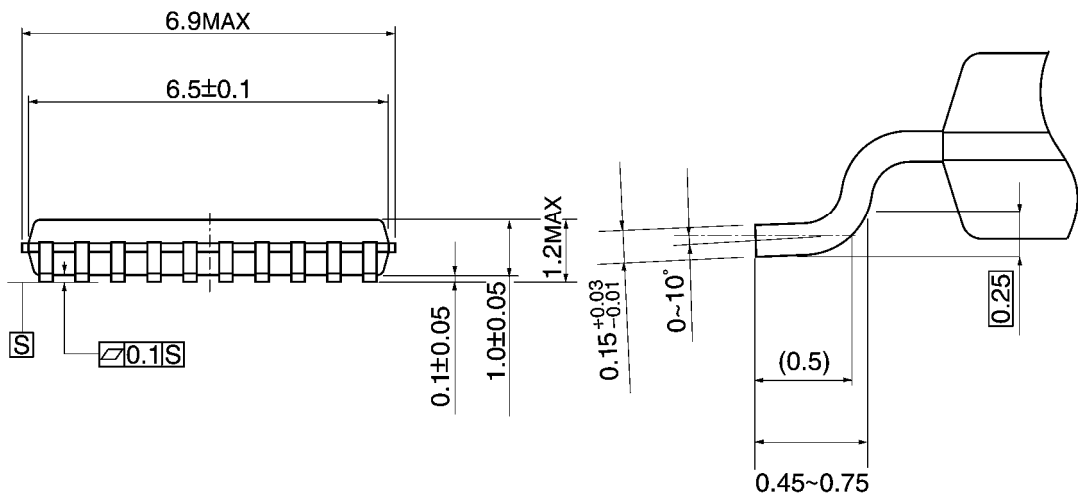
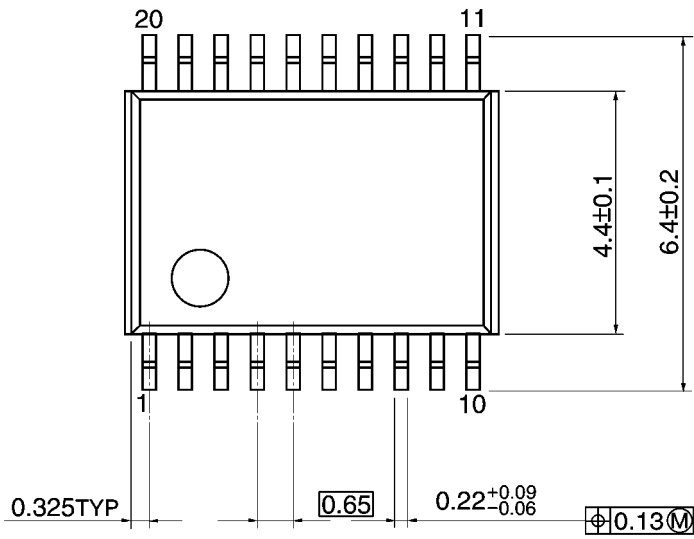


Weight: 0.22 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm



Weight: 0.08 g (typ.)

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