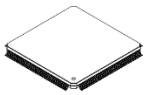
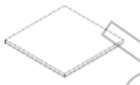
CMOS Digital Integrated Circuit Silicon Monolithic

TMPM4G Group(1)



LQFP176(20x20mm, 0.4mm pitch)
LQFP144(20x20mm, 0.5mm pitch)
LQFP128(14x14mm, 0.4mm pitch)
LQFP100(14x14mm, 0.5mm pitch)



VFBGA177(13x13mm, 0.8mm pitch)
VFBGA145(12x12mm, 0.8mm pitch)

General Description

- Arm ® Cortex®-M4(with FPU)
- Frequency: 1 to 160 MHz, Operation voltage: 2.7 to 3.6 V
- Code Flash: 512 KB to 1536 KB. Data Flash: 32KB
- Built-in High speed 12-bit AD converter and plenty of timers/serial channels

Applications

TMPM4G group(1) integrates widely used for the equipment in which high speed data procedure is required, such as OA/digital products, industrial equipment, and others.

Features

- Arm Cortex-M4(with FPU)
  - Operation frequency: 1 to 160 MHz
  - Memory Protection Unit (MPU)
- Supply voltage and power consumption
  - Operation voltage: 2.7 to 3.6 V
  - Low-power consumption operation: IDLE, STOP1, and STOP2
- Operation temperature:
  - 40 to +85℃@operation frequency 1 to 120 MHz
  - 40 to +70℃@operation frequency 1 to 160 MHz
- Internal memory
  - Code Flash: 512 KB to 1536 KB, rewritable up to 10,000 times
  - Data Flash: 32 KB, rewritable up to 100,000 times
  - Data Flash is rewritable during instruction execution
  - RAM: 128 KB to 192 KB and Backup RAM: 2 KB (all products)
- Clock
  - External high speed oscillator: 8 MHz to 20 MHz (Ceramic and Crystal)
  - External high speed clock input: 8 to 20 MHz
  - Internal high speed oscillator1 (IHOSC1):10MHz, user trimming function
  - Internal high speed oscillator2 (IHOSC2):10MHz
  - PLL: 160 MHz output
  - External low speed oscillator: 32.768 kHz
- Oscillation Frequency Detectior (OFD): Abnormal system clock detection
- Voltage Detection (LVD): 7 levels. selection between interrupts and reset outputs
- Interrupt
  - External: 12 to 16 factors. Integrate digital noise filters (DNF).
  - Internal: 91 to 124 factors
- I/O ports: 87 to 155 (Input: 4, Output: 1)
  - Enable to select Pull-up/Pull-down resistor, Open-drain
  - 5V tolerant, 3V tolerant
- On-chip debug (JTAG/SW) and NBDIF (RAM monitor)
- Trigger Selector (TRGSEL)
  - Expand trigger requests for DMA Controller, Timer counter, and others.
- DMA Controller: 3 units
  - MDMAC: 1 unit,
    DMA requests: 30 to 32 factors, internal/external triggers
  - HDMAC: 2 units,
    DMA requests: 13 to 15 factors, internal/external triggers
- External bus interface(EBIF)
  - Expandable to 64MB(Program/data)
  - External data bus(separate bug/multiplexed bun): 8/16 bit width
  - Chip select controller: 4 channels
- Asynchronous serial communication
  - UART: 3 to 6 channels, 5.0 Mbps (Max). FIFO (Transmission 8 stage and Reception 8 stage)
  - FUART: 1 or 2 channels, 2.5Mbps (Max). FIFO (Transmission 32 stage and Reception 32 stage) and IrDA 115.2Kbps (Max).
- Serial Peripheral Interface (TSPI): 5 to 9 channels
  - SIO/SPI mode, 25 Mbps (Max)
  - FIFO (Transmission 16bit x 8 stage and Reception 16bit x 8 stage)
- I²C Interface (I²C): 3 to 5 channels
  Multi master, standard mode/fast mode available
- Serial Memory Interface (SMIF): 1 channel
  - Connectable to two SPI FLASH

Start of commercial production
2019-2

- Consumer Electronics Control Circuit (CEC): 1 channel
- 8-bit DA converter (DAC): 2 channels
- 12-bit AD converter (ADC): 16 to 24 channel inputs
  - Sample and hold circuit
  - Conversion time: 1.0 µs @f_{ADCLK} = 60 MHz
- Advanced Programmable Motor Control Circuit (A-PMD): 1 channel
  - 3 phase PWM output, Synchronized with 12-bit ADC
  - Emergency stop function by external inputs (EMG0 pin and OVV0 pin)
- 32-bit Timer Event Counter (T32A)
  - 28 channels as 16-bit Timers:14 channels as 32-bit Timers
  - Interval Timer, event counter, input capture, phase difference input, PPG output, Sync Start,Trigger Start
- Interval Sensor Detection circuit (ISD): 3 units
  - 4 inputs per unit
  - Sampling 12 inputs at maximum simultaneously in Unit synchronous mode
  - Low speed oscillator (32.768 kHz) and 32-bit timer output can be used as sampling clock
- Long Term Timer (LTTMR): 1 channel
  - Interval time of 0.1µs to 6553.5µs can be set
- Real-time Clock (RTC): 1 channel
- Clock Selective Watchdog Timer (SIWDT): 1 channel
  - Clocks other than the system clock can be selected.
  - Clear window, interrupts and reset outputs
- Remote Control Signal Preprocessor (RMC): 1 to 2channels
- Supports boundary scan(BSC)

Products Lists Categorized by Functions

The product under development is contained in this table.
For the newest status of each product, Please contact your sales representative.

Table 1 TMPM4G9 (1)

Built-in Functions		TMPM4G9F15FG	TMPM4G9F10FG	TMPM4G9FEFG	TMPM4G9FDFG
Memory	Code Flash (KB)	1536	1024	768	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	192	192	128	128
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	155	155	155	155
External interrupt	INT	16	16	16	16
External bus	EBIF	Sep./Mul.	Sep./Mul.	Sep./Mul.	Sep./Mul.
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	14	14	14	14
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART(ch)	6	6	6	6
	FUART(ch)	2	2	2	2
	I^2C(ch)	5	5	5	5
	TSPI(ch)	9	9	9	9
	SMIF(ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	24	24	24	24
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor peripherals	RMC (ch)	2	2	2	2
Interval Sensor Detection peripherals	ISD (unit)	3	3	3	3
System function	LVD(ch)	1	1	1	1
	SIWDT(ch)	1	1	1	1
	OFD(ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	LQFP176 (20 mm x 20 mm, 0.4 mm pitch)			

Table 2 TMPM4G9 (2)

Built-in Functions		TMPM4G9F15XBG	TMPM4G9F10XBG	TMPM4G9FEXBG	TMPM4G9FDXBG
Memory	Code Flash (KB)	1536	1024	768	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	192	192	128	128
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	155	155	155	155
External interrupt	INT	16	16	16	16
External bus	EBIF	Sep./Mul.	Sep./Mul.	Sep./Mul.	Sep./Mul.
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	14	14	14	14
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART (ch)	6	6	6	6
	FUART (ch)	2	2	2	2
	I^2C (ch)	5	5	5	5
	TSPI (ch)	9	9	9	9
	SMIF (ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	24	24	24	24
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor peripherals	RMC (ch)	2	2	2	2
Interval Sensor Detection peripherals	ISD (unit)	3	3	3	3
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	VFBGA177 (13 mm x 13 mm, 0.8 mm pitch)			

Table 3 TMPM4G8 (1)

Built-in Functions		TMPM4G8F15FG	TMPM4G8F10FG	TMPM4G8FEFG	TMPM4G8FDFG
Memory	Code Flash (KB)	1536	1024	768	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	192	192	128	128
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	127	127	127	127
External interrupt	INT	16	16	16	16
External bus	EBIF	Sep./Mul.	Sep./Mul.	Sep./Mul.	Sep./Mul.
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	14	14	14	14
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART(ch)	5	5	5	5
	FUART(ch)	2	2	2	2
	I^2C(ch)	5	5	5	5
	TSPI(ch)	8	8	8	8
	SMIF(ch)	1	1	1	1
	CEC(ch)	1	1	1	1
Analog function	12-bit ADC(ch)	24	24	24	24
	8-bit DAC(ch)	2	2	2	2
Motor control function	A-PMD(ch)	1	1	1	1
Remote Control preprocessor peripherals	RMC(ch)	2	2	2	2
Interval Sensor Detection peripherals	ISD(unit)	2	2	2	2
System function	LVD(ch)	1	1	1	1
	SIWDT(ch)	1	1	1	1
	OFD(ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	LQFP144 (20 mm x 20 mm, 0.5 mm pitch)			

Table 4 TMPM4G8 (2)

Built-in Functions		TMPM4G8F15XBG	TMPM4G8F10XBG	TMPM4G8FEXBG	TMPM4G8FDXBG
Memory	Code Flash (KB)	1536	1024	768	512
	Data Flash (KB)	32	32	32	32
	RAM (KB)	192	192	128	128
	Backup RAM (KB)	2	2	2	2
I/O port	PORT (pin)	127	127	127	127
External interrupt	INT	16	16	16	16
External bus	EBIF	Sep./Mul.	Sep./Mul.	Sep./Mul.	Sep./Mul.
DMAC	MDMAC (ch)	32	32	32	32
	HDMAC (ch)	15	15	15	15
Timer function	T32A (ch)	14	14	14	14
	LTTMR (ch)	1	1	1	1
	RTC (ch)	1	1	1	1
Serial communication function	UART (ch)	5	5	5	5
	FUART (ch)	2	2	2	2
	I^2C (ch)	5	5	5	5
	TSPI (ch)	8	8	8	8
	SMIF (ch)	1	1	1	1
	CEC (ch)	1	1	1	1
Analog function	12-bit ADC (ch)	24	24	24	24
	8-bit DAC (ch)	2	2	2	2
Motor control function	A-PMD (ch)	1	1	1	1
Remote Control preprocessor peripherals	RMC (ch)	2	2	2	2
Interval Sensor Detection peripherals	ISD (unit)	2	2	2	2
System function	LVD (ch)	1	1	1	1
	SIWDT (ch)	1	1	1	1
	OFD (ch)	1	1	1	1
	POR	1	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	VFBGA145 (12 mm x 12 mm, 0.8 mm pitch)			

Table 5 TMPM4G7

Built-in Functions		TMPM4G7F10FG	TMPM4G7FEFG	TMPM4G7FDFG
Memory	Code Flash (KB)	1024	768	512
	Data Flash (KB)	32	32	32
	RAM (KB)	192	128	128
	Backup RAM (KB)	2	2	2
I/O port	PORT (pin)	111	111	111
External interrupt	INT	14	14	14
External bus	EBIF	Sep./Mul.	Sep./Mul.	Sep./Mul.
DMAC	MDMAC (ch)	30	30	30
	HDMAC (ch)	15	15	15
Timer function	T32A (ch)	14	14	14
	LTTMR (ch)	1	1	1
	RTC (ch)	1	1	1
Serial communication function	UART(ch)	4	4	4
	FUART(ch)	1	1	1
	I^2C (ch)	3	3	3
	TSPI (ch)	6	6	6
	SMIF (ch)	1	1	1
	CEC (ch)	1	1	1
Analog function	12-bit ADC (ch)	20	20	20
	8-bit DAC (ch)	2	2	2
Motor control function	A-PMD(ch)	1	1	1
Remote Control preprocessor peripherals	RMC(ch)	2	2	2
Interval Sensor Detection peripherals	ISD(unit)	2	2	2
System function	LVD(ch)	1	1	1
	SIWDT(ch)	1	1	1
	OFD(ch)	1	1	1
	POR	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	LQFP128 (14 mm x 14 mm, 0.4 mm pitch)		

Table 6 TMPM4G6

Built-in Functions		TMPM4G6F10FG	TMPM4G6FEFG	TMPM4G6FDFG
Memory	Code Flash (KB)	1024	768	512
	Data Flash (KB)	32	32	32
	RAM (KB)	192	128	128
	Backup RAM (KB)	2	2	2
I/O port	PORT (pin)	91	91	91
External interrupt	INT	12	12	12
External bus	EBIF	Sep./Mul.	Sep./Mul.	Sep./Mul.
DMAC	MDMAC (ch)	30	30	30
	HDMAC (ch)	13	13	13
Timer function	T32A (ch)	14	14	14
	LTTMR (ch)	1	1	1
	RTC (ch)	1	1	1
Serial communication function	UART (ch)	3	3	3
	FUART (ch)	1	1	1
	I^2C (ch)	3	3	3
	TSPI (ch)	5	5	5
	SMIF (ch)	1	1	1
	CEC (ch)	1	1	1
Analog function	12-bit ADC (ch)	16	16	16
	8-bit DAC (ch)	2	2	2
Motor control function	A-PMD (ch)	1	1	1
Remote Control preprocessor peripherals	RMC (ch)	1	1	1
Interval Sensor Detection peripherals	ISD(unit)	1	1	1
System function	LVD (ch)	1	1	1
	SIWDT (ch)	1	1	1
	OFD (ch)	1	1	1
	POR	1	1	1
Debug interface	Debug	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF	On-chip debug (JTAG/SW) TRACE(4bits) NBDIF
Package	Package type	LQFP100 (14 mm x 14 mm, 0.5 mm pitch)		

Contents

List of Figures

List of Tables

Preface

Conventions

- Numeric formats follow the rules as shown below:
  Hexadecimal: 0xABC
  Decimal: 123 or 0d123 – Only when it needs to be explicitly shown that they are decimal numbers.
  Binary: 0b111 – It is possible to omit the “0b” when the number of bit can be distinctly understood from a sentence.
- “_N” is added to the end of signal names to indicate low active signals.
- It is called “assert” that a signal moves to its active level, “deassert” to its inactive level.
- When two or more signal names are referred, they are described like as [m: n].
  Example: S[3: 0] shows four signal names S3, S2, S1 and S0 together.
- The characters surrounded by ***[ ]*** defines the register.
  Example: ***[ABCD]***
- “n” substitutes suffix number of two or more same kind of registers, fields, and bit names.
  Example: ***[XYZ1], [XYZ2], [XYZ3] → [XYZn]***
- "x" substitutes suffix number or character of units and channels in the Register List.
  In case of unit, “x” means A, B, and C . . .
  Example: ***[ADACR0], [ADBCR0], [ADCCR0] →[ADxCR0]***
  In case of channel, “x” means 0, 1, and 2 . . .
  Example: [***T32A0RUNA], [T32A1RUNA], [T32A2RUNA] → [T32AxRUNA]***
- The bit range of a register is written like as [m: n].
  Example: Bit[3: 0] expresses the range of bit 3 to 0.
- The configuration value of a register is expressed by either the hexadecimal number or the binary number.
  Example: ***[ABCD]***<EFG> = 0x01 (hexadecimal), ***[XYZn]***<VW> = 1 (binary)
- Word and Byte represent the following bit length.
  Byte: 8 bits
  Half word: 16 bits
  Word: 32 bits
  Double word: 64 bits
- Properties of each bit in a register are expressed as follows:
  R: Read only
  W: Write only
  R/W: Read and Write are possible
- Unless otherwise specified, register access supports only word access.
- The register defined as reserved must not be rewritten. Moreover, do not use the read value.
- The value read from the bit having default value of "-" is unknown.
- When a register containing both of writable bits and read-only bits is written, read-only bits should be written with their default value, In the cases that default is "-", follow the definition of each register.
- Reserved bits of the Write-only register should be written with their default value. In the cases that default is "-", follow the definition of each register.
- Do not use read-modified-write processing to the register of a definition which is different by writing and read out.

The flash memory uses the Super Flash® technology under license from Silicon Storage Technology, Inc.
Super Flash® is registered trademark of Silicon Storage Technology, Inc.

All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

Terms and Abbreviations

The following words are terms or abbreviations mainly used in this datasheet.

ADC	Analog to Digital Converter
A-PMD	Advanced Programmable Motor Control Circuit
BSC	Boundary Scan
CEC	Consumer Electronics Control
DAC	Digital to Analog Converter
DNF	Digital Noise Filter
EBIF	External Bus Interface
EHOSC	External High Speed Oscillator
ELOSC	External Low Speed Oscillator
FUART	Full Universal Asynchronous Receiver Transmitter
HDMAC	High Speed DMAC
IHOSC	Internal High Speed Oscillator
INT	Interrupt
I^2C	Inter-Integrated Circuit
ISD	Interval Sensor Detection Circuit
LTTMR	Long Term Timer
LVD	Voltage Detection Circuit
MDMAC	Multi-Function DMA Controller
NBDIF	Non Break Debug Interface
NMI	Non-Maskable Interrupt
OFD	Oscillation Frequency Detector
POR	Power On Reset Circuit
RMC	Remote Control Signal Preprocessor
RTC	Real Time Clock
SMIF	Serial Memory Interface
SIWDT	Clock Selective Watchdog Timer
TRGSEL	Trigger Selection circuit
TRM	Trimming Circuit
TSPI	Toshiba Serial Peripheral Interface
T32A	32-bit Timer Event Counter
UART	Universal Asynchronous Receiver Transmitter

1. Block Diagram

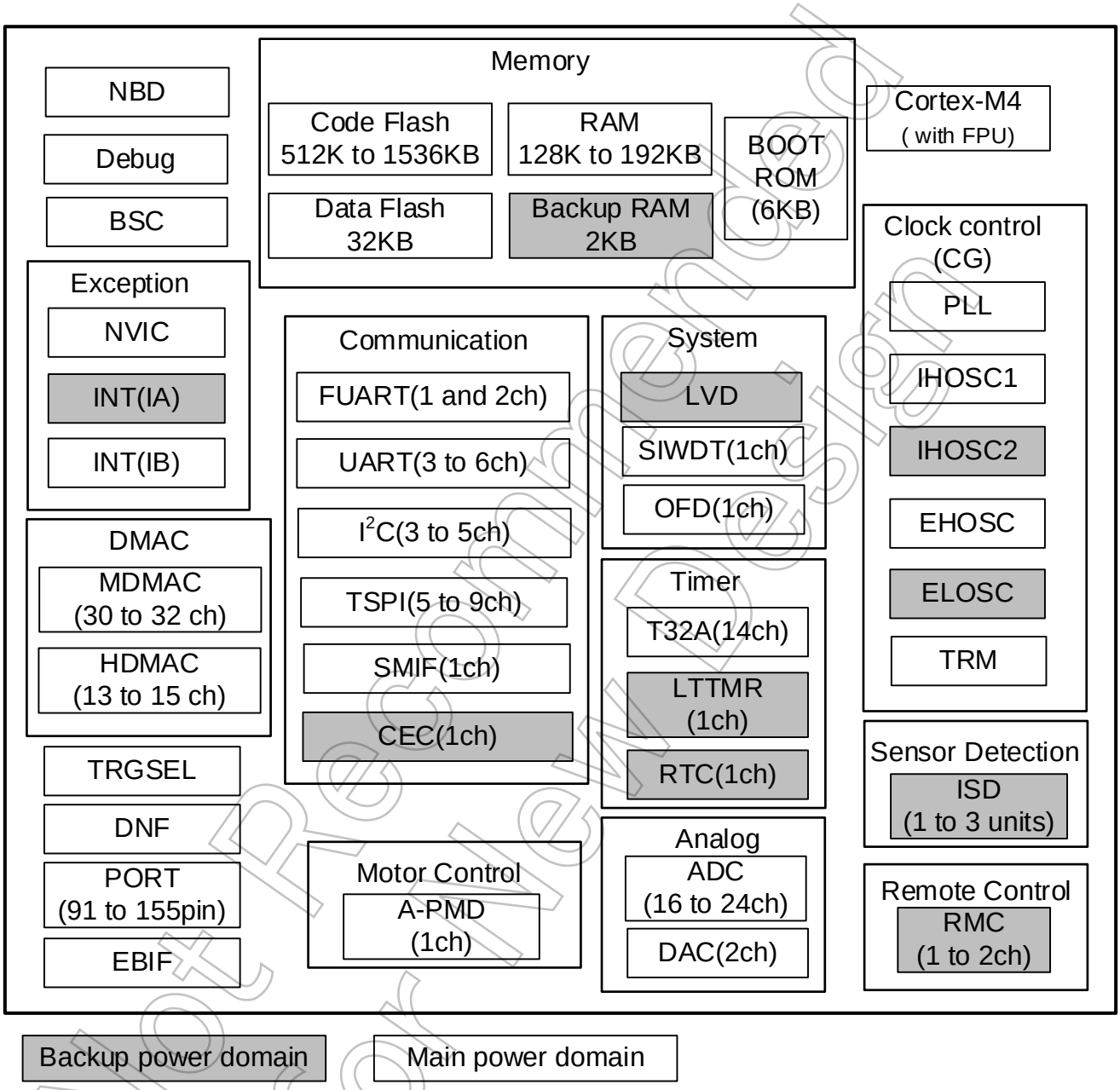
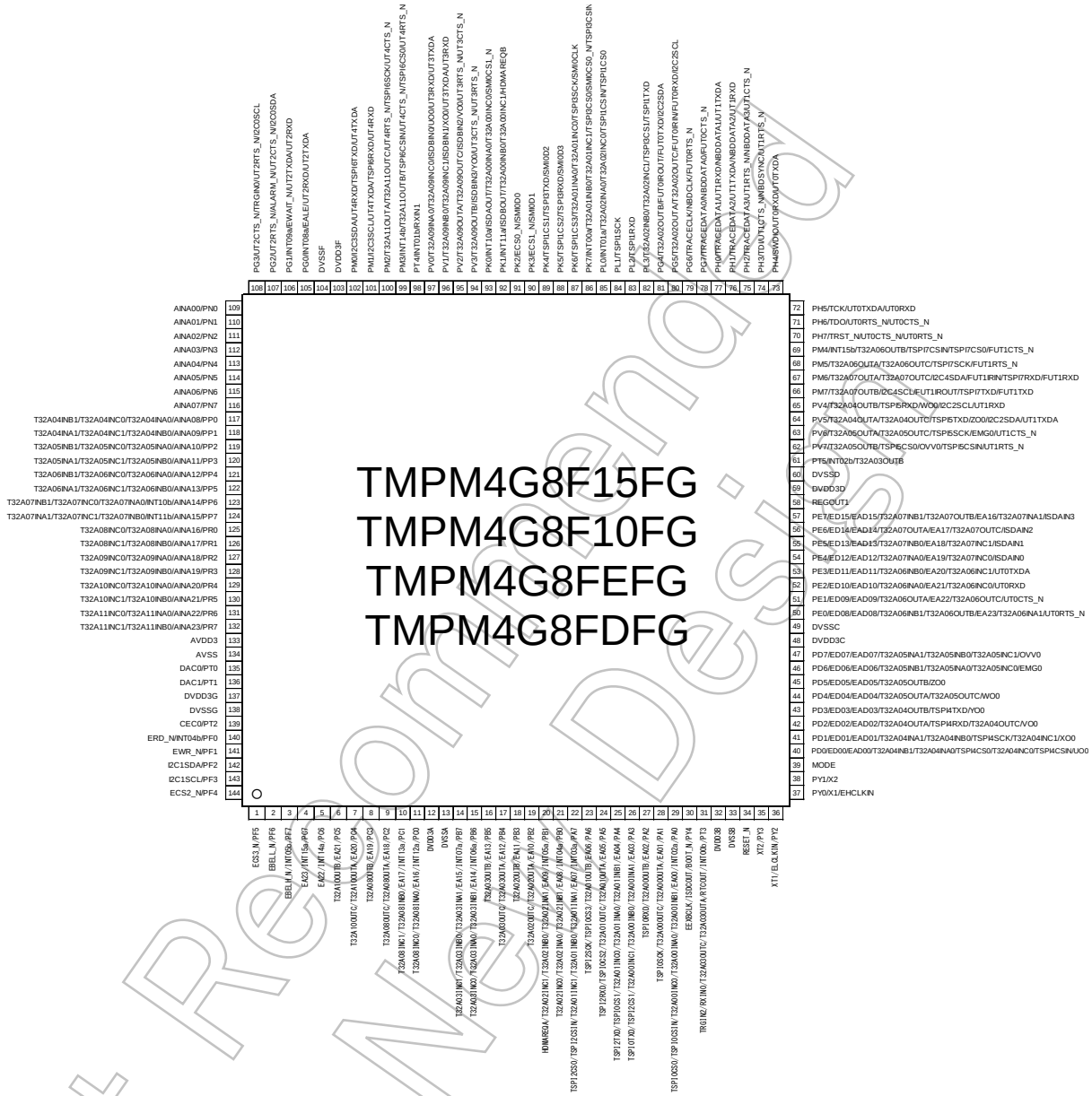


Figure 1.1 Block diagram of the TMPM4G Group(1)

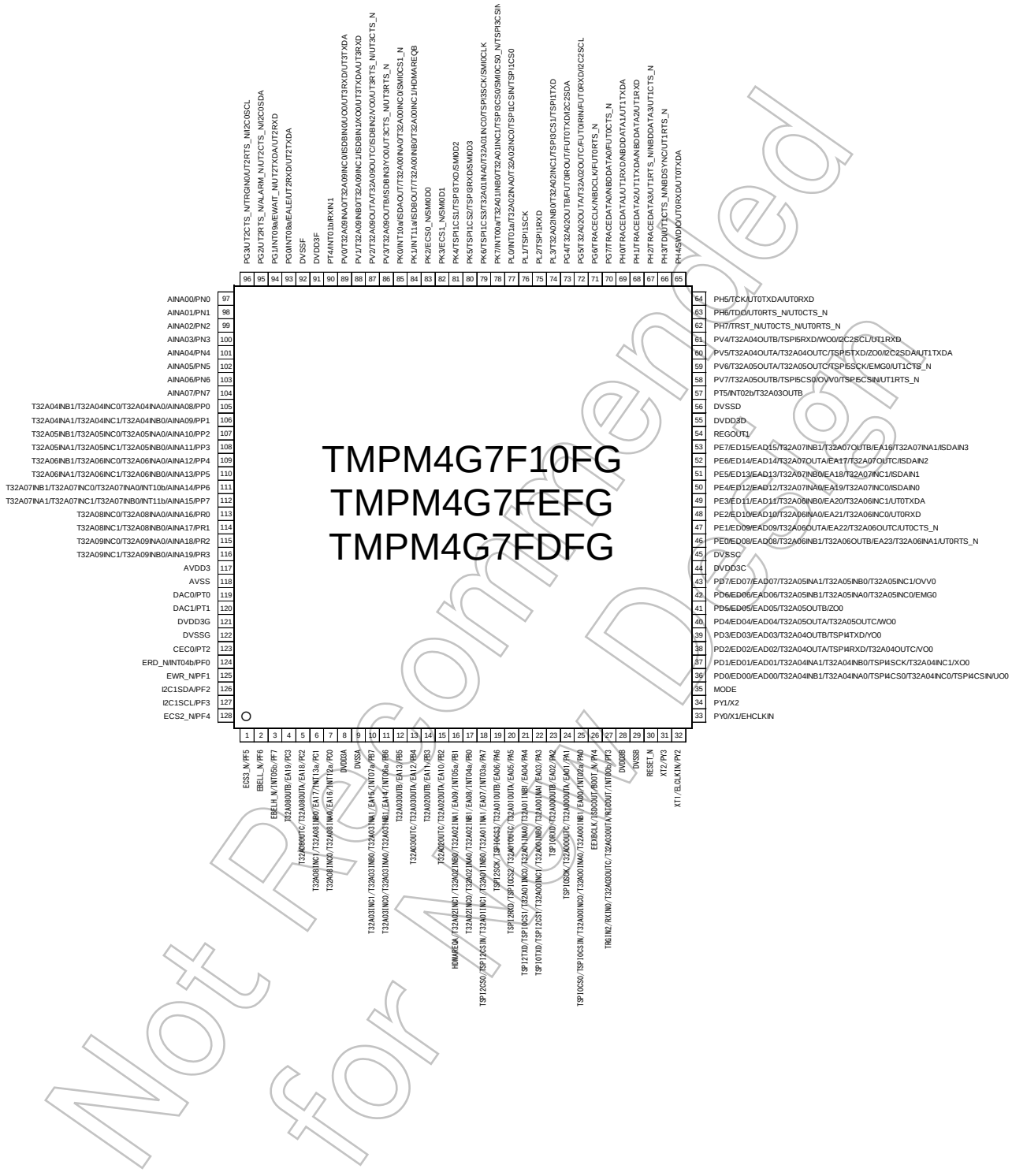
2. Pin Assignment

2.1. LQFP176

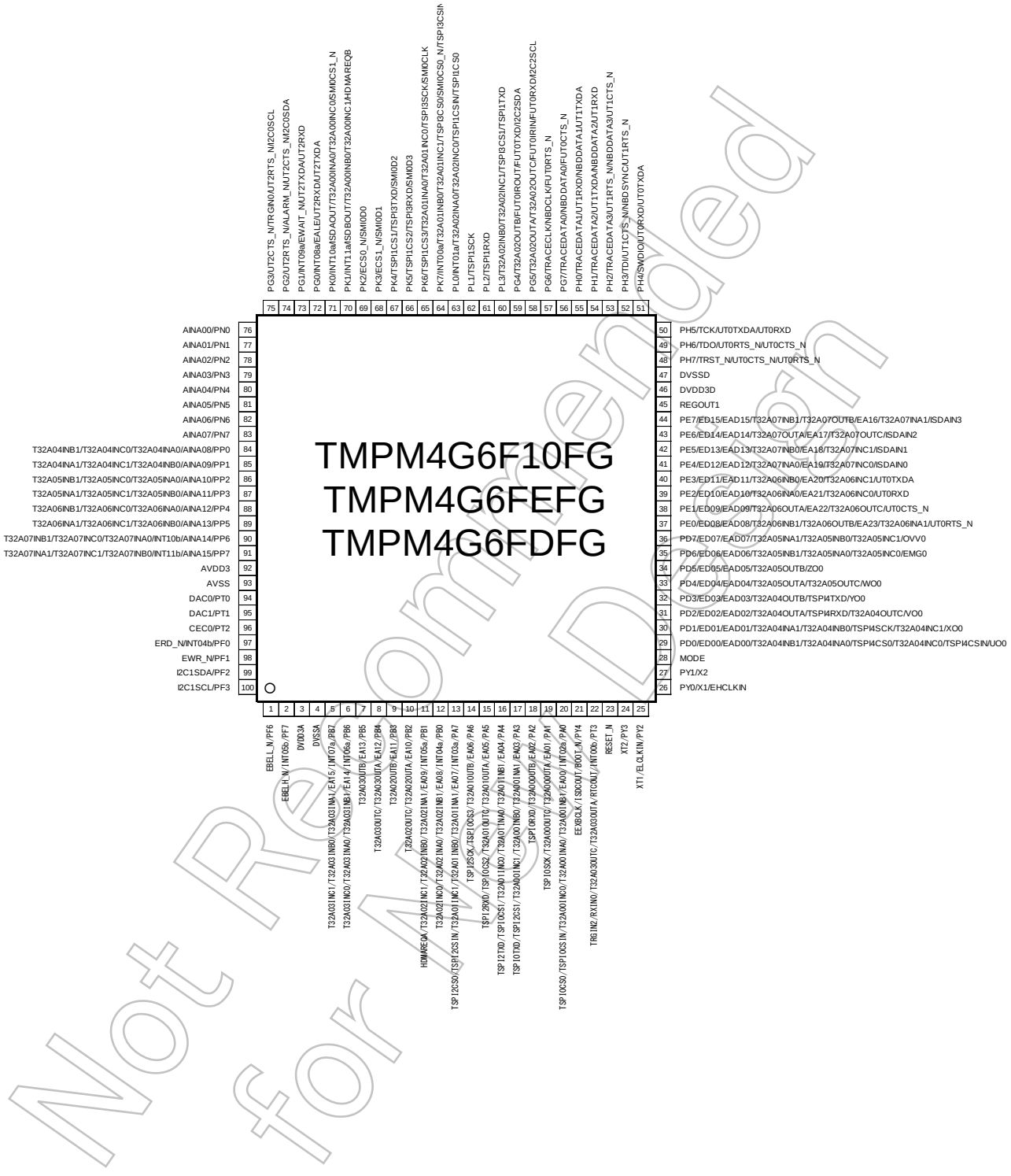
2.2. LQFP144



2.3. LQFP128



2.4. LQFP100



2.5. VFBGA177

TMPM4G9F15XBG/TMPM4G9F10XBG/TMPM4G9FEXBG/TMPM4G9FDXBG

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DVDD3A	PF4	PF3	PF1	PT1	PT0	AVDD3	PR4	PR3	PP7	PP3	PN7	PN5	PN3	PN1	DVSSF
B	PF7	PF6	PF5	PF2	PJ0	PJ1	AVSS	PR5	PR2	PP6	PP2	PN6	PN4	PN2	PN0	PG3
C	PC4	PC5	–	–	–	–	–	–	–	–	–	–	–	–	PG2	PG1
D	PC2	PC3	–	PC7	PF0	PJ2	PJ3	PR7	PR1	PP5	PP1	PP0	DVSSE	–	PG0	PL4
E	PB4	PB5	–	PC6	DVSSH	PT2	PL6	PL7	PR6	PR0	PP4	DVSSD	PM3	–	PL5	PM0
F	PB2	PB3	–	PC0	PC1	DVSSG	–	–	–	–	–	PV0	PT4	–	PM1	PM2
G	PB0	PB1	–	PB6	PB7	–	–	–	–	–	–	PV2	PV1	–	PW4	PW5
H	PA6	PA7	–	PU0	PT3	–	–	–	–	–	–	PK0	PV3	–	PW6	PW7
J	PA4	PA5	–	PU1	PU2	–	–	–	–	–	–	PK1	PK2	–	PK4	PK6
K	PA2	PA3	–	PU3	PU4	–	–	–	–	–	–	PK7	PK3	–	PK5	PL1
L	PA0	PA1	–	PU6	PU5	–	–	–	–	–	–	PG4	PL0	–	PL2	PL3
M	DVSSA	PY4	–	PU7	DVDD3G	PD1	PD3	PD5	PD7	PW2	PW0	DVDD3D	PG5	–	PG7	PG6
N	PY3/XT2	DVSSB	–	DVDD3H	PD0	PD2	PD4	PD6	PJ7	PW3	PW1	PM4	DVDD3E	–	PH1	PH0
P	PY2/XT1	DVSSC	–	–	–	–	–	–	–	–	–	–	–	–	PH3	PH2
R	RESET_N	DVDD3B	DVDD3C	PE0	PE1	PE4	PE5	PJ6	PJ5	PT5	PV7	PV4	PM6	PH7	PH6	PH4
T	MODE	PY0/X1	PY1/X2	DVDD3F	PE2	PE3	PE6	PE7	PJ4	REGOUT1	PV6	PV5	PM7	PM5	PH5	BSC

2.6. VFBGA145

TMPM4G8F15XBG/TMPM4G8F10XBG/TMPM4G8FEXBG/TMPM4G8FDXBG

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	DVDD3A	PF4	PF3	PT1	PT0	AVDD3	PR3	PP7	PP3	PN7	PN5	PN3	PN1	DVSSF
B	PF7	PF6	PF5	PF2	PF1	AVSS	PR2	PP6	PP2	PN6	PN4	PN2	PN0	PG3
C	PC4	PC5	–	–	–	–	–	–	–	–	–	–	PG2	PG1
D	PC2	PC3	–	PC7	PF0	PR7	PR4	PR0	PP4	PP1	PP0	–	PG0	PM0
E	PB4	PB5	–	PC6	PT2	PR6	PR5	PR1	PP5	DVSSD DVSSE	PT4	–	PM1	PM2
F	PB2	PB3	–	PC0	PC1	DVSSG DVSSH	–	–	–	PV0	PV1	–	PM3	PK2
G	PA5	PA6	–	PB6	PB7	–	–	–	–	PV3	PV2	–	PK3	PK4
H	PA3	PA4	–	PB0	PB1	–	–	–	–	PK0	PK1	–	PK5	PK6
J	PA1	PA2	–	PA0	PA7	–	–	–	–	PK7	PL0	–	PL2	PL1
K	DVSSA	PY4	–	PT3	DVDD3G DVDD3H	PD2	PD5	PD6	PT5	DVDD3D DVDD3E	PG5	–	PG4	PL3
L	PY3/XT2	DVSSB	–	PD0	PD1	PD3	PD4	PD7	PV7	PM4	PH0	–	PG7	PG6
M	PY2/XT1	DVSSC	–	–	–	–	–	–	–	–	–	–	PH1	PH2
N	RESET_N	DVDD3B	DVDD3C	PE0	PE1	PE3	PE6	PE7	PV6	PV4	PM6	PH7	PH3	PH4
P	MODE	PY0/X1	PY1/X2	DVDD3F	PE2	PE4	PE5	REGOUT1	PV5	PM7	PM5	PH6	PH5	BSC

3. Memory Map

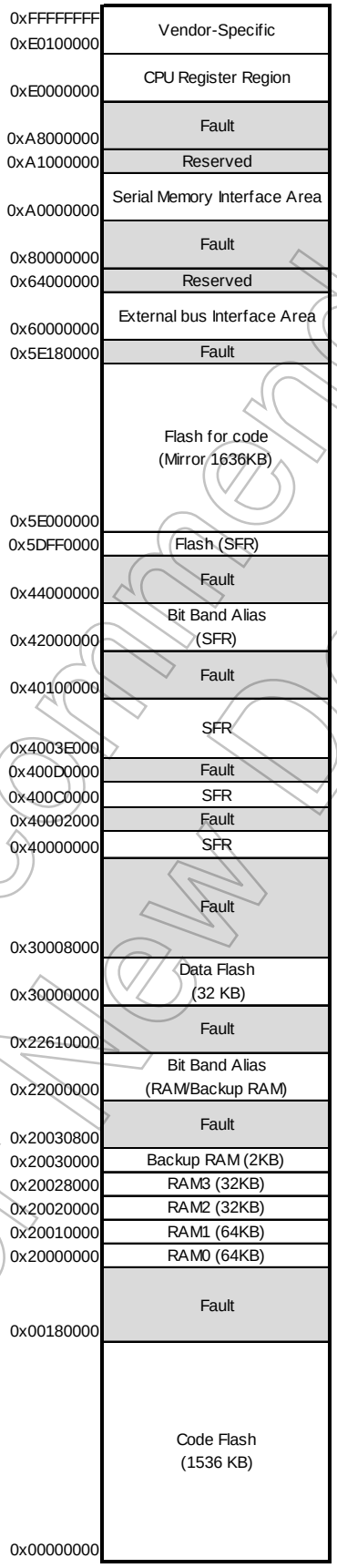


Figure 3.1 Example of the memory map of TMPM4G9F15

Note: “Fault” and “Reserved” areas should not be accessed.

3.1. List of Memory Sizes

Table 3.1 Memory sizes and addresses

Products			TMPM4G9F15FG TMPM4G9F15XBG TMPM4G8F15FG TMPM4G8F15XBG	TMPM4G9F10FG TMPM4G9F10XBG TMPM4G8F10FG TMPM4G8F10XBG TMPM4G7F10FG TMPM4G6F10FG	TMPM4G9FEFG TMPM4G9FEXBG TMPM4G8FEFG TMPM4G8FEXBG TMPM4G7FEFG TMPM4G6FEFG	TMPM4G9FDFG TMPM4G9FDXBG TMPM4G8FDFG TMPM4G8FDXBG TMPM4G7FDFG TMPM4G6FDFG
Peripheral region	Code Flash (Mirror)	START	0x5E000000	0x5E000000	0x5E000000	0x5E000000
		END	0x5E17FFFF	0x5E0FFFFF	0x5E0BFFFF	0x5E07FFFF
SRAM region	Data Flash	Size	32 KB			
		START	0x30000000			
		END	0x30007FFF			
	Backup RAM	Size	2 KB			
		START	0x20030000			
		END	0x200307FF			
	RAM	Size	192 KB		128 KB	
		START(0)	0x20000000			
		END(0)	0x2000FFFF			
		START(1)	0x20010000		0x20010000	
		END(1)	0x2001FFFF		0x20017FFF	
		START(2)	0x20020000		-	
		END(2)	0x20027FFF		-	
		START(3)	0x20028000			
		END(3)	0x2002FFFF			
Code region	Code Flash	Size	1536 KB	1024 KB	768 KB	512 KB
		START	0x00000000	0x00000000	0x00000000	0x00000000
		END	0x0017FFFF	0x000FFFFF	0x000BFFFF	0x0007FFFF

4. Pin Description

4.1. Functional Pin Name and Function

4.1.1. Peripheral Function Pins

Table 4.1 Pin names and functions of peripheral pins

Peripheral function	Pin name	Input or Output	Function
Interrupt control	INTx	Input	External interrupt input pin External input pin provides the noise filter (filter width: typ. 30 ns).
32-bit Timer event counter (T32A)	T32AxINA0	Input	16-bit timer-A input capture input pin 0
	T32AxINA1	Input	16-bit timer-A input capture input pin 1
	T32AxOUTA	Output	16-bit timer A output pin
	T32AxINB0	Input	16-bit timer B input capture input pin 0
	T32AxINB1	Input	16-bit timer B input capture input pin 1
	T32AxOUTB	Output	16-bit timer B output pin
	T32AxINC0	Input	32-bit timer C input capture input pin 0
	T32AxINC1	Input	32-bit timer C input capture input pin 1
	T32AxOUTC	Output	32-bit timer C output pin
Serial peripheral interface (TSPI)	TSPIxRXD	Input	Data input pin
	TSPIxTXD	Output	Data output pin
	TSPIxSCK	I/O	Clock input/output pin
	TSPIxCS0	Output	Chip select output pin 0
	TSPIxCS1	Output	Chip select output pin 1
	TSPIxCS2	Output	Chip select output pin 2
	TSPIxCS3	Output	Chip select output pin 3
	TSPIxCSIN	Input	Chip select input pin
Serial Memory Interface (SMIF)	SMIxCLK	Output	Clock output pin
	SMIxD0	I/O	Data input/output pin 0
	SMIxD1	I/O	Data input/output pin 1
	SMIxD2	I/O	Data input/output pin 2
	SMIxD3	I/O	Data input/output pin 3
	SMIxCSx_N	Output	Chip select output pin

Asynchronous serial communication circuit (UART)	UTxTXDA	Output	Data output pin A
	UTxRXD	Input	Data input pin
	UTxCTS_N	Input	Clear to send signal pin
	UTxRTS_N	Output	Request to send signal pin
Full Universal Asynchronous Receiver Transmitter circuit (FUART)	FUTxTXD	Output	Data output pin
	FUTxRXD	Input	Data input pin
	FUTxCTS_N	Input	Transmission control input pin
	FUTxRTS_N	Output	Transmission request output pin
	FUTxIROUT	Output	IrDA 1.0 Data output pin
	FUTxIRIN	Input	IrDA 1.0 Data input pin
I^2C interface (I^2C)	I2CxSDA	I/O	Data input/output pin
	I2CxSCL	I/O	Clock input/output pin
High speed DMA Controller (HDMAC)	HDMAREQx	Input	HDMA request input pin
Interval Sensor Detection (ISD)	ISDxIN0	Input	Data input pin 0
	ISDxIN1	Input	Data input pin 1
	ISDxIN2	Input	Data input pin 2
	ISDxIN3	Input	Data input pin 3
	ISDxOUT	Output	Data output pin
Consumer Electronics Control Circuit (CEC)	CECx	I/O	Data input/output pin
External bus interface (EBIF)	EAx	Output	Address bus output pin
	EDx	I/O	Data bus input/output pin
	ERD_N	Output	Read strobe output pin
	EWR_N	Output	Write strobe output pin
	ECSx_N	Output	Chip select output pin
	EBELL_N	Output	Byte enable output pin
	EBELH_N	Output	Byte enable output pin
	EALE	Output	Address latch enable output pin
	EWAIT_N	Input	Wait input pin
	EEXBCLK	Output	Clock output pin

Advanced Programmable Motor control circuit (A-PMD)	XOx	Output	X-phase output pin
	YOx	Output	Y-phase output pin
	ZOx	Output	Z-phase output pin
	UOx	Output	U-phase output pin
	VOx	Output	V-phase output pin
	WOx	Output	W-phase output pin
	EMGx	Input	Emergency state detection input pin
	OVVx	Input	Overvoltage detection input pin
Trigger input (TRGSEL)	TRGINx	Input	External trigger input pin (MDMAC/ADC)
Analog to digital converter (ADC)	AINAx	Input	Analog input pin
Digital to analog converter (DAC)	DACx	Output	DAC output pin
Remote Control Signal Preprocessor (RMC)	RXINx	Input	Remote Signaling Data input pin
Real Time Clock (RTC)	ALARM_N	Output	Alarm output pin
	RTCOUT	Output	1Hz clock output pin

Note: “x” means channel number or unit number or interrupt number.

4.1.2. Debug Pins

There are the special pins which output internal information using TRACE and NBDIF as well as basic debug pins of JTAG/SWD.

Table 4.2 Debug pin names and functions

Debug Function	Pin name	Input or Output	Function
JTAG	TMS	Input	JTAG test mode selection input pin
	TCK	Input	JTAG serial clock input pin
	TDO	Output	JTAG serial data output pin
	TDI	Input	JTAG serial data input pin
	TRST_N	Input	JTAG test reset input pin JTAG test reset input pin have noise filter(filter width: typ.30ns)
SW	SWDIO	I/O	Serial wire data input/output pin
	SWCLK	Input	Serial wire clock input pin
	SWV	Output	Serial wire viewer output pin
TRACE	TRACECLK	Output	Trace clock output pin
	TRACEDATA0	Output	Trace data output pin 0
	TRACEDATA1	Output	Trace data output pin 1
	TRACEDATA2	Output	Trace data output pin 2
	TRACEDATA3	Output	Trace data output pin 3
NBDIF	NBDSYNC	Input	Non-break debug synchronous input pin
	NBDCLK	Input	Non-break debug clock input pin
	NBDDATA0	I/O	Non-break debug data input/output pin 0
	NBDDATA1	I/O	Non-break debug data input/output pin 1
	NBDDATA2	I/O	Non-break debug data input/output pin 2
	NBDDATA3	I/O	Non-break debug data input/output pin 3

4.1.3. Control Pins

Table 4.3 Control pin names and functions

	Pin name	Input or Output	Function
Control pin	X1	Input	High speed oscillator connection pin, External clock input pin
	X2	Output	High speed oscillator connection pin
	XT1	Input	Low speed oscillator connection pin, Low clock input pin
	XT2	Output	Low speed oscillator connection pin
	MODE	Input	Mode pin This pin must be fixed to "Low" level.
	RESET_N	Input	Reset signal input pin Reset signal input pin has noise filter(filter width: typ.30ns)
	BOOT_N	Input	BOOT mode control pin The BOOT mode control pin is sampled at the rising edge of the RESET_N pin input or the rising edge of POR, whichever is delayed. It's not sampled by internal Reset factor. If the BOOT mode control pin is "Low" level, the MCU enters single boot mode. If it is "High", the MCU enters single chip mode. For details, refer to "Flash Memory" reference manual.
	BSC	Input	Boundary-scan mode control pin

4.1.4. Power Supply Pins

Table 4.4 Power supply pin names and functions

Power Supply	Pin name	Function
Power	DVDD3A (Note1) DVDD3B (Note1) DVDD3C (Note1) DVDD3D (Note1) DVDD3E (Note1) DVDD3F (Note1) DVDD3G (Note1) DVDD3H (Note1)	Power supply pin for digital DVDD3A/B/C/D/E/F/G/H supplies the power to the following pins: PA to PH, PJ to PM, PT(PT2 to PT5), PU to PW, PY, X1, X2, XT1, XT2, MODE, RESET_N, BOOT_N,BSC
	DVSSA (Note2) DVSSB (Note2) DVSSC (Note2) DVSSD (Note2) DVSSE (Note2) DVSSF (Note2) DVSSG (Note2) DVSSH (Note2)	GND pin for digital
	REGOUT1 (Note3)	Capacitor for a regulator connection pin (Note4)
	AVDD3	Power supply pin and Reference power pin (VREFH) for analog circuits A AVDD3 supplies the power to the following pins: PN, PP, PR, PT(PT0, PT1)
	AVSS	GND pin and Reference GND (VREFL)pin for analog circuits

Note1: Apply the voltage to DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, and DVDD3H at the same potential except the case that the pins are not provided.

Note2: Apply the external voltage to DVSSA, DVSSB, DVSSC, DVSSD, DVSSE, DVSSF, DVSSG, and DVSSH at the same potential except the case that the pins are not provided.

Note3: For REGOUT1, do not cause a short circuit with DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H, DVSSA, DVSSB, DVSSC, DVSSD, DVSSE, DVSSF, DVSSG, or DVSSH

Note4: For the capacitor value, refer to the “Electrical Characteristics”

4.2. Functional Pin and Port Assignment (Pin Number)

Following table shows a pin number of the port assignment and each product which were seen from the functional pin.

"-" means that does not have a pin or there is no assignment of a function.

Table 4.5 List of signal connections (1/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
UT0RXD	PE2	60	52	48	39	T5	P5
	PH4	89	73	65	51	R16	N14
	PH5	88	72	64	50	T15	P13
UT0TXDA	PE3	61	53	49	40	T6	N6
	PH5	88	72	64	50	T15	P13
	PH4	89	73	65	51	R16	N14
UT0CTS_N	PE1	59	51	47	38	R5	N5
	PH7	86	70	62	48	R14	N12
	PH6	87	71	63	49	R15	P12
UT0RTS_N	PE0	58	50	46	37	R4	N4
	PH6	87	71	63	49	R15	P12
	PH7	86	70	62	48	R14	N12
UT1RXD	PH0	93	77	69	55	N16	L11
	PH1	92	76	68	54	N15	M13
	PV4	81	65	61	-	R12	N10
UT1TXDA	PH1	92	76	68	54	N15	M13
	PH0	93	77	69	55	N16	L11
	PV5	80	64	60	-	T12	P9
UT1CTS_N	PH3	90	74	66	52	P15	N13
	PH2	91	75	67	53	P16	M14
	PV6	79	63	59	-	T11	N9
UT1RTS_N	PH2	91	75	67	53	P16	M14
	PH3	90	74	66	52	P15	N13
	PV7	78	62	58	-	R11	L9

Table 4.6 List of signal connections (2/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
UT2RXD	PG0	129	105	93	72	D15	D13
	PG1	130	106	94	73	C16	C14
UT2TXDA	PG1	130	106	94	73	C16	C14
	PG0	129	105	93	72	D15	D13
UT2CTS_N	PG3	132	108	96	75	B16	B14
	PG2	131	107	95	74	C15	C13
UT2RTS_N	PG2	131	107	95	74	C15	C13
	PG3	132	108	96	75	B16	B14
UT3RXD	PU6	40	-	-	-	L4	-
	PV0	115	97	89	-	F12	F10
	PV1	114	96	88	-	G13	F11
UT3TXDA	PU7	41	-	-	-	M4	-
	PV1	114	96	88	-	G13	F11
	PV0	115	97	89	-	F12	F10
UT3CTS_N	PU5	39	-	-	-	L5	-
	PV3	112	94	86	-	H13	G10
	PV2	113	95	87	-	G12	G11
UT3RTS_N	PU4	38	-	-	-	K5	-
	PV2	113	95	87	-	G12	G11
	PV3	112	94	86	-	H13	G10
UT4RXD	PM0	124	102	-	-	E16	D14
	PM1	123	101	-	-	F15	E13
	PU1	35	-	-	-	J4	-
UT4TXDA	PM1	123	101	-	-	F15	E13
	PM0	124	102	-	-	E16	D14
	PU0	34	-	-	-	H4	-
UT4CTS_N	PM3	121	99	-	-	E13	F13
	PM2	122	100	-	-	F16	E14
	PU2	36	-	-	-	J5	-
UT4RTS_N	PM2	122	100	-	-	F16	E14
	PM3	121	99	-	-	E13	F13
	PU3	37	-	-	-	K4	-

Table 4.7 List of signal connections (3/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
UT5RXD	PJ0	168	-	-	-	B5	-
	PJ1	167	-	-	-	B6	-
UT5TXDA	PJ1	167	-	-	-	B6	-
	PJ0	168	-	-	-	B5	-
UT5CTS_N	PJ3	165	-	-	-	D7	-
	PJ2	166	-	-	-	D6	-
UT5RTS_N	PJ2	166	-	-	-	D6	-
	PJ3	165	-	-	-	D7	-
FUT0RXD	PG5	96	80	72	58	M13	K11
	PJ5	68	-	-	-	R9	-
FUT0TXD	PG4	97	81	73	59	L12	K13
	PJ4	69	-	-	-	T9	-
FUT0CTS_N	PG7	94	78	70	56	M15	L13
FUT0RTS_N	PG6	95	79	71	57	M16	L14
FUT0IROUT	PG4	97	81	73	59	L12	K13
FUT0IRIN	PG5	96	80	72	58	M13	K11
FUT1RXD	PJ7	66	-	-	-	N9	-
	PM6	83	67	-	-	R13	N11
FUT1TXD	PJ6	67	-	-	-	R8	-
	PM7	82	66	-	-	T13	P10
FUT1CTS_N	PM4	85	69	-	-	N12	L10
FUT1RTS_N	PM5	84	68	-	-	T14	P11
FUT1IROUT	PM7	82	66	-	-	T13	P10
FUT1IRIN	PM6	83	67	-	-	R13	N11
I2C0SDA	PG2	131	107	95	74	C15	C13
I2C0SCL	PG3	132	108	96	75	B16	B14
I2C1SDA	PF2	174	142	126	99	B4	B4
I2C1SCL	PF3	175	143	127	100	A3	A3
I2C2SDA	PG4	97	81	73	59	L12	K13
	PV5	80	64	60	-	T12	P9
I2C2SCL	PG5	96	80	72	58	M13	K11
	PV4	81	65	61	-	R12	N10

Table 4.8 List of signal connections (4/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
I2C3SDA	PJ6	67	-	-	-	R8	-
	PM0	124	102	-	-	E16	D14
I2C3SCL	PJ7	66	-	-	-	N9	-
	PM1	123	101	-	-	F15	E13
I2C4SDA	PJ3	165	-	-	-	D7	-
	PM6	83	67	-	-	R13	N11
I2C4SCL	PJ2	166	-	-	-	D6	-
	PM7	82	66	-	-	T13	P10
ISDAIN0	PE4	62	54	50	41	R6	P6
ISDAIN1	PE5	63	55	51	42	R7	P7
ISDAIN2	PE6	64	56	52	43	T7	N7
ISDAIN3	PE7	65	57	53	44	T8	N8
ISDAOUT	PK0	111	93	85	71	H12	H10
ISDBIN0	PV0	115	97	89	-	F12	F10
ISDBIN1	PV1	114	96	88	-	G13	F11
ISDBIN2	PV2	113	95	87	-	G12	G11
ISDBIN3	PV3	112	94	86	-	H13	G10
ISDBOUT	PK1	110	92	84	70	J12	H11
ISDCIN0	PW4	120	-	-	-	G15	-
ISDCIN1	PW5	119	-	-	-	G16	-
ISDCIN2	PW6	118	-	-	-	H15	-
ISDCIN3	PW7	117	-	-	-	H16	-
ISDCOUT	PY4	30	30	26	21	M2	K2
TSPI0CSIN	PA0	29	29	25	20	L1	J4
TSPI0CS0	PA0	29	29	25	20	L1	J4
TSPI0CS1	PA4	25	25	21	16	J1	H2
TSPI0CS2	PA5	24	24	20	15	J2	G1
TSPI0CS3	PA6	23	23	19	14	H1	G2
TSPI0RXD	PA2	27	27	23	18	K1	J2
TSPI0TXD	PA3	26	26	22	17	K2	H1
TSPI0SCK	PA1	28	28	24	19	L2	J1

Table 4.9 List of signal connections (5/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
TSPI1CSIN	PL0	103	85	77	63	L13	J11
TSPI1CS0	PL0	103	85	77	63	L13	J11
TSPI1CS1	PK4	107	89	81	67	J15	G14
TSPI1CS2	PK5	106	88	80	66	K15	H13
TSPI1CS3	PK6	105	87	79	65	J16	H14
TSPI1RXD	PL2	101	83	75	61	L15	J13
TSPI1TXD	PL3	100	82	74	60	L16	K14
TSPI1SCK	PL1	102	84	76	62	K16	J14
TSPI2CSIN	PA7	22	22	18	13	H2	J5
TSPI2CS0	PA7	22	22	18	13	H2	J5
TSPI2CS1	PA3	26	26	22	17	K2	H1
TSPI2RXD	PA5	24	24	20	15	J2	G1
TSPI2TXD	PA4	25	25	21	16	J1	H2
TSPI2SCK	PA6	23	23	19	14	H1	G2
TSPI3CSIN	PK7	104	86	78	64	K12	J10
TSPI3CS0	PK7	104	86	78	64	K12	J10
TSPI3CS1	PL3	100	82	74	60	L16	K14
TSPI3RXD	PK5	106	88	80	66	K15	H13
TSPI3TXD	PK4	107	89	81	67	J15	G14
TSPI3SCK	PK6	105	87	79	65	J16	H14
TSPI4CSIN	PD0	48	40	36	29	N5	L4
TSPI4CS0	PD0	48	40	36	29	N5	L4
TSPI4RXD	PD2	50	42	38	31	N6	K6
TSPI4TXD	PD3	51	43	39	32	M7	L6
TSPI4SCK	PD1	49	41	37	30	M6	L5
TSPI5CSIN	PV7	78	62	58	-	R11	L9
TSPI5CS0	PV7	78	62	58	-	R11	L9
TSPI5RXD	PV4	81	65	61	-	R12	N10
TSPI5TXD	PV5	80	64	60	-	T12	P9
TSPI5SCK	PV6	79	63	59	-	T11	N9
TSPI6CSIN	PM3	121	99	-	-	E13	F13
TSPI6CS0	PM3	121	99	-	-	E13	F13
TSPI6RXD	PM1	123	101	-	-	F15	E13
TSPI6TXD	PM0	124	102	-	-	E16	D14
TSPI6SCK	PM2	122	100	-	-	F16	E14

Table 4.10 List of signal connections (6/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
TSPI7CSIN	PM4	85	69	-	-	N12	L10
TSPI7CS0	PM4	85	69	-	-	N12	L10
TSPI7RXD	PM6	83	67	-	-	R13	N11
TSPI7TXD	PM7	82	66	-	-	T13	P10
TSPI7SCK	PM5	84	68	-	-	T14	P11
TSPI8CSIN	PW0	77	-	-	-	M11	-
TSPI8CS0	PW0	77	-	-	-	M11	-
TSPI8RXD	PW2	75	-	-	-	M10	-
TSPI8TXD	PW3	74	-	-	-	N10	-
TSPI8SCK	PW1	76	-	-	-	N11	-
SMI0CS1_N	PK0	111	93	85	71	H12	H10
SMI0D0	PK2	109	91	83	69	J13	F14
SMI0D1	PK3	108	90	82	68	K13	G13
SMI0D2	PK4	107	89	81	67	J15	G14
SMI0D3	PK5	106	88	80	66	K15	H13
SMI0CLK	PK6	105	87	79	65	J16	H14
SMI0CS0_N	PK7	104	86	78	64	K12	J10
T32A00INA0	PA0	29	29	25	20	L1	J4
	PK0	111	93	85	71	H12	H10
T32A00INA1	PA3	26	26	22	17	K2	H1
T32A00OUTA	PA1	28	28	24	19	L2	J1
	PW1	76	-	-	-	N11	-
T32A00INB0	PA3	26	26	22	17	K2	H1
	PK1	110	92	84	70	J12	H11
T32A00INB1	PA0	29	29	25	20	L1	J4
T32A00OUTB	PA2	27	27	23	18	K1	J2
	PW0	77	-	-	-	M11	-
T32A00INC0	PA0	29	29	25	20	L1	J4
	PK0	111	93	85	71	H12	H10
T32A00INC1	PA3	26	26	22	17	K2	H1
	PK1	110	92	84	70	J12	H11
T32A00OUTC	PA1	28	28	24	19	L2	J1
	PW1	76	-	-	-	N11	-

Table 4.11 List of signal connections (7/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
T32A01INA0	PA4	25	25	21	16	J1	H2
	PK6	105	87	79	65	J16	H14
T32A01INA1	PA7	22	22	18	13	H2	J5
T32A01OUTA	PA5	24	24	20	15	J2	G1
	PW2	75	-	-	-	M10	-
T32A01INB0	PA7	22	22	18	13	H2	J5
	PK7	104	86	78	64	K12	J10
T32A01INB1	PA4	25	25	21	16	J1	H2
T32A01OUTB	PA6	23	23	19	14	H1	G2
	PW3	74	-	-	-	N10	-
T32A01INC0	PA4	25	25	21	16	J1	H2
	PK6	105	87	79	65	J16	H14
T32A01INC1	PA7	22	22	18	13	H2	J5
	PK7	104	86	78	64	K12	J10
T32A01OUTC	PA5	24	24	20	15	J2	G1
	PW2	75	-	-	-	M10	-
T32A02INA0	PB0	21	21	17	12	G1	H4
	PL0	103	85	77	63	L13	J11
T32A02INA1	PB1	20	20	16	11	G2	H5
T32A02OUTA	PB2	19	19	15	10	F1	F1
	PG5	96	80	72	58	M13	K11
T32A02INB0	PB1	20	20	16	11	G2	H5
	PL3	100	82	74	60	L16	K14
T32A02INB1	PB0	21	21	17	12	G1	H4
T32A02OUTB	PB3	18	18	14	9	F2	F2
	PG4	97	81	73	59	L12	K13
T32A02INC0	PB0	21	21	17	12	G1	H4
	PL0	103	85	77	63	L13	J11
T32A02INC1	PB1	20	20	16	11	G2	H5
	PL3	100	82	74	60	L16	K14
T32A02OUTC	PB2	19	19	15	10	F1	F1
	PG5	96	80	72	58	M13	K11

Table 4.12 List of signal connections (8/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
T32A03INA0	PB6	15	15	11	6	G4	G4
	PJ4	69	-	-	-	T9	-
T32A03INA1	PB7	14	14	10	5	G5	G5
T32A03OUTA	PB4	17	17	13	8	E1	E1
	PT3	31	31	27	22	H5	K4
T32A03INB0	PB7	14	14	10	5	G5	G5
	PJ5	68	-	-	-	R9	-
T32A03INB1	PB6	15	15	11	6	G4	G4
T32A03OUTB	PB5	16	16	12	7	E2	E2
	PT5	73	61	57	-	R10	K9
T32A03INC0	PB6	15	15	11	6	G4	G4
	PJ4	69	-	-	-	T9	-
T32A03INC1	PB7	14	14	10	5	G5	G5
	PJ5	68	-	-	-	R9	-
T32A03OUTC	PB4	17	17	13	8	E1	E1
	PT3	31	31	27	22	H5	K4
T32A04INA0	PD0	48	40	36	29	N5	L4
	PP0	141	117	105	84	D12	D11
T32A04INA1	PD1	49	41	37	30	M6	L5
	PP1	142	118	106	85	D11	D10
T32A04OUTA	PD2	50	42	38	31	N6	K6
	PV5	80	64	60	-	T12	P9
T32A04INB0	PD1	49	41	37	30	M6	L5
	PP1	142	118	106	85	D11	D10
T32A04INB1	PD0	48	40	36	29	N5	L4
	PP0	141	117	105	84	D12	D11
T32A04OUTB	PD3	51	43	39	32	M7	L6
	PV4	81	65	61	-	R12	N10
T32A04INC0	PD0	48	40	36	29	N5	L4
	PP0	141	117	105	84	D12	D11
T32A04INC1	PD1	49	41	37	30	M6	L5
	PP1	142	118	106	85	D11	D10
T32A04OUTC	PD2	50	42	38	31	N6	K6
	PV5	80	64	60	-	T12	P9

Table 4.13 List of signal connections (9/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
T32A05INA0	PD6	54	46	42	35	N8	K8
	PP2	143	119	107	86	B11	B9
T32A05INA1	PD7	55	47	43	36	M9	L8
	PP3	144	120	108	87	A11	A9
T32A05OUTA	PD4	52	44	40	33	N7	L7
	PV6	79	63	59	-	T11	N9
T32A05INB0	PD7	55	47	43	36	M9	L8
	PP3	144	120	108	87	A11	A9
T32A05INB1	PD6	54	46	42	35	N8	K8
	PP2	143	119	107	86	B11	B9
T32A05OUTB	PD5	53	45	41	34	M8	K7
	PV7	78	62	58	-	R11	L9
T32A05INC0	PD6	54	46	42	35	N8	K8
	PP2	143	119	107	86	B11	B9
T32A05INC1	PD7	55	47	43	36	M9	L8
	PP3	144	120	108	87	A11	A9
T32A05OUTC	PD4	52	44	40	33	N7	L7
	PV6	79	63	59	-	T11	N9
T32A06INA0	PE2	60	52	48	39	T5	P5
	PP4	145	121	109	88	E11	D9
T32A06INA1	PE0	58	50	46	37	R4	N4
	PP5	146	122	110	89	D10	E9
T32A06OUTA	PE1	59	51	47	38	R5	N5
	PM5	84	68	-	-	T14	P11
T32A06INB0	PE3	61	53	49	40	T6	N6
	PP5	146	122	110	89	D10	E9
T32A06INB1	PE0	58	50	46	37	R4	N4
	PP4	145	121	109	88	E11	D9
T32A06OUTB	PE0	58	50	46	37	R4	N4
	PM4	85	69	-	-	N12	L10
T32A06INC0	PE2	60	52	48	39	T5	P5
	PP4	145	121	109	88	E11	D9
T32A06INC1	PE3	61	53	49	40	T6	N6
	PP5	146	122	110	89	D10	E9
T32A06OUTC	PE1	59	51	47	38	R5	N5
	PM5	84	68	-	-	T14	P11

Table 4.14 List of signal connections (10/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
T32A07INA0	PE4	62	54	50	41	R6	P6
	PP6	147	123	111	90	B10	B8
T32A07INA1	PE7	65	57	53	44	T8	N8
	PP7	148	124	112	91	A10	A8
T32A07OUTA	PE6	64	56	52	43	T7	N7
	PM6	83	67	-	-	R13	N11
T32A07INB0	PE5	63	55	51	42	R7	P7
	PP7	148	124	112	91	A10	A8
T32A07INB1	PE7	65	57	53	44	T8	N8
	PP6	147	123	111	90	B10	B8
T32A07OUTB	PE7	65	57	53	44	T8	N8
	PM7	82	66	-	-	T13	P10
T32A07INC0	PE4	62	54	50	41	R6	P6
	PP6	147	123	111	90	B10	B8
T32A07INC1	PE5	63	55	51	42	R7	P7
	PP7	148	124	112	91	A10	A8
T32A07OUTC	PE6	64	56	52	43	T7	N7
	PM6	83	67	-	-	R13	N11
T32A08INA0	PC0	11	11	7	-	F4	F4
	PR0	149	125	113	-	E10	D8
T32A08OUTA	PC2	9	9	5	-	D1	D1
	PL4	126	-	-	-	D16	-
T32A08INB0	PC1	10	10	6	-	F5	F5
	PR1	150	126	114	-	D9	E8
T32A08OUTB	PC3	8	8	4	-	D2	D2
	PL5	125	-	-	-	E15	-
T32A08INC0	PC0	11	11	7	-	F4	F4
	PR0	149	125	113	-	E10	D8
T32A08INC1	PC1	10	10	6	-	F5	F5
	PR1	150	126	114	-	D9	E8
T32A08OUTC	PC2	9	9	5	-	D1	D1
	PL4	126	-	-	-	D16	-

Table 4.15 List of signal connections (11/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
T32A09INA0	PR2	151	127	115	-	B9	B7
	PV0	115	97	89	-	F12	F10
T32A09OUTA	PL6	164	-	-	-	E7	-
	PV2	113	95	87	-	G12	G11
T32A09INB0	PR3	152	128	116	-	A9	A7
	PV1	114	96	88	-	G13	F11
T32A09OUTB	PL7	163	-	-	-	E8	-
	PV3	112	94	86	-	H13	G10
T32A09INC0	PR2	151	127	115	-	B9	B7
	PV0	115	97	89	-	F12	F10
T32A09INC1	PR3	152	128	116	-	A9	A7
	PV1	114	96	88	-	G13	F11
T32A09OUTC	PL6	164	-	-	-	E7	-
	PV2	113	95	87	-	G12	G11
T32A10INA0	PR4	153	129	-	-	A8	D7
	PW4	120	-	-	-	G15	-
T32A10INA1	PW7	117	-	-	-	H16	-
T32A10OUTA	PC4	7	7	-	-	C1	C1
	PW5	119	-	-	-	G16	-
T32A10INB0	PR5	154	130	-	-	B8	E7
T32A10OUTB	PC5	6	6	-	-	C2	C2
	PW4	120	-	-	-	G15	-
T32A10INC0	PR4	153	129	-	-	A8	D7
T32A10INC1	PR5	154	130	-	-	B8	E7
T32A10OUTC	PC4	7	7	-	-	C1	C1
	PW5	119	-	-	-	G16	-

Table 4.16 List of signal connections (12/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
T32A11INA0	PR6	155	131	-	-	E9	E6
	PW7	117	-	-	-	H16	-
T32A11INA1	PW4	120	-	-	-	G15	-
T32A11OUTA	PM2	122	100	-	-	F16	E14
	PW6	118	-	-	-	H15	-
T32A11INB0	PR7	156	132	-	-	D8	D6
T32A11OUTB	PM3	121	99	-	-	E13	F13
	PW7	117	-	-	-	H16	-
T32A11INC0	PR6	155	131	-	-	E9	E6
T32A11INC1	PR7	156	132	-	-	D8	D6
T32A11OUTC	PM2	122	100	-	-	F16	E14
	PW6	118	-	-	-	H15	-
T32A12INA0	PU2	36	-	-	-	J5	-
T32A12OUTA	PU0	34	-	-	-	H4	-
T32A12INB0	PU3	37	-	-	-	K4	-
T32A12OUTB	PU1	35	-	-	-	J4	-
T32A12INC0	PU2	36	-	-	-	J5	-
T32A12INC1	PU3	37	-	-	-	K4	-
T32A12OUTC	PU0	34	-	-	-	H4	-
T32A13INA0	PU5	39	-	-	-	L5	-
T32A13OUTA	PU6	40	-	-	-	L4	-
T32A13INB0	PU4	38	-	-	-	K5	-
T32A13OUTB	PU7	41	-	-	-	M4	-
T32A13INC0	PU5	39	-	-	-	L5	-
T32A13INC1	PU4	38	-	-	-	K5	-
T32A13OUTC	PU6	40	-	-	-	L4	-

Table 4.17 List of signal connections (13/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
EA00	PA0	29	29	25	20	L1	J4
EA01	PA1	28	28	24	19	L2	J1
EA02	PA2	27	27	23	18	K1	J2
EA03	PA3	26	26	22	17	K2	H1
EA04	PA4	25	25	21	16	J1	H2
EA05	PA5	24	24	20	15	J2	G1
EA06	PA6	23	23	19	14	H1	G2
EA07	PA7	22	22	18	13	H2	J5
EA08	PB0	21	21	17	12	G1	H4
EA09	PB1	20	20	16	11	G2	H5
EA10	PB2	19	19	15	10	F1	F1
EA11	PB3	18	18	14	9	F2	F2
EA12	PB4	17	17	13	8	E1	E1
EA13	PB5	16	16	12	7	E2	E2
EA14	PB6	15	15	11	6	G4	G4
EA15	PB7	14	14	10	5	G5	G5
EA16	PC0	11	11	7	-	F4	F4
	PE7	65	57	53	44	T8	N8
EA17	PC1	10	10	6	-	F5	F5
	PE6	64	56	52	43	T7	N7
EA18	PC2	9	9	5	-	D1	D1
	PE5	63	55	51	42	R7	P7
EA19	PC3	8	8	4	-	D2	D2
	PE4	62	54	50	41	R6	P6
EA20	PC4	7	7	-	-	C1	C1
	PE3	61	53	49	40	T6	N6
EA21	PC5	6	6	-	-	C2	C2
	PE2	60	52	48	39	T5	P5
EA22	PC6	5	5	-	-	E4	E4
	PE1	59	51	47	38	R5	N5
EA23	PC7	4	4	-	-	D4	D4
	PE0	58	50	46	37	R4	N4

Table 4.18 List of signal connections (14/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
ED00/EAD00	PD0	48	40	36	29	N5	L4
ED01/EAD01	PD1	49	41	37	30	M6	L5
ED02/EAD02	PD2	50	42	38	31	N6	K6
ED03/EAD03	PD3	51	43	39	32	M7	L6
ED04/EAD04	PD4	52	44	40	33	N7	L7
ED05/EAD05	PD5	53	45	41	34	M8	K7
ED06/EAD06	PD6	54	46	42	35	N8	K8
ED07/EAD07	PD7	55	47	43	36	M9	L8
ED08/EAD08	PE0	58	50	46	37	R4	N4
ED09/EAD09	PE1	59	51	47	38	R5	N5
ED10/EAD10	PE2	60	52	48	39	T5	P5
ED11/EAD11	PE3	61	53	49	40	T6	N6
ED12/EAD12	PE4	62	54	50	41	R6	P6
ED13/EAD13	PE5	63	55	51	42	R7	P7
ED14/EAD14	PE6	64	56	52	43	T7	N7
ED15/EAD15	PE7	65	57	53	44	T8	N8
ERD_N	PF0	172	140	124	97	D5	D5
EWR_N	PF1	173	141	125	98	A4	B5
ECS0_N	PK2	109	91	83	69	J13	F14
ECS1_N	PK3	108	90	82	68	K13	G13
ECS2_N	PF4	176	144	128	-	A2	A2
ECS3_N	PF5	1	1	1	-	B3	B3
EBELL_N	PF6	2	2	2	1	B2	B2
EBELH_N	PF7	3	3	3	2	B1	B1
EALE	PG0	129	105	93	72	D15	D13
EWAIT_N	PG1	130	106	94	73	C16	C14
EEXBCLK	PY4	30	30	26	21	M2	K2
NBDCLK	PG6	95	79	71	57	M16	L14
NBDDATA0	PG7	94	78	70	56	M15	L13
NBDDATA1	PH0	93	77	69	55	N16	L11
NBDDATA2	PH1	92	76	68	54	N15	M13
NBDDATA3	PH2	91	75	67	53	P16	M14
NBDSYNC	PH3	90	74	66	52	P15	N13

Table 4.19 List of signal connections (15/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
AINA00	PN0	133	109	97	76	B15	B13
AINA01	PN1	134	110	98	77	A15	A13
AINA02	PN2	135	111	99	78	B14	B12
AINA03	PN3	136	112	100	79	A14	A12
AINA04	PN4	137	113	101	80	B13	B11
AINA05	PN5	138	114	102	81	A13	A11
AINA06	PN6	139	115	103	82	B12	B10
AINA07	PN7	140	116	104	83	A12	A10
AINA08	PP0	141	117	105	84	D12	D11
AINA09	PP1	142	118	106	85	D11	D10
AINA10	PP2	143	119	107	86	B11	B9
AINA11	PP3	144	120	108	87	A11	A9
AINA12	PP4	145	121	109	88	E11	D9
AINA13	PP5	146	122	110	89	D10	E9
AINA14	PP6	147	123	111	90	B10	B8
AINA15	PP7	148	124	112	91	A10	A8
AINA16	PR0	149	125	113	-	E10	D8
AINA17	PR1	150	126	114	-	D9	E8
AINA18	PR2	151	127	115	-	B9	B7
AINA19	PR3	152	128	116	-	A9	A7
AINA20	PR4	153	129	-	-	A8	D7
AINA21	PR5	154	130	-	-	B8	E7
AINA22	PR6	155	131	-	-	E9	E6
AINA23	PR7	156	132	-	-	D8	D6
TRGIN0	PG3	132	108	96	75	B16	B14
TRGIN1	PL7	163	-	-	-	E8	-
DAC0	PT0	159	135	119	94	A6	A5
DAC1	PT1	160	136	120	95	A5	A4

Table 4.20 List of signal connections (16/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
INT00a	PK7	104	86	78	64	K12	J10
INT00b	PT3	31	31	27	22	H5	K4
INT01a	PL0	103	85	77	63	L13	J11
INT01b	PT4	116	98	90	-	F13	E11
INT02a	PA0	29	29	25	20	L1	J4
INT02b	PT5	73	61	57	-	R10	K9
INT03a	PA7	22	22	18	13	H2	J5
INT03b	PL6	164	-	-	-	E7	-
INT04a	PB0	21	21	17	12	G1	H4
INT04b	PF0	172	140	124	97	D5	D5
INT05a	PB1	20	20	16	11	G2	H5
INT05b	PF7	3	3	3	2	B1	B1
INT06a	PB6	15	15	11	6	G4	G4
INT06b	PU2	36	-	-	-	J5	-
INT07a	PB7	14	14	10	5	G5	G5
INT07b	PU3	37	-	-	-	K4	-
INT08a	PG0	129	105	93	72	D15	D13
INT08b	PU4	38	-	-	-	K5	-
INT09a	PG1	130	106	94	73	C16	C14
INT09b	PU5	39	-	-	-	L5	-
INT10a	PK0	111	93	85	71	H12	H10
INT10b	PP6	147	123	111	90	B10	B8
INT11a	PK1	110	92	84	70	J12	H11
INT11b	PP7	148	124	112	91	A10	A8
INT12a	PC0	11	11	7	-	F4	F4
INT12b	PL4	126	-	-	-	D16	-
INT13a	PC1	10	10	6	-	F5	F5
INT13b	PL5	125	-	-	-	E15	-
INT14a	PC6	5	5	-	-	E4	E4
INT14b	PM3	121	99	-	-	E13	F13
INT15a	PC7	4	4	-	-	D4	D4
INT15b	PM4	85	69	-	-	N12	L10

Table 4.21 List of signal connections (17/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
EMG0	PD6	54	46	42	35	N8	K8
	PV6	79	63	59	-	T11	N9
OVV0	PD7	55	47	43	36	M9	L8
	PV7	78	62	58	-	R11	L9
UO0	PD0	48	40	36	29	N5	L4
	PV0	115	97	89	-	F12	F10
VO0	PD2	50	42	38	31	N6	K6
	PV2	113	95	87	-	G12	G11
WO0	PD4	52	44	40	33	N7	L7
	PV4	81	65	61	-	R12	N10
XO0	PD1	49	41	37	30	M6	L5
	PV1	114	96	88	-	G13	F11
YO0	PD3	51	43	39	32	M7	L6
	PV3	112	94	86	-	H13	G10
ZO0	PD5	53	45	41	34	M8	K7
	PV5	80	64	60	-	T12	P9
CEC0	PT2	171	139	123	96	E6	E5
ALARM_N	PG2	131	107	95	74	C15	C13
RTCOUT	PT3	31	31	27	22	H5	K4
RXIN0	PT3	31	31	27	22	H5	K4
RXIN1	PT4	116	98	90	-	F13	E11
TRGIN2	PT3	31	31	27	22	H5	K4
HDMAREQA	PB1	20	20	16	11	G2	H5
HDMAREQB	PK1	110	92	84	70	J12	H11
TMS	PH4	89	73	65	51	R16	N14
TCK	PH5	88	72	64	50	T15	P13
TDO	PH6	87	71	63	49	R15	P12
TDI	PH3	90	74	66	52	P15	N13
TRST_N	PH7	86	70	62	48	R14	N12
SWDIO	PH4	89	73	65	51	R16	N14
SWCLK	PH5	88	72	64	50	T15	P13
SWV	PH6	87	71	63	49	R15	P12
TRACECLK	PG6	95	79	71	57	M16	L14
TRACEDATA0	PG7	94	78	70	56	M15	L13
TRACEDATA1	PH0	93	77	69	55	N16	L11
TRACEDATA2	PH1	92	76	68	54	N15	M13
TRACEDATA3	PH2	91	75	67	53	P16	M14

Table 4.22 List of signal connections (18/18)

Combination functional pin name	Port name	M4G9 (LQFP176)	M4G8 (LQFP144)	M4G7 (LQFP128)	M4G6 (LQFP100)	M4G9 (BGA177)	M4G8 (BGA145)
X1	PY0	45	37	33	26	T2	P2
X2	PY1	46	38	34	27	T3	P3
XT1	PY2	44	36	32	25	P1	M1
XT2	PY3	43	35	31	24	N1	L1
BOOT_N	PY4	30	30	26	21	M2	K2
EHCLKIN	PY0	45	37	33	26	T2	P2
ELCLKIN	PY2	44	36	32	25	P1	M1
RESET_N		42	34	30	23	R1	N1
MODE		47	39	35	28	T1	P1
BSC		-	-	-	-	T16	P14
DVDD3A		12	12	8	3	A1	A1
DVDD3B		32	32	28	-	R2	N2
DVDD3C		56	48	44	-	R3	N3
DVDD3D		72	59	55	46	M12	K10
DVDD3E		98	-	-	-	N13	K10
DVDD3F		127	103	91	-	T4	P4
DVDD3G		161	137	121	-	M5	K5
DVDD3H		169	-	-	-	N4	K5
DVSSA		13	13	9	4	M1	K1
DVSSB		33	33	29	-	N2	L2
DVSSC		57	49	45	-	P2	M2
DVSSD		72	60	56	47	E12	E10
DVSSE		99	-	-	-	D13	E10
DVSSF		128	104	92	-	A16	A14
DVSSG		162	138	122	-	F6	F6
DVSSH		170	-	-	-	E5	F6
REGOUT1		70	58	54	45	T10	P8
AVDD3		157	133	117	92	A7	A6
AVSS		158	134	118	93	B7	B6

4.3. Ports

The symbols of each table of port have the following meanings.

- Input/Output: Input or/and Output of Port
  Input: Input port
  Output: Output port
  I/O: Input/output port

- PU/PD: Programmable pull-up/pull-down
  PU: Programmable pull-up is selectable
  PD: Programmable pull-down is selectable

- OD: Programmable open-drain output
  YES: Support
  NO: Non support

- 5VT/3VT: Tolerant
  5VT: 5V-tolerant
  3VT: 3V-tolerant
  N/A: Not available

- SMT/CMOS: Input gate
  SMT: Schmitt trigger input
  CMOS: CMOS input

- Under Reset: Port state under Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

- After Reset: Port state after Reset
  Hi-z: High impedance
  PU: Pull-up
  PD: Pull-down

4.3.1. Port Specifications Table

Table 4.23 Port names, and specifications of Port A, B, C, D

Port Name	Input/Output	PU/PD	OD	5V/3VT	SMT/ CMOS	Under Reset	After Reset
PA0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA1	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PA2	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PA3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PA5	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PA6	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PA7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PB7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PC7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD1	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PD2	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PD3	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PD4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PD7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Table 4.24 Port names, and specifications of Port E, F, G, H

Port Name	Input/Output	PU/PD	OD	5V/3VT	SMT/ CMOS	Under Reset	After Reset
PE0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PE7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF2	I/O	PU/PD	YES	5VT	SMT	Hi-z	Hi-z
PF3	I/O	PU/PD	YES	5VT	SMT	Hi-z	Hi-z
PF4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PF7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG2	I/O	PU/PD	YES	5VT	SMT	Hi-z	Hi-z
PG3	I/O	PU/PD	YES	5VT	SMT	Hi-z	Hi-z
PG4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PG7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH3	I/O	PU/PD	YES	N/A	SMT	PU	PU
PH4	I/O	PU/PD	YES	N/A	SMT	PU	PU
PH5	I/O	PU/PD	YES	N/A	SMT	PD	PD
PH6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PH7	I/O	PU/PD	YES	N/A	SMT	PU	PU

Table 4.25 Port names, and specifications of Port J, K, L, M

Port Name	Input/Output	PU/PD	OD	5V/3VT	SMT/ CMOS	Under Reset	After Reset
PJ0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PJ7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PK2	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PK3	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PK4	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PK5	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PK6	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PK7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL1	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PL2	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PL3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PL7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM1	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PM2	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PM3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PM5	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PM6	I/O	PU/PD	YES	N/A	CMOS	Hi-z	Hi-z
PM7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Table 4.26 Port names, and specifications of Port N, P, R, T

Port Name	Input/Output	PU/PD	OD	5V/3VT	SMT/ CMOS	Under Reset	After Reset
PN0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PN7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PP7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PR7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT2	I/O	PU/PD	YES	3VT	SMT	Hi-z	Hi-z
PT3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PT5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z

Table 4.27 Port names, and specifications of Port U, V, W, Y

Port Name	Input/Output	PU/PD	OD	5V/3VT	SMT/ CMOS	Under Reset	After Reset
PU0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PU7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PV7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW0	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW1	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW2	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW3	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW4	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW5	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW6	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PW7	I/O	PU/PD	YES	N/A	SMT	Hi-z	Hi-z
PY0	Input	PU/PD	N/A	N/A	SMT	Hi-z	Hi-z
PY1	Input	PU/PD	N/A	N/A	SMT	Hi-z	Hi-z
PY2	Input	PU/PD	N/A	N/A	SMT	Hi-z	Hi-z
PY3	Input	PU/PD	N/A	N/A	SMT	Hi-z	Hi-z
PY4	Output	PU/PD	YES	N/A	SMT	Hi-z(Note)	Hi-z

Note: This pin is shared by BOOT_N pin. When RESET_N pin is “0”, PU (Pull-up resistor connection) is active. If RESET_N =1 and the internal reset is asserted, this pin is in Hi-z state.

5. Functional Description and Operation Description

For the details of the functions, refer to Reference manuals.

5.1. Reference Manuals

For more information on product of TMPM4G Group (1), please refer to Reference Manuals below;

Table 5.1 Reference Manuals for TMPM4G Group (1)

Reference Manual	IP Symbol	Category
Input/Output Ports (TMPM4G Group(1))	PORT-M4G(1)	System
Memory Map (TMPM4G Group(1))	MMAP-M4G(1)	System
Exception (TMPM4G Group(1))	EXCEPT-M4G(1)	System
Clock Control and Operation Mode (TMPM4G Group(1))	CG-M4G(1)-C	System
Product Information (TMPM4G Group(1))	PINFO-M4G(1)	System
Power Supply and Reset Operation (TMPM4G Group(1))	RESET-M4G(1)	System
Flash Memory (Code Flash 1.5MB/1.0MB/768KB/512KB Data Flash 32KB)	FLASH15MHD32-A	Peripheral
Trimming Circuit	TRM-A	Peripheral
Oscillation Frequency Detector	OFD-A	Peripheral
Voltage Detection Circuit	LVD-C	Peripheral
Digital Noise Filter Circuit	DNF-A	Peripheral
Debug Interface	DEBUG-A	Peripheral
Non Break Debug Interface	NBDIF-A	Peripheral
Interval Sensor Detection Circuit	ISD-A	Peripheral
Multi-Function DMA Controller	MDMAC-A	Peripheral
High Speed DMA Controller	HDMAC-A	Peripheral
External Bus Interface	EBIF-A	Peripheral
Serial Memory Interface	SMIF-A	Peripheral
Asynchronous Serial Communication Circuit	UART-C	Peripheral
Full Universal Asynchronous Receiver Transmitter Circuit	FUART-B	Peripheral
Serial Peripheral Interface	TSPI-C	Peripheral
I^2C Interface	I2C-B	Peripheral
Consumer Electronics Control Circuit	CEC-A	Peripheral
12-bit Analog to Digital Converter	ADC-C	Peripheral
8-bit Digital to Analog Converter	DAC-A	Peripheral
Advanced Programmable Motor Control Circuit	A-PMD-C	Peripheral
32-bit Timer Event Counter	T32A-B	Peripheral
Long Term Timer	LTTMR-A	Peripheral
Real Time Clock	RTC-A	Peripheral
Clock Selective Watchdog Timer	SIWDT-A	Peripheral
Remote Control Signal Preprocessor	RMC-B	Peripheral
Boundary Scan	BSC-A	Peripheral

5.2. Processor Core

TMPM4G group(1) incorporates a high-performance 32-bit processor core (Arm Cortex-M4 (with FPU)).

For the operation of the processor core, refer to the Arm documentation set of the Arm "Cortex-M" series processors. This section explains the product-specific information.

5.2.1. Core Information

The Cortex-M4(with FPU) core revision used in TMPM4G group(1) is shown as below:
For details of the CPU core and the architecture, refer to the Arm documentation in the following URL:
http: //infocenter.arm.com/help/index.jsp

Table 5.2 Core revision

Group name	Core revision
TMPM4G(1)	r0p1

5.2.2. Configurable Options

In the Cortex-M4(with FPU) core, some blocks can be selected to implement. The following table shows the configurations of TMPM4G group(1).

Table 5.3 Configurable options and their implementations

Configurable option	Implementation
FWB	Literal comparator: 2 Instruction comparator: 6
DWT	Comparator: 4
ITM	Available
MPU	Available
ETM	Available
AHB-AP	Available
AHB trace macro cell interface	Not available
TPIU	Available
WIC	Not available
Debug port	JTAG/Serial wire
Bit band	Available
Sequential control of AHB	Not available

5.3. Clock Control and Operation Mode (CG)

The CG selects a clock gear ratio and the prescaler clock, or warm up time of the oscillator.

There are NORMAL mode and low power consumption mode as operation modes. Power consumption can be reduced by mode transition.

The system clock consists of “High speed system clock” and “Middle speed system clock”. The former is a high speed oscillation clock and the latter is generated by dividing High speed system clock.

The outline of the clock control circuit is as follows:

- Internal high speed oscillation circuit 1: 10MHz
- Internal high speed oscillation circuit 2: 10MHz
- Selectable from the external high speed oscillation circuit or internal high speed oscillation circuit.
- PLL (Clock Multiplication Circuit):

  Capable of 160 MHz output by changing the multiplication ratio according to the frequency of the high speed oscillation circuit
- Clock gear:

  The high speed clock can be divided by 1/1, 1/2, 1/4, 1/8, or 1/16 and the clock is used as the system clock (fsys).
- Low power consumption mode:

  IDLE: Only the CPU is stopped in this mode. Each peripheral circuit can enable or disable operation in the IDLE mode.

  STOP1: Except some peripheral circuits, all the internal circuits including the internal oscillator are brought to a stop in STOP1 mode. The low frequency oscillator can be supplied to RTC, RMC CEC and ISD by the corresponding setting. LTTMR can be worked by enabling of IHOSC2.

  STOP2: This mode halts voltage supply, retaining some peripheral circuits operation. The low frequency clock can be supplied to RTC, RMC, CEC and ISD by the corresponding setting. LTTMR can be worked by enabling of IHOSC2.

5.4. Flash Memory (Code FLASH, Data FLASH)

The cord flash stores instruction code, and CPU reads instruction code and executes.

The code flash and data flash store data, and even if a power supply is off, data can be kept.

It has the dual mode that possible to write and erase a data flash while executing an order by a code flash, and it's also possible to continue executing an application program during writing or erasing data flash.

While saving the data to the data flash, it can continue running the application program on the code flash.

It has protection function which prohibits write or erase by the block unit and it has the security function which prohibits the reading of the program code by the 3rd person.

5.5. Oscillation Circuit

External High Speed Oscillator (EHOSC): Connect crystal resonator or ceramic resonator to terminals. Use clock source for System clock.

External Low Speed Oscillator (ELOSC): Connect crystal resonator (32.768 kHz) to terminals. Use clock source for Real Time Clock or Power consumption mode.

Internal High Speed Oscillator 1(IHOSC1): Oscillation frequency is 10MHz. Use clock source for System clock.

Internal High Speed Oscillator 2(IHOSC2): Oscillation frequency is 10MHz. Use clock source for OFD, SIWDT and LTTMR.

The built-in oscillators in TMPM4G group(1) are shown in the following table.

Table 5.4 Built-in Oscillator

	M4G9	M4G8	M4G7	M4G6
EHOSC	✓	✓	✓	✓
ELOSC	✓	✓	✓	✓
IHOSC1	✓	✓	✓	✓
IHOSC2	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.6. Trimming Circuit (TRM)

The trimming function can adjust frequency of the internal high speed oscillator1 (IHOSC1).

The built-in trimming circuit is integrated in TMPM4G group(1) as shown in the following table.

Table 5.5 Built-in TRM

	M4G9	M4G8	M4G7	M4G6
TRM	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.7. Oscillation Frequency Detector (OFD)

The oscillation frequency detection circuit (OFD) is a function that detects an abnormal state of the clock. It measures the external high speed oscillation (f_{EHOSC}) or high speed clock (fc) based on the internal reference clock (f_{IHOSC2}). If an oscillation or clock frequency is out of the specified range, a reset signal occurs.

The upper limit and the lower limit of detection frequency ranges can be specified respectively.

Table 5.6 Built-in OFD

	M4G9	M4G8	M4G7	M4G6
OFD	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.8. Voltage Detection Circuit (LVD)

The LVD is a peripheral function that detects whether a power supply voltage is lower or higher than the preset voltage. When a low voltage or higher voltage than the preset voltage is detected, the LVD generates an interrupt request or reset the MCU.

Setting voltage can be chosen from seven kinds. LVD is set to enable from the Reset state at the Power-on.

Table 5.7 Built-in LVD

	M4G9	M4G8	M4G7	M4G6
LVD	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.9. Digital Noise Filter Circuit (DNF)

The digital noise canceler circuit can eliminate noise of input signals from external interrupt pins at the certain range. The noise of the High level / Low level input of the external interrupt signal INTx is removed. The noise rejection of width can be selected from among 0.0875 to 5.6 μs (fc=160MHz) for each interrupt input pin independently.

TMPM4G group(1) can have 17 to 32 external interrupt input pins.

Table 5.8 Number of External interrupt pins (Built-in DNF)

	M4G9	M4G8	M4G7	M4G6
External interrupt pins	32	25	21	17

5.10. Debug Interface (DEBUG)

TMPM4G Group (1) contain Interface for connect debug tool, which is the Serial Wire Debug Port (SWCLK, SWDIO) and the JTAG Debug Port (TDI, TDO, TMS, TCK, TRST_N). These are connected with the Debug tool and used for program development. And also it contain the trace clock (TRACECLK) and data output (TRACEDATA0to3) to reduce the Debug Process.

TMPM4G group(1) supports Serial Wire Debug Port, JTAG Debug Port and Trace outputs.

Table 5.9 Built-in Debug Interface

	Port	M4G9	M4G8	M4G7	M4G6
TMS/SWDIO	PH4	✓	✓	✓	✓
TCK/SWCLK	PH5	✓	✓	✓	✓
TDO/SWV	PH6	✓	✓	✓	✓
TDI	PH3	✓	✓	✓	✓
TRST_N	PH7	✓	✓	✓	✓
TRACECLK	PG6	✓	✓	✓	✓
TRACEDATA0	PG7	✓	✓	✓	✓
TRACEDATA1	PH0	✓	✓	✓	✓
TRACEDATA2	PH1	✓	✓	✓	✓
TRACEDATA3	PH2	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.11. Non Break Debug Interface(NBDIF)

Connecting debug tools supporting NBD interface can provide RAM monitor function.

Table 5.10 Built-in NBDIF

	M4G9	M4G8	M4G7	M4G6
NBDSYNC	✓	✓	✓	✓
NBDCLK	✓	✓	✓	✓
NBDDATA0	✓	✓	✓	✓
NBDDATA1	✓	✓	✓	✓
NBDDATA2	✓	✓	✓	✓
NBDDATA3	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.12. Interval Sensor Detection Circuit(ISD)

ISD can generate an interrupt when the value of the sensor input changes (High level, Low level, High to Low transition, and Low to High transition). And the low power consumption mode can be released by the input signal detection interrupt.

Table 5.11 Built-in ISD

UNIT	M4G9	M4G8	M4G7	M4G6
unit A	✓	✓	✓	✓
unit B	✓	✓	✓	-
unit C	✓	-	-	-

Note: ✓: Available, -: N/A

5.13. DMA Controller

5.13.1. Multi-Function DMA Controller (MDMAC)

MDMAC transfers data from peripheral function to memory, from memory to peripheral function and between memories. These operations are performed separately from the CPU control. The CPU load can be greatly reduced by using it. The transfer count can be set infinitely by using chain transfer.

TMPM4G group(1) has one unit of MDMAC. There are 32 channel requests per unit. The inputs of channels 0 to 31 can be startup factors which is assigned to TSPI, UART, FUART, I^2C, T32A, ADC, A-PMD, external trigger input via the trigger selector (TRGSEL).

Table 5.12 Built-in MDMAC

UNIT	M4G9	M4G8	M4G7	M4G6
unit A	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.13.2. High Speed DMA Controller (HDMAC)

HDMAC transfers data from peripheral function to memory, from memory to peripheral function and between memories. High speed transfer of up to 4095 counts is possible.These operations are performed separately from the CPU control. The CPU load can be greatly reduced by using it.

TMPM4G group(1) has two units of HDMAC. SMIF,TSPI,External trigger pin can be startup factors of HDMAC.

Table 5.13 Built-in HDMAC

UNIT	M4G9	M4G8	M4G7	M4G6
unit A	✓	✓	✓	✓
unit B	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.14. External Bus Interface (EBIF)

EBIF (External bus interface) connects external memories, external I/O's, and others.
Two modes (Separate bus mode and Multiplex bus mode) are available and EBIF supports 64 MB access space (16 MB × 4 channels) at maximum. The data bus width can be set to 8 bits or 16 bits per channel.

Table 5.14 Built-in EBIF

	M4G9	M4G8	M4G7	M4G6
EBIF	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.15. Serial Memory Interface (SMIF)

SMIF is communication function that can be high speed serial transfer with external devices such as SPI Flash. Up to 2 devices can be connected to one channel. A direct access and a register access are supported. The Single I/O, Dual I/O read and Quad I/O read are supported by communication interface of SPI(Mode 0).

Table 5.15 Built-in SMIF

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.16. Asynchronous Serial Communication Circuit

5.16.1. Asynchronous Serial Communication Circuit (UART)

The UART is asynchronous serial communication function. It can choose the data length of 7, 8 or 9bits, parity existence, and a STOP bit length function. Moreover, selection of the MSB first / LSB first and reversal of data polarity can be performed and Terminal exchanged of TXD/RXD can be performed in a Port setting.

The FIFO buffer supports data communication on 8 stage at transmission; and on 8 stage at reception.

The telecommunication control by CTS/RTS are supported.

Table 5.16 Built-in UART

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓
Channel 3	✓	✓	✓	-
Channel 4	✓	✓	-	-
Channel 5	✓	-	-	-

Note1: ✓: Available, -: N/A

Note2: External pin are not same by product. Please refer to section “2 Pin Assignment”.

5.16.2. Full Universal Asynchronous Receiver Transmitter Circuit (FUART)

FUART is asynchronous serial communication function. It can choose a data length of 5, 6, 7, or 8 bits, parity existence, and a STOP bit length.

The FIFO buffer contains data communication on 32 stage at transmission and on 32 stage at reception. The communication control by CTS/RTS, IrDA 1.0 function, and DMA are supported.

Table 5.17 Built-in FUART

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	–	–

Note1: ✓: Available, -: N/A

Note2: External pin are not same by product. Please refer to section “2 Pin Assignment”.

5.17. Serial Peripheral Interface (TSPI)

The TSPI supports two communication methods and enables to perform serial communication between other devices at high speed. The SPI bus type, which uses a CS (Chip Select) signal at communications, and SIO bus type, which does not use a CS signal at communications can be selected.

The data length can be changed from 7 bits (with a parity bit) to 32 bits (without a parity bit) in the unit of one bit. There are an 8 stage 16-bit FIFO for reception and transmission, each. The TSPI supports the master and slave communications.

Table 5.18 Built-in TSPI

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓
Channel 5	✓	✓	✓	-
Channel 6	✓	✓	-	-
Channel 7	✓	✓	-	-
Channel 8	✓	-	-	-

Note1: ✓: Available, -: N/A

Note2: External pin are not same by product. Please refer to section “2 Pin Assignment”.

5.18. I²C Interface (I²C)

I²C is two-wire bi-directional serial communications between Master and Slave device. The mode in which two or more masters can exist on the same bus called a multi-master is supported. It supports Standard mode (Max 100kbps), Fast mode (Max 400kbps).

Table 5.19 Built-in I²C

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓
Channel 3	✓	✓	-	-
Channel 4	✓	✓	-	-

Note: ✓: Available, -: N/A

5.19. Consumer Electronics Control Circuit (CEC)

CEC (Consumer Electronics Control) transfers data compliant with HDMI standard Version 1.3a.

Table 5.20 Built-in CEC

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.20. 8-bit Digital to Analog Converter (DAC)

The DAC is an R-2R type 8-bit digital to analog converter that can output the specified voltage. A buffer amplifier is not incorporated.

Table 5.21 Built-in DAC

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.21. 12-bit Analog to Digital Converter (ADC)

The ADC is a successive-approximation analog to digital converter. It supports maximum 24 analog inputs. The combination of conversion result register and analog input can be programmed for each AD conversion start factor, and it can be selected the highest startup factor / general purpose startup factor or sampling period. A startup trigger for ADC can be selected from software or peripheral functions (timer/event counter outputs, port inputs).

The monitor function is also available and it can generate an interrupt request when the compare conditions are matched.

Table 5.22 Built-in ADC

UNIT	M4G9	M4G8	M4G7	M4G6
unit A	✓	✓	✓	✓

Note: ✓: Available, -: N/A

Table 5.23 Number of analog inputs for ADC

	M4G9	M4G8	M4G7	M4G6
Analog inputs pin count	24	24	20	16

5.22. Advanced Programmable Motor Control Circuit (A-PMD)

The Advanced Programmable Motor control circuit (A-PMD) can control motors easily. It incorporates a three-phase pulse modulation circuit and a dead-time circuit, and easily generates waveforms for motor control.

Table 5.24 Built-in A-PMD

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.23. 32-bit Timer Event Counter (T32A)

The T32A is a timer event counter that can operate as a 32-bit timer or two 16-bit timers. 16-bit Timer or 32-bit Timer can be selected. In 16-bit Timer, the T32A is comprised of Timer A and Timer B incorporating a 16-bit counter respectively. In 32-bit Timer, the T32A operates as Timer C incorporating a 32-bit counter.

The T32A have an interval timer, event counter, input capture, 2-phase counter input, PPG output, Synchronous Start, and Trigger start/stop functions.

Table 5.25 Built-in T32A

Channel	M4G9	M4G8	M4G7	M4G6
Channel 0	✓	✓	✓	✓
Channel 1	✓	✓	✓	✓
Channel 2	✓	✓	✓	✓
Channel 3	✓	✓	✓	✓
Channel 4	✓	✓	✓	✓
Channel 5	✓	✓	✓	✓
Channel 6	✓	✓	✓	✓
Channel 7	✓	✓	✓	✓
Channel 8	✓	✓	✓	✓
Channel 9	✓	✓	✓	✓
Channel 10	✓	✓	✓	✓
Channel 11	✓	✓	✓	✓
Channel 12	✓	✓	✓	✓
Channel 13	✓	✓	✓	✓

Note1: ✓: Available, -: N/A

Note2: External pin are not same by product. Please refer to section “2 Pin Assignment”.

5.24. Long Term Timer (LTTMR)

The long term timer (LTTMR) notifies an interrupt request at a constant period. The period is generated based on the frequency of the internal oscillator 2 (IHOSC2). The interrupt cycle can be generated in the range of 0.1 μs to 6553.5 μs. The output of LTTMR can be used as the source clock of RMC and CEC.

Table 5.26 Built-in LTTMR

Channel	M4G9	M4G8	M4G7	M4G6
LTTMR	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.25. Real Time Clock (RTC)

The RTC is a peripheral function that has a second counter, clock function, and leap year calendar function. It also has the alarm function that generates an interrupt on a specified time and date.

Since the RTC operates on a low speed external oscillation clock, it can operate in low power consumption mode such as IDLE, STOP1 or STOP2 mode. In addition, the MCU can be returned from low power consumption mode by an interrupt request of the RTC.

The RTC easily corrects a gain/loss of the clock caused by an error of low speed oscillation frequency using the clock correction function.

Table 5.27 Built-in RTC

	M4G9	M4G8	M4G7	M4G6
RTC	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.26. Clock Selective Watchdog Timer (SIWDT)

The SIWDT is a peripheral function that detects an overflow of the binary counter and generates an interrupt request or resets the MCU. This state occurs when a binary counter cannot be cleared within the preset detection time.

The count clock can be selected from three clocks: system clock (fsys/4), internal high speed oscillator 1(f_{IHOSC1}), or internal high speed oscillator 2 (f_{IHOSC2}).

It also provides the count-clear window function that can clear the count only for the specified period.

Moreover, change of a register can be forbidden by setting to protected mode.(the count-clear function is possible)

Table 5.28 Built-in SIWDT

	M4G9	M4G8	M4G7	M4G6
SIWDT	✓	✓	✓	✓

Note: ✓: Available, -: N/A

5.27. Remote Control Signal Preprocessor (RMC)

The RMC is a peripheral function that receives signals excluding carrier signal from remote control reception signals. The RMC detects a leader signal to receive 72 bits data in a collective manner. Two data formats can be received: synchronous format and fixed-synchronous phase format.

In addition, it contains a digital noise canceller to avoid external noise. The interval of the leader signals can be also measured using the timer event counter.

Since the RMC operates on a low speed clock, it can operate in low power consumption mode, such as IDLE mode, STOP1 mode or STOP2 mode according to the setting. The MCU can also be returned from low power consumption mode by an interrupt request of the RMC.

Table 5.29 Built-in RMC

Channel	M4G9	M4G8	M4G7	M4G6
Channel0	✓	✓	✓	✓
Channel1	✓	✓	✓	-

Note: ✓: Available, -: N/A

5.28. Boundary Scan (BSC)

A boundary-scan support the on-board Test. The TMPM4G group (1) provides a boundary-scan interface that is compatible with Joint Test Action Group (JTAG) specifications and uses the industry-standard JTAG protocol (IEEE Standard 1149.1・1990 <Includes IEEE Standard 1449.1a・1993>).

Table 5.30 Built-in BSC

	M4G9	M4G8	M4G7	M4G6
Boundary-scan	✓	✓	-	-

Note1: ✓: Available, -: N/A

Note2: It is implemented only VFBGA177 and VFBGA145

6. Equivalent Circuit

Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCXX] series.

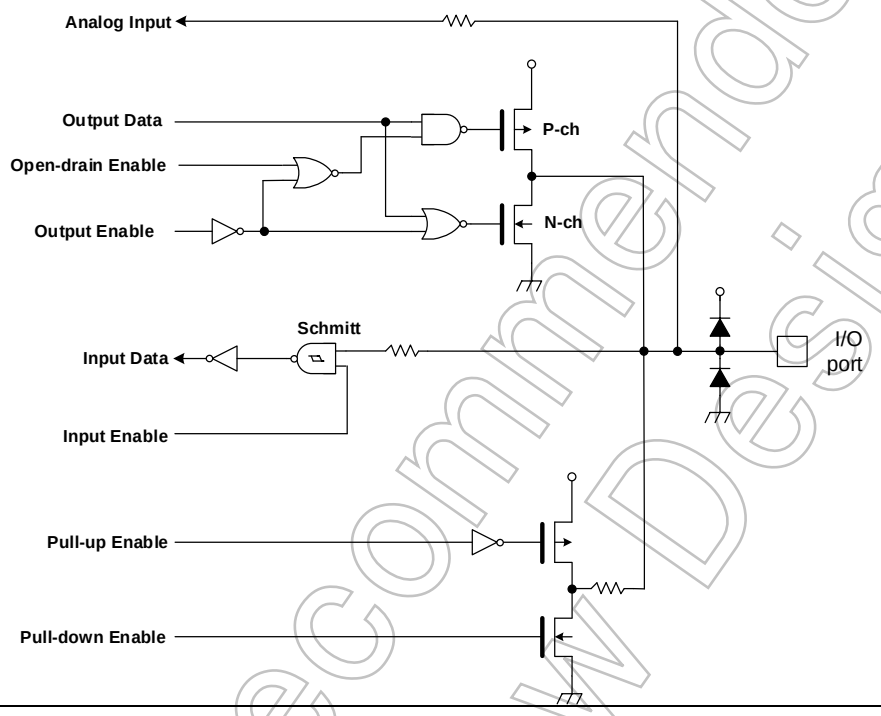
The input protection resistance ranges from several tens of Ω to several hundred Ω Feedback resistor and Damping resistor are shown with a typical value.

Note: The resistance without the statement of the numerical value in the figure shows input protection resistance.

6.1. Port

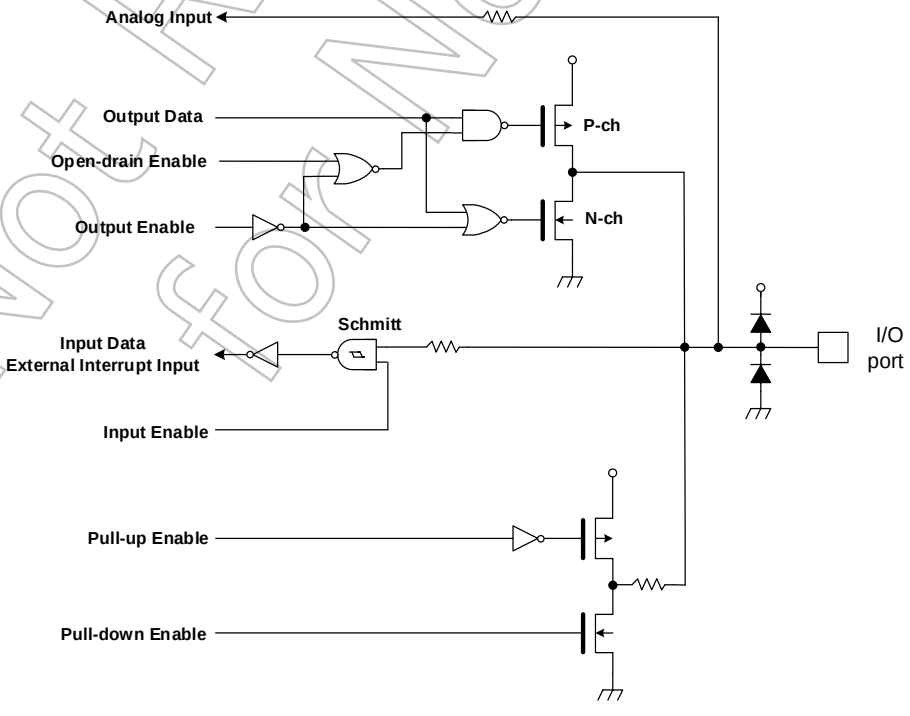
PN0 to PN7, PP0 to PP5, PR0 to PR7

(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input, Analog Input)



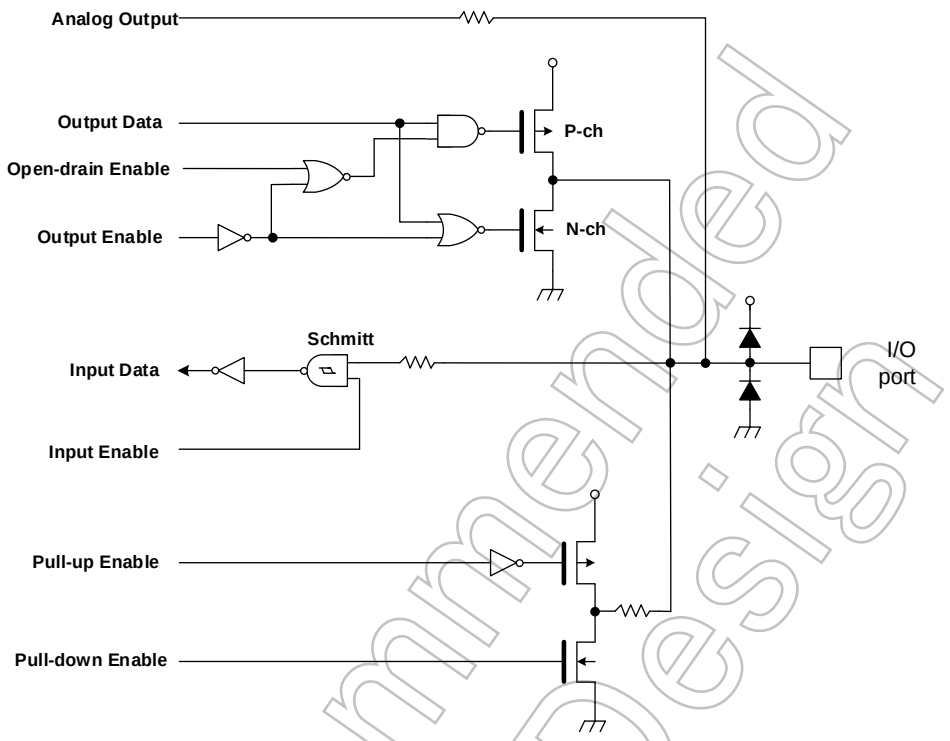
PP6, PP7

(Programmable pull-up/pull-down, Programmable Open-drain output, Schmitt Input, Analog Input, External Interrupt input)



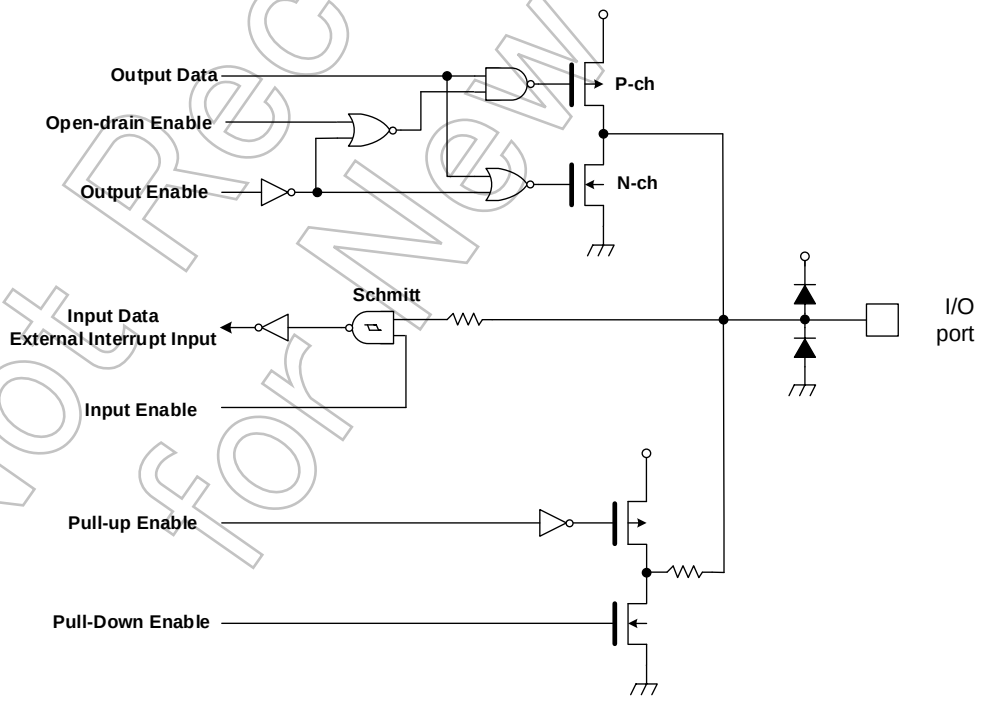
PT0, PT1

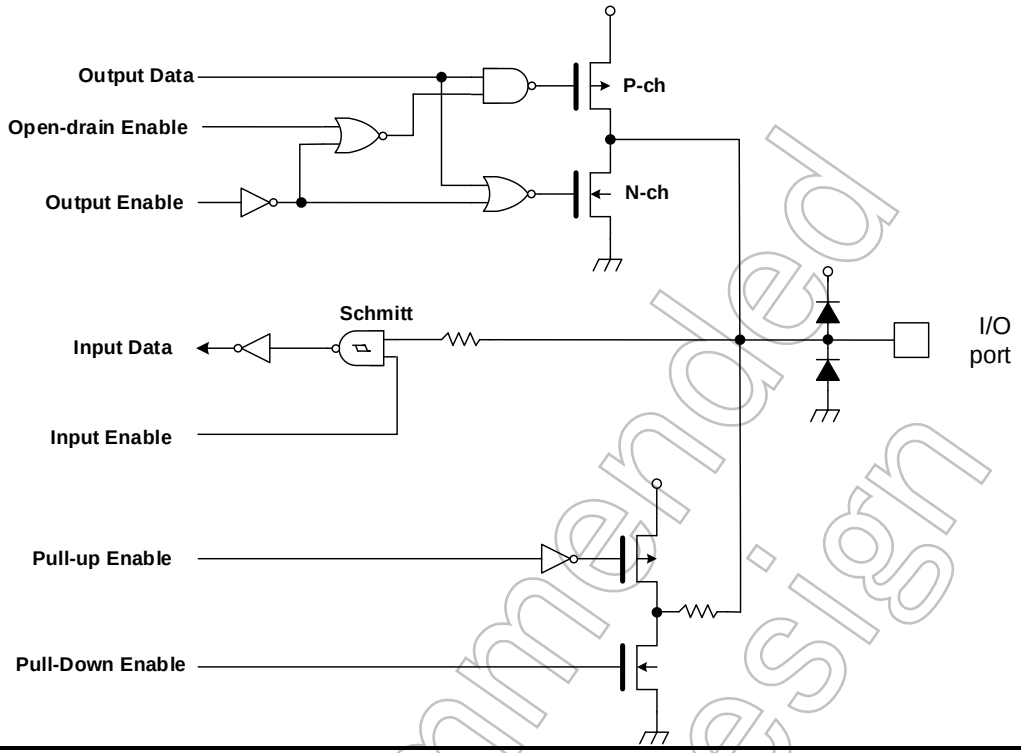
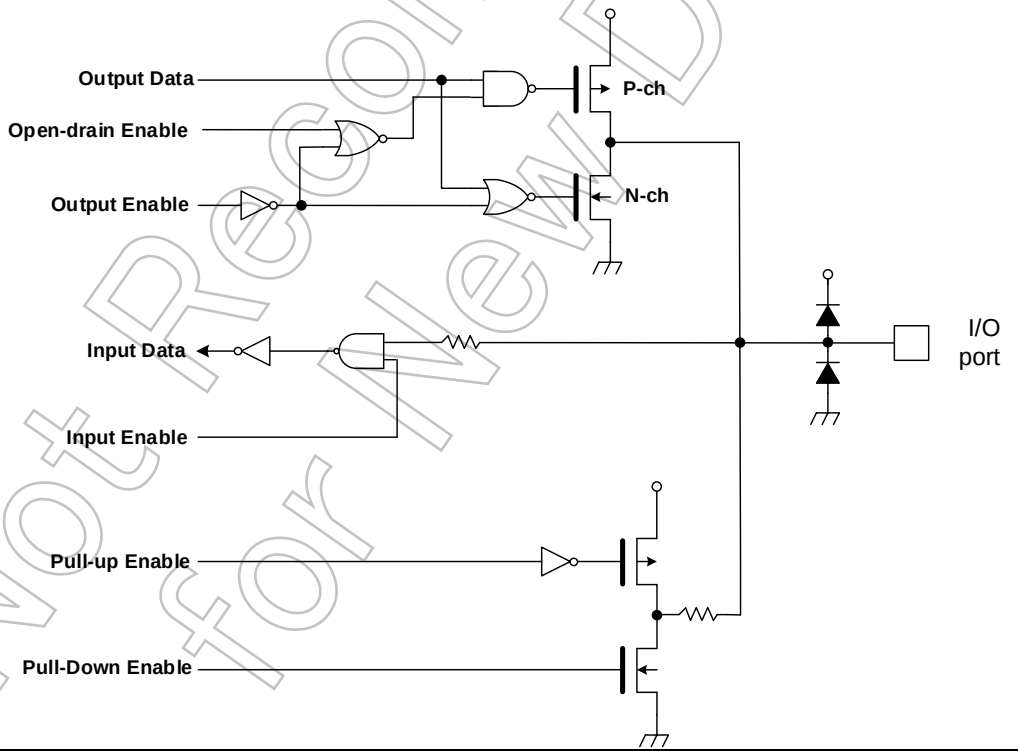
(Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input, Analog Output)

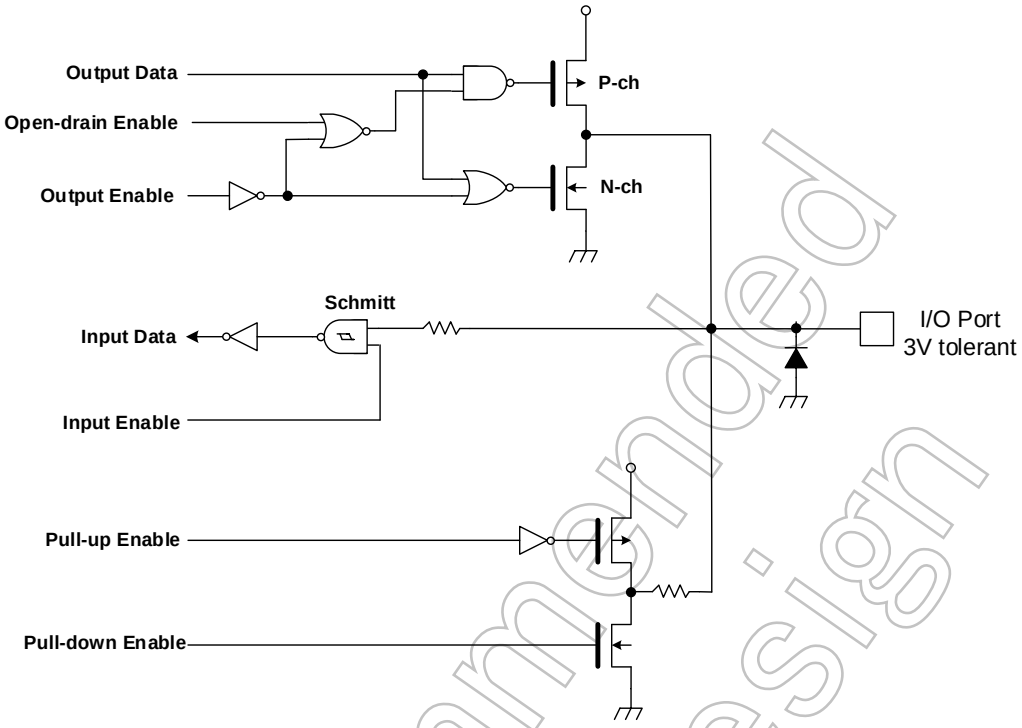
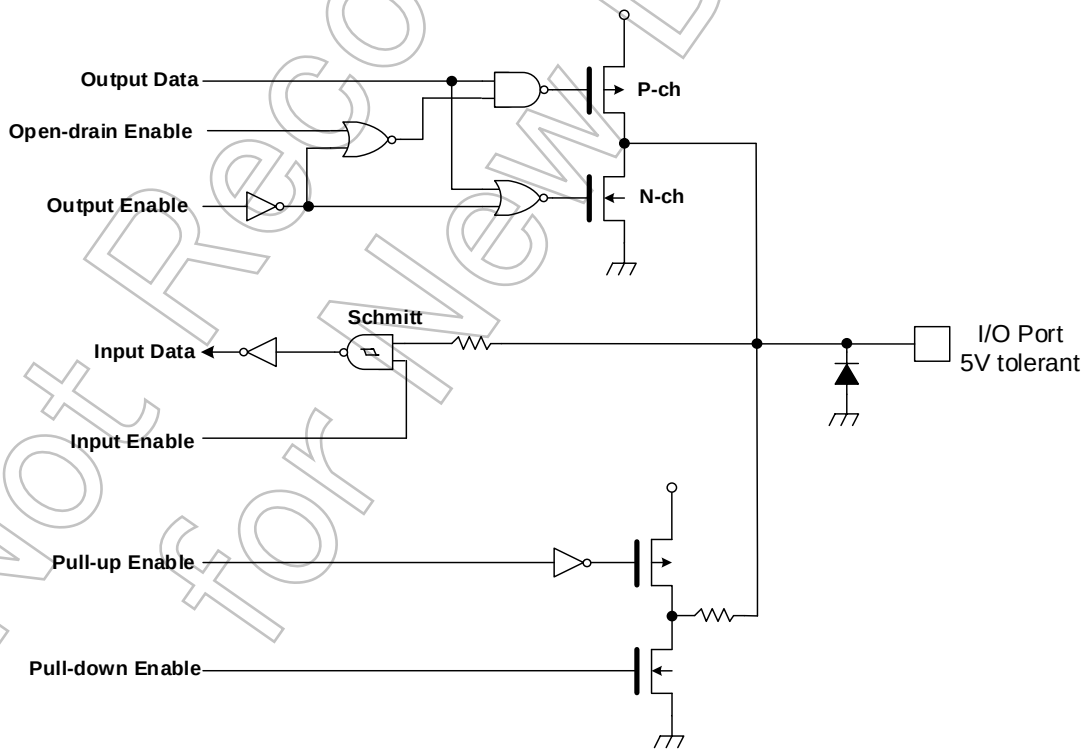


PA3, PA4, PB2 to PB5, PC2 to PC5, PD0, PD4 to PD7, PE0 to PE7, PF1, PF4 to PF6, PG4 to PG7, PH0 to PH7, PJ0 to PJ7, PL3, PL7, PM0, PM7, PU0, PU1, PU6, PU7, PV0 to PV7, PW0 to PW7

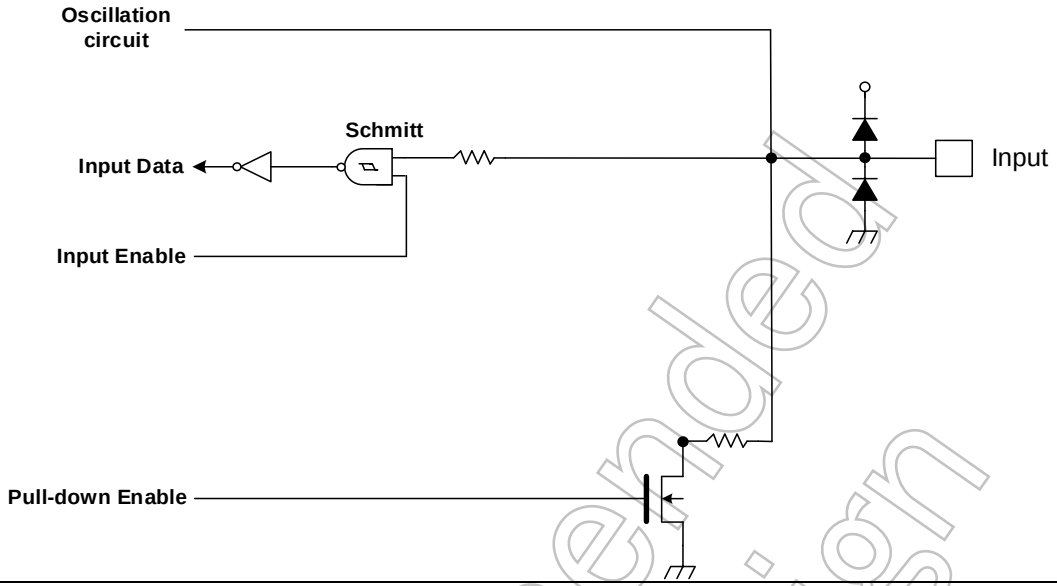
(Programmable Pull-up/Pill-down, Programmable Open-drain Output, Schmitt Input, External Interrupt Input)

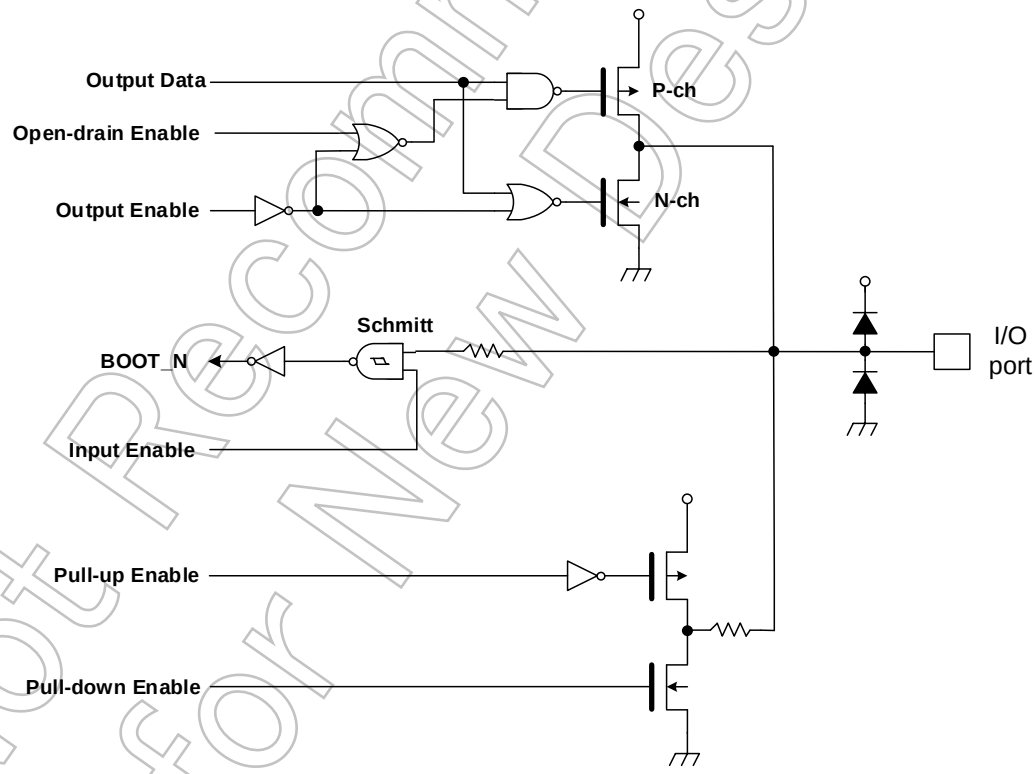


PA0, PA7, PB0, PB1, PB6, PB7, PC0, PC1, PC6, PC7, PF0, PF7, PG0, PG1, PH0 to PH7, PJ0 to PJ7, PK0, PK1, PK7, PL0, PL4 to PL6, PM3, PM4, PT3 to PT5, PU2 to PU5	(Programmable Pull-up/Pill-down, Programmable Open-drain Output, Schmitt Input) 
PA1, PA2, PA5, PA6, PD1 to PD3, PK2 to PK6, PL1, PL2, PM1, PM2, PM5, PM6	(Programmable Pull-up/Pull-down, Programmable Open-drain Output, CMOS Input) 

PT2	**(3V-tolerant, Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input)** 
PF2, PF3, PG2, PG3	**(5V tolerant, Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input)** 

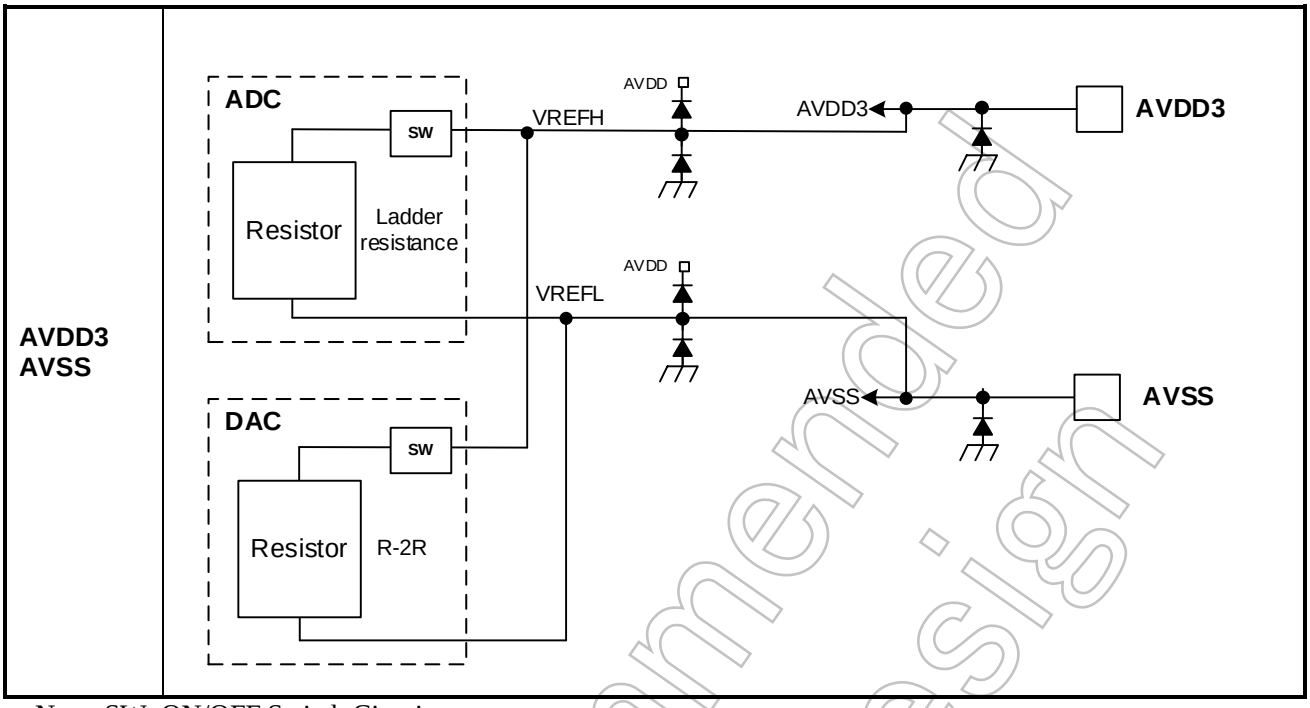
PY0 to PY3	(Programmable Pull-down, Schmitt Input, Oscillation circuit)
PY4/ BOOT_N	(BOOT Input, Programmable Pull-up/Pull-down, Programmable Open-drain Output, Schmitt Input)





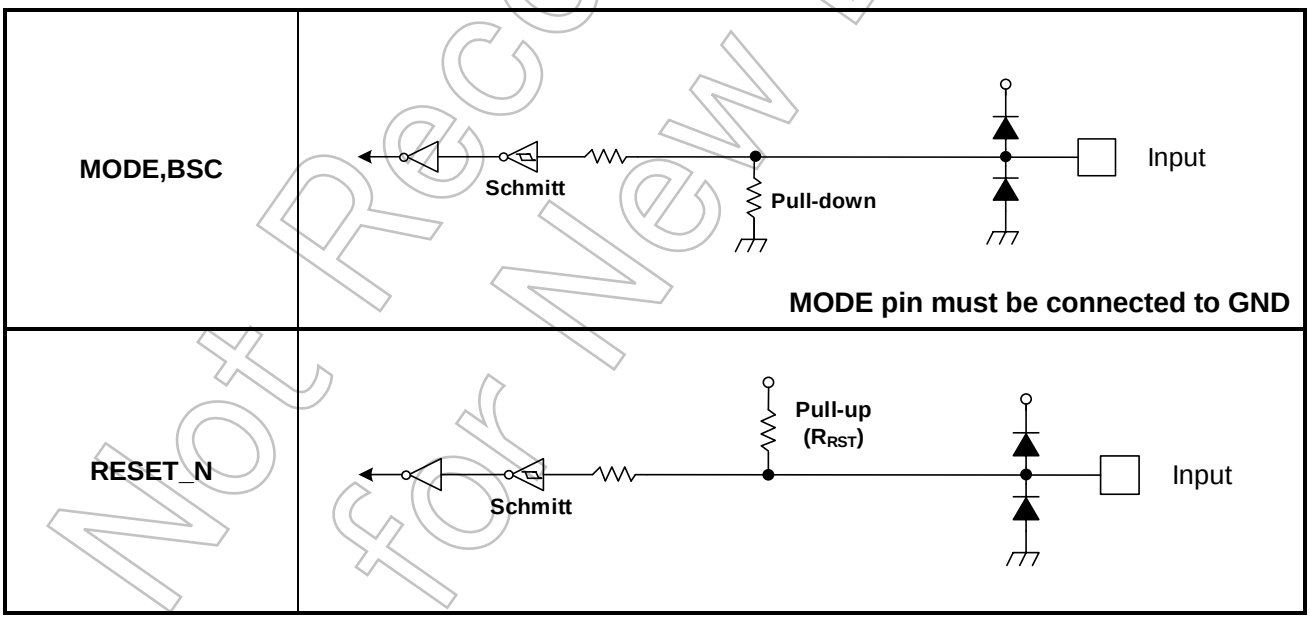
Note: Although, this port is input during pin reset period and POR period, it can be used for output port when use as port.

6.2. Analog Power pin

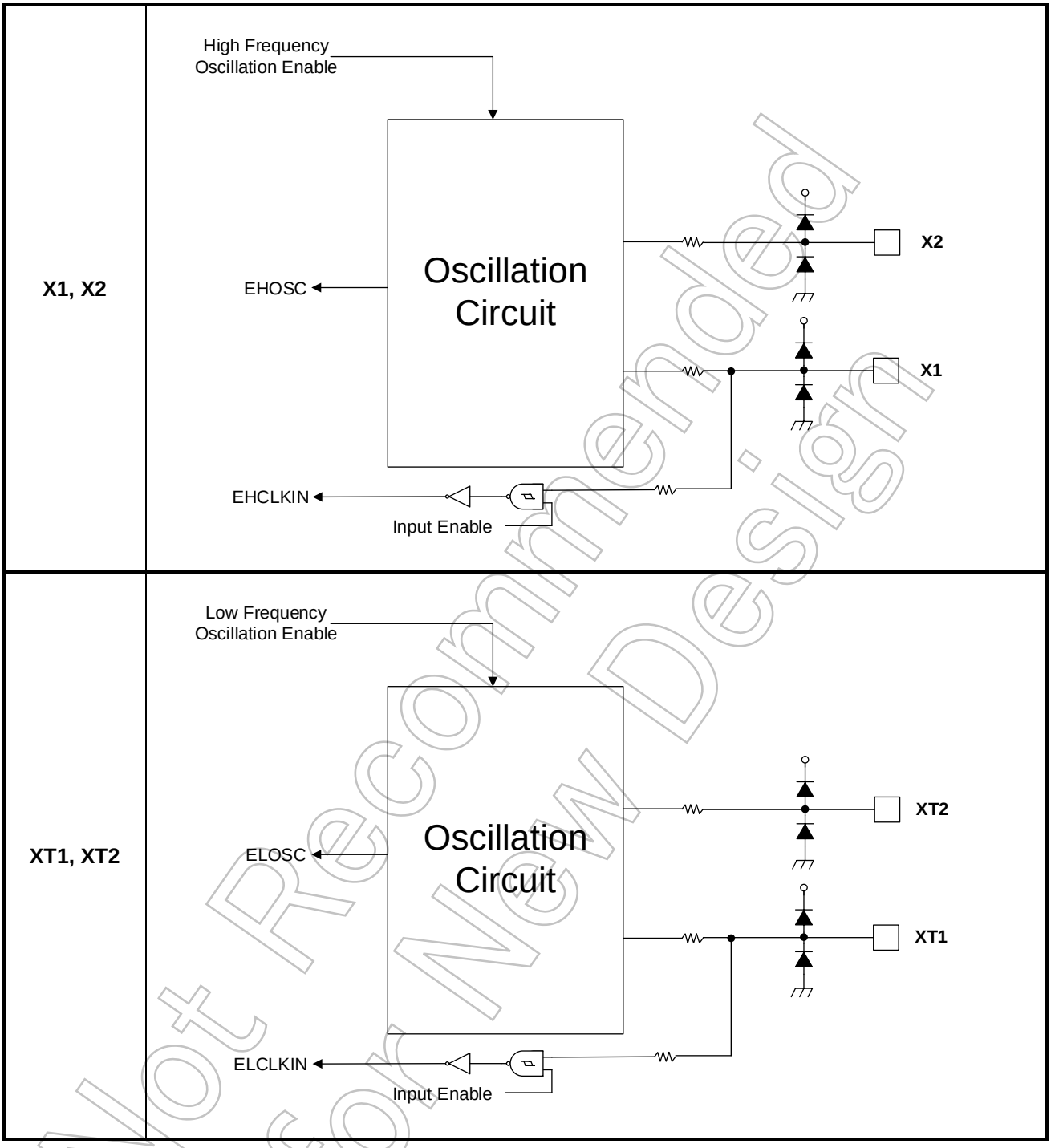


Note: SW: ON/OFF Switch Circuit

6.3. Control Pin



6.4. Clock control



7. Electrical Characteristics

7.1. Absolute Maximum Ratings

Table 7.1 Absolute maximum ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		DVDD3A to DVDD3H	-0.3 to 3.9	V
		AVDD3	-0.3 to 3.9	
Input voltage	PA0 to PA7,PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7,PF0,PF1, PF4 to PF7,PG0, PG1, PG4 to PG7, PH0 to PH7, PJ0 to PJ7,PK0 to PK7, PL0 to PL7,PM0 to PM7, PT3 to PT5, PU0 to PU7,PV0 to PV7,PW0 to PW7, PY0 to PY3, MODE, RESET_N, BOOT_N, BSC	V_{IN1}	-0.3 to DVDD3+0.3(≤ 3.9V) (DVDD3 is generic name for DVDD3A to DVDD3H)	V
	PN0 to PN7,PP0 to PP7, PR0 to PR7,PT0,PT1	V_{IN2}	-0.3 to AVDD3+0.3(≤ 3.9V)	
	PF2,PF3,PG2,PG3	V_{IN3}	-0.3 to 5.5	
	PT2	V_{IN4}	-0.3 to 3.9	
Low level output current	PA0 to PA7,PB0 to PB7,PC0 to PC7, PD0 to PD7,PE0 to PE7,PF0,PF1, PF4 to PF7,PG0,PG1,PG4 to PG7, PH0 to PH7,PJ0 to PJ7,PK0 to PK7, PL0 to PL7,PN0 to PN7,PM0 to PM7, PP0 to PP7,PR0 to PR7,PT0 to PT5, PU0 to PU7,PV0 to PV7,PW0 to PW7, PY4	I_{OL1}	5	mA
	PF2,PF3,PG2,PG3	I_{OL2}	25	
	Total	ΣI_{OL}	50	
High level output current	PA0 to PA7,PB0 to PB7,PC0 to PC7, PD0 to PD7,PE0 to PE7,PF0 to PF7, PG0 to PG7,PH0 to PH7,PJ0 to PJ7, PK0 to PK7,PL0 to PL7,PN0 to PN7, PM0 to PM7,PP0 to PP7,PR0 to PR7, PT0 to PT5,PU0 to PU7,PV0 to PV7, PW0 to PW7,PY4	I_{OH1}	-5	
	Total	ΣI_{OH}	-50	
Power consumption (Ta= 85°C)		PD	600	mW
Soldering temperature		T_{SOLDER}	260	°C
Storage temperature		T_{STG}	-55 to 125	°C
Operational temperature	fsys ≤ 120MHz	T_{OPR1}	-40 to 85	°C
	fsys ≤ 160MHz	T_{OPR2}	-40 to 70	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions. The equipment manufacturer should design so that no Absolute maximum rating value is exceeded with respect to current, voltage, power consumption, temperature, etc. Exposure to conditions beyond those listed above may cause permanent damage to the device or affect device reliability, which could increase potential risks of personal injury due to IC blow up and/or burning.

7.2. DC Electrical Characteristics (1/2)

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Power supply voltage	DVDD3A to DVDD3H AVDD3	VDD	f_{OSC} = 8 to 20MHz f_{sys} =1 to 160MHz (Ta=-40 to 70°C) 1 to 120MHz (Ta=-40 to 85°C) fs = 30 to 34kHz	2.7	-	3.6	V
Low level Input voltage	PA1, PA2,PA5, PA6, PD1 to PD3,PK2 to PK6, PL1, PL2,PM1, PM2, PM5, PM6	V_{IL1}		-0.3	-	DVDD3×0.3	V
	PA0,PA3 to PA4,PA7, PB0 to PB7, PC0 to PC7, PD0,PD4 to PD7, PE0 to PE7,PF0, PF1, PF4 to PF7,PG0, PG1, PG4 to PG7, PH0 to PH7, PJ0 to PJ7,PK0, PK1, PK7, PL0,PL3 to PL7, PM0, PM3, PM4, PM7, PT3 to PT5, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY0 to PY3, MODE, RESET_N,BOOT_N, BSC	V_{IL2}				DVDD3×0.25	
	PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0, PT1	V_{IL3}				AVDD3×0.25	
	PF2, PF3,PG2, PG3, PT2	V_{IL4}				DVDD3×0.3	
High level Input voltage	PA1, PA2,PA5, PA6, PD1 to PD3, PK2 to PK6, PL1, PL2,PM1, PM2, PM5, PM6	V_{IH1}		DVDD3×0.7	-	DVDD3+0.3	V
	PA0, PA3, PA4, PA7, PB0 to PB7, PC0 to PC7, PD0, PD4 to PD7, PE0 to PE7, PF0, PF1, PF4 to PF7, PG0, PG1, PG4 to PG7, PH0 to PH7, PJ0 to PJ7,PK0, PK1, PK7, PL0, PL3 to PL7, PM0, PM3, PM4, PM7, PT3 to PT5, PU0 to PU7, PV0 to PV7, PW0 to PW7, PY0 to PY3, MODE, RESET_N,BOOT_N, BSC	V_{IH2}		DVDD3×0.75		DVDD3+0.3	
	PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0, PT1	V_{IH3}		AVDD3×0.75		AVDD3+0.3	
	PF2, PF3,PG2, PG3, PT2	V_{IH4}		DVDD3×0.7	-	DVDD3+0.3	

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Low level output voltage	PA0 to PA7,PB0 to PB7, PC0 to PC7,PD0 to PD7, PE0 to PE7, PF0, PF1,PF4 to PF7, PG0, PG1,PG6, PG7, PH0 to PH7,PJ0 to PJ7, PK0 to PK7,PL0 to PL7, PM0 to PM7, PN0 to PN7, PP0 to PP7,PR0 to PR7, PT0 to PT2, PT4, PU0 to PU7,PV0 to PV7, PW0 to PW7, PY4	V_{OL1}	DVDD3=AVDD3=2.7V I_{OL} = 1.6mA	-	-	0.4	V
	PG4, PG5, PT3, PT5	V_{OL2}	DVDD3=2.7V I_{OL}=8mA	-	-	0.4	
	PF2, PF3, PG2, PG3	V_{OL3}	DVDD3=2.7V I_{OL}=12mA	-	-	1.0	
High level output voltage	PA0 to PA7,PB0 to PB7, PC0 to PC7,PD0 to PD7, PE0 to PE7, PF0, PF1,PF4 to PF7, PG0, PG1, PG6, PG7, PH0 to PH7, PJ0 to PJ7, PK0 to PK7, PL0 to PL7, PM0 to PM7, PN0 to PN7, PP0 to PP7,PR0 to PR7, PT0 to PT2, PT4, PU0 to PU7,PV0 to PV7, PW0 to PW7, PY4	V_{OH1}	DVDD3=AVDD3=2.7V I_{OH} = -1.6mA	DVDD3-0.4 AVDD3-0.4	-	-	V
	PG4, PG5, PT3, PT5	V_{OH2}	DVDD3=2.7V I_{OH}= -8mA	DVDD3-0.4	-	-	
	PF2, PF3,PG2, PG3	V_{OH3}	DVDD3=2.7V I_{OH}= -1.0mA	DVDD3-0.4	-	1.0	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.
Note2: Typ. value is in Ta = 25 °C, DVDD3 = AVDD3 = 3.3V, unless otherwise noted.
Note3: Apply same voltage to DVDD3 and AVDD3.

DVDD3=AVDD3= 2.7V to 3.6V
DVSS=AVSS=0V
Ta= -40 to 85°C

Parameter		Symbol	Conditions	Min	Typ.	Max	Unit
Input leak current		I_{LI}	0.0V ≤ VIN ≤ DVDD3 0.0V ≤ VIN ≤ AVDD3	-	0.05	±5	μA
Output leak current		I_{LO}	0.2 ≤ VIN ≤ DVDD3-0.2 0.2 ≤ VIN ≤ AVDD3-0.2	-	0.05	±10	
Schmitt trigger Input width		VTH		-	0.8	-	V
Reset pull-up resistor		R_{RST}		25	45	100	kΩ
Programmable pull-up/pull-down resistor	Other than the following	P_{KH}	Pull-up	25	45	100	kΩ
			Pull-down	25	45	100	
	5V tolerant	P_{KH5}	Pull-up	40	70	150	
			Pull-down	40	70	150	
	3V tolerant	P_{KH3}	Pull-up	30	47	200	
			Pull-down	30	47	200	
Pin capacity (except power supply pin)		C_{IO}	fc =1MHz	-	-	10	pF
Low level output current	Per pin PA0 to PA7,PB0 to PB7, PC0 to PC7,PD0 to 7,PE0 to PE7, PF0,PF1, PF4 to PF7,PG0,PG1, PG6,PG7,PH0 to PH7,PJ0 to PJ7, PK0 to PK7,PL0 to PL7, PM0 to PM7, PN0 to PN7, PP0 to PP7, PR0 to PR7, PT0 to PT2, PT4,PU0 to PU7, PV0 to PV7,PW0 to PW7,PY4	I_{OL1}	DVDD3=3V AVDD3=3V	-	-	2	mA
	Per pin PG4, PG5,PT3,PT5	I_{OL2}	DVDD3=3V	-	-	8	
	Per pin PF2, PF3,PG2, PG3	I_{OL3}	DVDD3=3V	-	-	12	
	Total of PA0 to PA7,PB0 to PB7,PT3,PY4	ΣI_{OL1}	DVDD3=3V	-	-	35	
	Total of PD0 to PD7, PE0 to PE7, PJ4 to PJ7, PU0 to PU7	ΣI_{OL2}	DVDD3=3V	-	-	35	
	Total of PC0 to PC7, PF0 to PF7, PJ0 to PJ3, PL6, PL7,PT2	ΣI_{OL3}	DVDD3=3V	-	-	35	
	Total of PG4 to PG7, PH0 to PH7, PM4 to PM7, PV4 to PV7, PW0 to PW3, PT5	ΣI_{OL4}	DVDD3=3V	-	-	35	
	Total of PG0 to PG3, PK0 to PK7, PL0 to PL5, PM0 to PM3, PV0 to PV3, PW4 to PW7,PT4	ΣI_{OL5}	DVDD3=3V	-	-	35	
	Total of PN0 to PN7,PP0 to PP7, PR0 to PR7,PT0, PT1	ΣI_{OL6}	AVDD3=3V	-	-	35	

High level output current	per Pin PA0 to PA7,PB0 to PB7, PC0 to PC7,PD0 to PD7, PE0 to PE7,PF0,PF1, PF4 to PF7,PG0,PG1,PG6,PG7 PH0 to PH7,PJ0 to PJ7,PK0 to PK7, PL0 to PL7,PM0 to PM7, PN0 to PN7,PP0 to PP7, PR0 to PR7, PT0 to PT2 PT4,PU0 to PU7,PV0 to PV7, PW0 to PW7,PY4	I_{OH1}	DVDD3=3V AVDD3=3V	-2	-	-	mA
	per Pin PG4, PG5,PT3,PT5	I_{OH2}	DVDD3=3V	-8	-	-	
	per Pin PF2,PF3,PG2, PG3	I_{OH3}	DVDD3=3V	-12	-	-	
	Total of PA0 to PA7,PB0 to PB7, PT3,PY4	ΣI_{OH1}	DVDD3=3V	-35	-	-	
	Total of PD0 to PD7, PE0 to PE7, PJ4 to PJ7, PU0 to PU7	ΣI_{OH2}	DVDD3=3V	-35	-	-	
	Total of PC0 to PC7, PF0 to PF7, PJ0 to PJ3, PL6, PL7,PT2	ΣI_{OH3}	DVDD3=3V	-35	-	-	
	Total of PG4 to PG7, PH0 to PH7, PM4 to PM7, PV4 to PV7, PW0 to PW3, PT5	ΣI_{OH4}	DVDD3=3V	-35	-	-	
	Total of PG0 to PG3, PK0 to PK7, PL0 to PL5, PM0 to PM3, PV0 to PV3, PW4 to PW7,PT4	ΣI_{OH5}	DVDD3=3V	-35	-	-	
	Total of PN0 to PN7,PP0 to PP7, PR0 to PR7,PT0, PT1	ΣI_{OH6}	AVDD3=3V	-35	-	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.
Note2: Typ. value is in Ta = 25 °C, DVDD3 = AVDD3 = 3.3V, unless otherwise noted.
Note3: Apply same voltage to DVDD3 and AVDD3.

7.3. DC Electrical Characteristics (2/2) (Consumption current)

Item	Products
Code Flash 1.5MB	TMPM4G9F15FG, TMPM4G9F15XBG, TMPM4G8F15FG, TMPM4G8F15XBG
Code Flash 1.0MB or less	TMPM4G9F10FG, TMPM4G9FEFG, TMPM4G9FDFG, TMPM4G9F10XBG, TMPM4G9FEXBG, TMPM4G9FDXBG, TMPM4G8F10FG, TMPM4G8FEFG, TMPM4G8FDFG, TMPM4G8F10XBG, TMPM4G8FEXBG, TMPM4G8FDXBG, TMPM4G7F10FG, TMPM4G7FEFG, TMPM4G7FDFG, TMPM4G6F10FG, TMPM4G6FEFG, TMPM4G6FDFG

For the newest status of each product, Please contact your sales representative.

Ta= -40 to 85°C

Parameter	Symbol	Conditions				Code Flash1.5MB			Code Flash 1.0MB or less			Unit
		Supply voltage	High speed oscillator	Low speed oscillator	Operating condition	Min	Typ.	Max	Min	Typ.	Max	
Normal	I_{DD}	DVDD3= AVDD3= 3.6V	Refer to the “Table 7.2” and “Table 7.3” for detail			-	45	100	-	40	95	mA
			Oscillation	Stop	CPU only		28	93	-	23	80	
IDLE			Refer to “Table 7.2” and “Table 7.3” about Operation conditions			-	13	78	-	9.5	70	
STOP1			Stop	Oscillation	Refer to “Table 7.2” and “Table 7.3” about Operation conditions	-	1.2	65	-	1.2	65	
STOP2						-	13.3	735	-	13.3	735	µA
				Stop		-	9.6	700	−	9.6	700	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.
Note2: Typ. value is in Ta=25 °C, DVDD3=AVDD3=3.3V, unless otherwise noted.
Note3: Apply same voltage to DVDD3 and AVDD3.
Note4: Input pin is fixed level, Output pin is open.

Table 7.2 IDD measurement condition (Pin setting, Oscillation Circuit)

		NORMAL	IDLE	STOP1	STOP2
				LOSC run	LOSC stop
Pin setting	DVDD3= AVDD3=	3.3V(Typ.), 3.6V(max)			
	X1,X2	Oscillator connected (10MHz)			
	XT1,XT2	Oscillator connected (32.768kHz)			
	Input pins	Fixed			
	Output pins	Open			
Operation condition (Oscillation Circuit)	System clock (fsys)	High speed160MHz Middle speed 80MHz		Stop	
	External High speed oscillator (EHOSC)	Oscillation		Stop	
	Internal High speed oscillator 1 (IHOSC1)	Stop			
	PLL	run(16 times)		Stop	
	External Low speed oscillator (ELOSC)	Oscillation			Stop

Table 7.3 IDD measurement condition (CPU, Peripheral)

Peripheral	unit number	NORMAL	IDLE	STOP1	STOP2	
				LOSC oscillation	LOSC oscillation RTC,RMC run	LOSC stop
CPU	1	Run (Dhrystone Ver.2.1)	Stop			
HDMAC	2	Unit A (software startup of ch1, memory to memory transmission) / Unit B (software startup of ch0,memory to peripheral(EBIF) transmission)	Stop			
MDMAC	1	Unit A (software startup, memory to memory transmission)	Stop			
ADC	1	Run (1.15µs, Repeated conversion)	Stop			
DAC	2	Run	Stop			
EBIF	1	Run (Asynchronous separate mode, Internal 4 wait access)	Stop			
T32A	14	All Ch: Run	Stop			
A-PMD	1	Run	Stop			
A-ENC	1	Run	Stop			
RTC	1	Run	Run			Stop
SIWDT	1	Run	Stop			
UART	6	Data Transmission (5Mbps)	Stop			
FUART	2	Data Transmission (2.5Mbps)	Stop			
I^2C	5	Run only clock(fprsck = 5MHz)	Stop			
TSPI	9	Transfer Clock ch0 to ch3: 20MHz ch4 to ch8: 10MHz	Stop			
SMIF	1	Run	Stop			
ISD	3	Run	Run		Stop	
LTTMR	1	Run	Stop			
CEC	1	Run, Transfer	Stop (supply only clock)	Stop		
RMC	2	Run	Run			Stop
LVD	1	Stop	Stop			
OFD	1	Run (OFD reset output disable)	Stop			
PORT	-	Stop	Stop			

fsysm=80MHz
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Power consumption (ADC,DAC run)	I_{AVDD}	AVDD3=3.3V	-	2.0	3.0	mA

7.4. 12-bit AD Converter Characteristics

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage (+)	VREFH		AVDD3	-	AVDD3	V
Analog input voltage	VAIN		AVSS	-	AVDD3 (VREFH)	V
Integral nonlinearity error (INL)	-	2.7V ≤ AVDD3 ≤ 3.6V AIN load resistor ≤ 600Ω AIN load capacity ≥ 0.1μF Conversion time ≥ 1.0μs	-6	-	+6	LSB
Differential nonlinearity error (DNL)			-5	-	+5	
Zero-scale error			-6	-	+6	
Full-scale error			-6	-	+6	
Total errors			-7	-	+7	
Stable time	t_{sta}	***[ADAMOD0]***<DACON>= 1 is set	3	-	-	μs
Conversion time	t_{conv}	2.7V ≤ AVDD3 ≤ 3.6V	1.0	-	5.0	μs

7.5. 8-bit DA Converter Characteristics

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog reference voltage(+)	VREFH		AVDD3	-	AVDD3	V
Integral nonlinearity error(INL)	-	2.7V ≤ AVDD3 ≤ 3.6V Rload= 10MΩ	-2	-	+2	LSB
Differential nonlinearity error(DNL)			-1	-	+1	
Total errors			-2	-	+2	
Stable time	t_{sta}	Cload = 20pF	4.5	-	-	μs

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.
Note2: Typ. value is in Ta=25 °C, DVDD3=AVDD3=3.3V, unless otherwise noted.
Note3: 1LSB = (AVDD5(VREFH) - AVSS(VREFL)) / 256 [V]
Note4: This is the characteristic in case only DA converter is operating.
Note5: When using DAC0 as the reference voltage of Comparator, DAC0 pin should be open.

7.6. Characteristics of Internal processing at RESET

DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Internal Initialized time	t_{IINIT}	Power-On	-	-	2.4	ms
		STOP2 Release by RESET with RESET_N	-	-	1.0	
		STOP2 Release by Interrupt	-	-	0.55	
Internal processing time for Reset	t_{IRST}		0.13	-	0.21	
Pull-up enable time of BOOT_N pin	t_{pup}		-	-	1.5	
Waiting time till CPU running	t_{CPUWT}	Cold Reset	12	-	15	µs
		Warm Reset	97	-	153	
Power on rising gradient	V_{PON}		0.01	-	100	mV/µs

7.7. Characteristics of Power on Reset

DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{PREL}	Power-up	2.05	2.15	2.25	V
	V_{PDET}	Power-down	2.0	2.1	2.2	
Detection pulse width	T_{PDET}		200	-	-	µs

7.8. Characteristics of Voltage Detection Circuit

DVDD3 = AVDD3 = 2.7V to 3.6V
DVSS = AVSS = 0V
Ta= -40 to 85°C

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Detection voltage	V_{LVL0}	Power-up	2.45	2.55	2.65	V
		Power-down	2.4	2.5	2.6	
	V_{LVL1}	Power-up	2.55	2.65	2.75	V
		Power-down	2.5	2.6	2.7	
	V_{LVL2}	Power-up	2.65	2.75	2.85	V
		Power-down	2.6	2.7	2.8	
	V_{LVL3}	Power-up	2.75	2.85	2.95	V
		Power-down	2.7	2.8	2.9	
	V_{LVL4}	Power-up	2.85	2.95	3.05	V
		Power-down	2.8	2.9	3.0	
	V_{LVL5}	Power-up	2.95	3.05	3.15	V
		Power-down	2.9	3.0	3.1	
	V_{LVL6}	Power-up	3.05	3.15	3.25	V
		Power-down	3.0	3.10	3.2	
Detection response time	t_{VDDT1}	Power-up	-	-	200	µs
Detection Release time	t_{VDDT2}	Power-down	-	-	200	
setup time	t_{LVDEN}		-	-	50	
Detection Minimum pulse width	t_{LVDPW}		200	-	-	

7.9. AC Electrical Characteristics

7.9.1. Serial Peripheral Interface (TSPI)

7.9.1.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD3=AVDD3=2.7V to 3.6V
- Ta = -40 to 85°C(fsys≤120MHz), Ta= -40 to 70°C (fsys≤160MHz)
- Output level: High = 0.8×DVDD3, Low = 0.2×DVDD3
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.9.1.2. AC Electrical Characteristics

"T" indicates an operation clock cycle of the TSPI. This operation clock has the same cycle of the system clock (fsys). This cycle depends on the clock gear setting.

The number of cycles can be 1 to 16. It is specified with TSPIxSCK. The value of k1 is specified with ***[TSPIxFMTR0]***<CSSCKDL[3:0]>; the value of k2 is specified with ***[TSPIxFMTR0]***<SCKCSDL[3:0]>. These values are 1 to 16.

(1) Master mode

k1=k2=1

Parameter	Symbol	Equation		fsysh = 100MHz (Note2)		fsys = 80MHz (Note3)		Unit
				ch0-3		ch4-8		
		Min	Max	Min	Max	Min	Max	
TSPIxSCK output frequency (Note1)	f_{CYC}	-	ch0-3: 25	-	25	-	-	MHz
			ch4-8: 10	-	-	-	10	
TSPIxSCK output cycle	t_{CYC}	-	-	40	-	100	-	ns
TSPIxSCK low level output pulse width	t_{WL}	(t_{CYC}/2)-10	-	10	-	40	-	
TSPIxSCK high level output pulse width	t_{WH}	(t_{CYC}/2)-10	-	10	-	40	-	
TSPIxCSn output ← TSPIxSCK rise/fall time	t_{CSUM}	(t_{CYC}×k1)-15	ch0-3: (t_{CYC}×k1)+9	25	49	-	-	
			ch4-8: (t_{CYC}×k1)+13	-	-	85	113	
TSPIxSCK rise/fall time → TSPIxCSn hold time	t_{CHD}	ch0-3: (t_{CYC}×k2)-10	-	30	-	-	-	
		ch4-8: (t_{CYC}×k2)-15		-	-	85	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	ch0-3: 20-2xT:	-	0	-	-	-	
		ch4-8: 30-2xT:		-	-	5	-	
TSPIxSCK rise/fall time → TSPIxRXD hold time	t_{DHD}	2xT	-	20	-	25	-	
TSPIxSCK rise/fall time → TSPIxTXD hold time	t_{ODLY1}	ch0-3: -7	-	-7	-	-	-	
		ch4-8: -10		-	-	-10	-	
TSPIxSCK rise/fall time → TSPIxTXD delay time	t_{ODLY2}	-	ch0-3: 7	-	7	-	-	
			ch4-8: 13	-	-	-	13	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	ch0-3: (t_{CYC}×(k1-0.5))-20	(t_{CYC}×(k1-0.5))+9	0	29	-	-	
		ch4-8: (t_{CYC}×(k1-0.5))-50		-	-	0	59	

Note1: The output frequency is determined by the setting value of ***[TSPIxBR]***<BRCK><BRS>. Please set the

output frequency within the range not exceeding the Max value of the Equation.

Note2: Although the maximum frequency of fsysh is 160 MHz, it is described as an example of fsysh = 100 MHz so as to show of outputting the maximum frequency (25 MHz) of TSPIxSCK

Note3: ch4 and ch5 is shown fsysh(160MHz maximum), and ch6 to ch8 is shown fsysm(80MHz maximum).

(2) Slave mode

Parameter	Symbol	Equation		fsysh = 100MHz ch0-3		fsys = 80MHz (Note) ch4-8		Unit
		Min	Max	Min	Max	Min	Max	
TSPIxSCK Input frequency	f_{CYC}	-	ch0-3: 20	-	20	-	-	MHz
			ch4-8: 10	-	-	-	10	
TSPIxSCK Input cycle	t_{CYC}	1/fcyc	-	50	-	100	-	ns
TSPIxSCK low level Input pulse width	t_{WL}	ch0-3: 15	-	15	-	-	-	
		ch4-8: 40		-	-	40	-	
TSPIxSCK High level Input pulse width	t_{WH}	ch0-3: 15	-	15	-	-	-	
		ch4-8: 40		-	-	40	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU1}	ch0-3: 40	-	40	-	-	-	
		ch4-8: 90		-	-	90	-	
TSPIxCSIN Input ← TSPIxSCK rise/fall time	t_{CSU2}	ch0-3: 40	-	40	-	-	-	
		ch4-8: 90		-	-	90	-	
TSPIxSCK rise/fall time → TSPIxCSIN hold time	t_{CHD}	ch0-3: 40	-	40	-	-	-	
		ch4-8: 90		-	-	90	-	
TSPIxRXD Input ← TSPIxSCK rise/fall time	t_{DSU}	ch0-3: 3	-	3	-	-	-	
		ch4-8: 16		-	-	16	-	
TSPIxSCK rise/fall → TSPIxRXD hold time	t_{DHD}	ch0-3: 8	-	8	-	-	-	
		ch4-8: 6		-	-	6	-	
TSPIxSCK rise/fall → TSPIxTXD hold time	t_{ODLY1}	2	-	2	-	2	-	
TSPIxSCK rise/fall → TSPIxTXD delay time	t_{ODLY2}	ch0-3: 25	-	-	25	-	-	
		ch4-8: 35		-	-	-	35	
TSPIxCSIN fall → TSPIxTXD delay time	t_{ODLY3}	ch0-3: 25	-	-	25	-	-	
		ch4-8: 38		-	-	-	38	
TSPIxCSIN high level input pulse width	t_{WDIS}	T×2+10	-	30	-	35	-	

Note: ch4 and ch5 is shown fsysh(160MHz maximum), and ch6 to ch8 is shown fsysm(80MHz maximum).

(1) 1st clock edge sampling (Master)

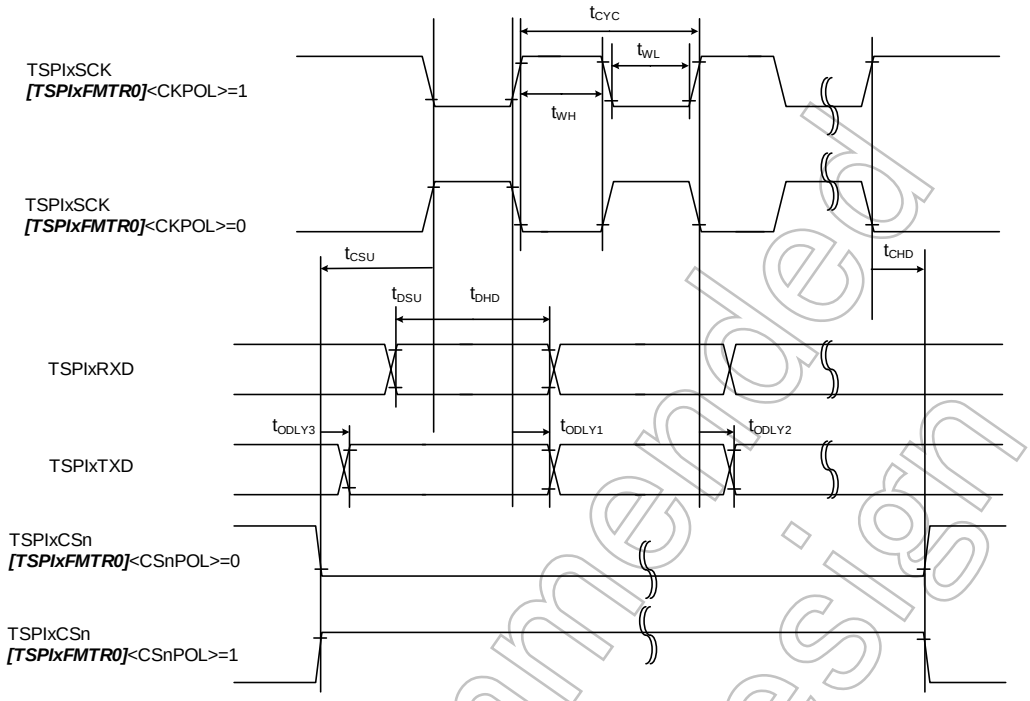


Figure 7.1 1st clock edge sampling (Master)

(2) 2nd clock edge sampling (Master)

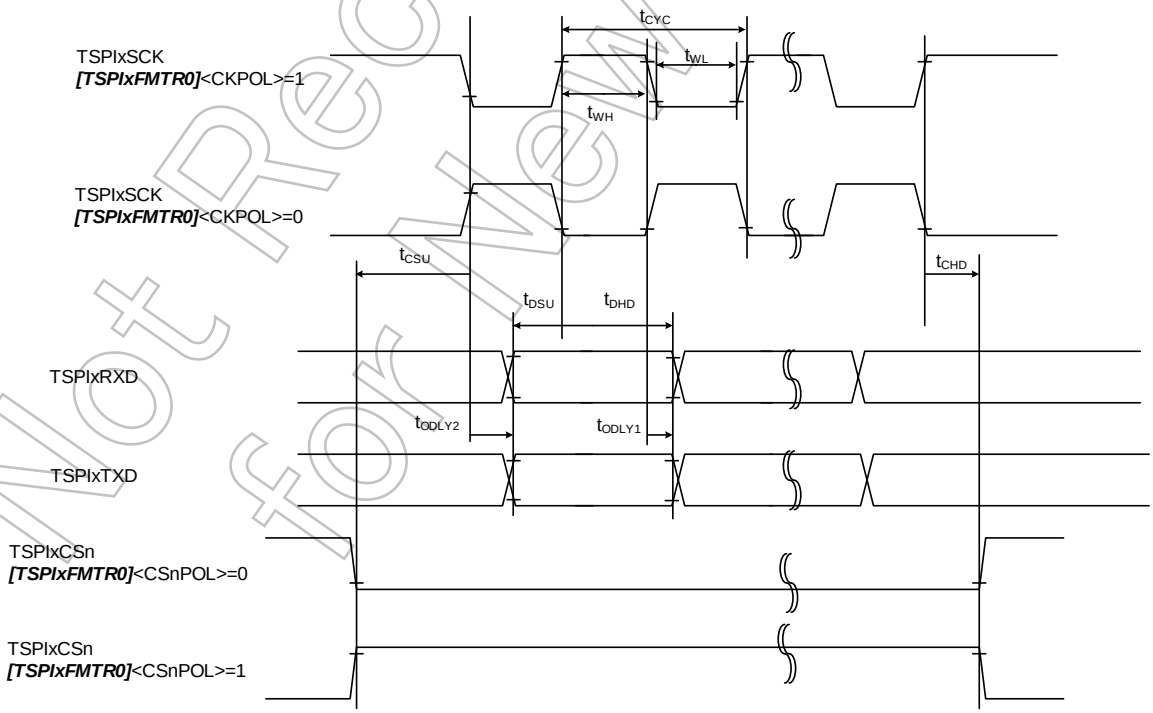


Figure 7.2 2nd clock edge sampling (Master)

(3) 2nd clock edge sampling (slave)

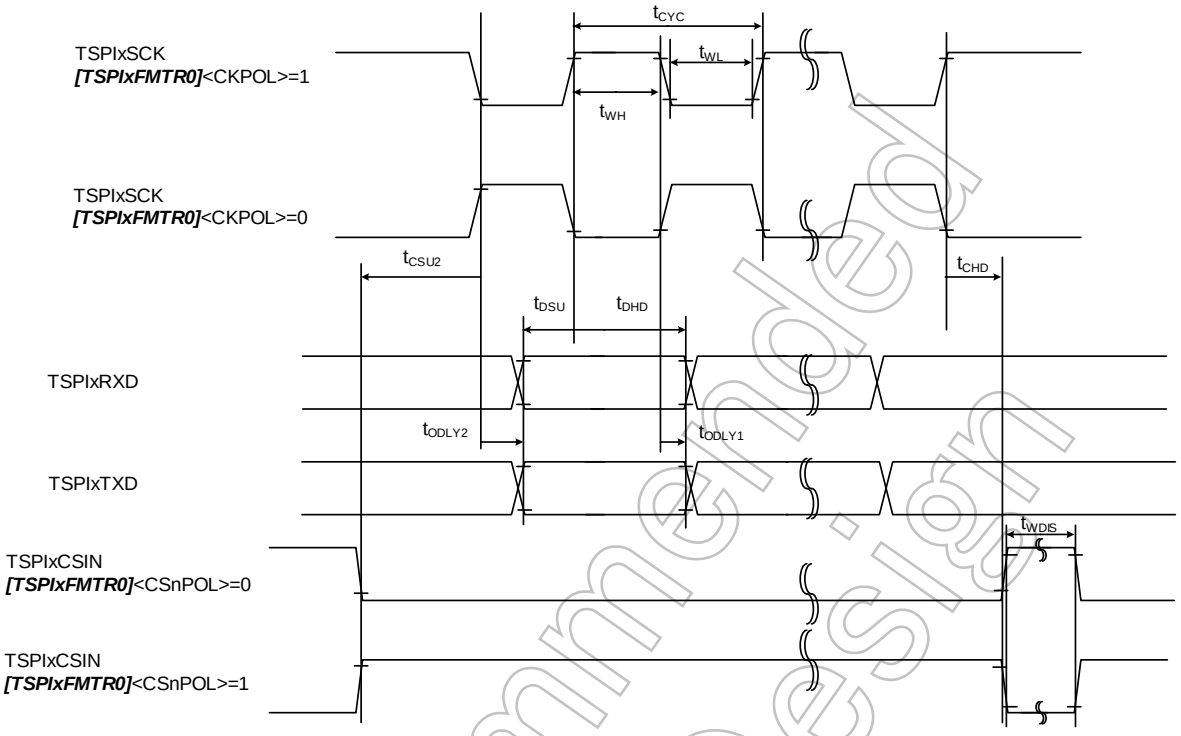


Figure 7.3 2nd clock edge sampling (Slave)

7.9.2. I2C Interface (I2C)

7.9.2.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Output level: Low = 0.4V
- Input level: High = 0.7×DVDD3, Low = 0.3×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.9.2.2. AC Electrical Characteristics

"T" indicate the Operation clock cycle of I^2C. The value of "n" is the SCL output clock frequency specified with ***[I2CxCR1]***<SCK>.

The value of "p" is the prescaler dividing ratio specified with ***[I2CxPRS]***<PRSCK>.

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Start condition hold time	$t_{HD,\ STA}$	4.0	-	0.6	-	μs
SCL clock Low width (Input) (Note 1)	t_{LOW}	4.7	-	1.3	-	
SCL clock High width (Input) (Note 2)	t_{HIGH}	4.0	-	0.6	-	
Re-start condition setup time (Note 5)	$t_{SU,\ STA}$	4.7	-	0.6	-	
Data hold time (Input) (Note 3, 4)	$t_{HD,\ DAT}$	0	-	0	-	
Data setup time	$t_{SU,\ DAT}$	250	-	100	-	ns
Stop condition setup time	$t_{SU,\ STO}$	4.0	-	0.6	-	μs
Bus free time between stop condition and start condition (Note 5)	t_{BUF}	4.7	-	1.3	-	

Note1: SCL clock low level width (output): $p \times (2^{n+1}+10)/T$ (***[I2CxOP]***<NFSEL>=0)

Note2: SCL clock high level width (output): $p \times (2^{n+1}+6)/T$ (***[I2CxOP]***<NFSEL>=0)

On I2C bus standard, the maximum speed of standard mode/fast mode is 100kHz/400 kHz respectively. Note that an internal SCL clock frequency is determined by the fsys and the calculation of Note 1 and Note 2 above-mentioned.

Note3: The data hold time (output) is equal to four cycles of the prescaler clock (Tprsck) started from the internal SCL.

Note4: On I2C bus standard, it is described that a data internal hold time should be set at least 300 ns to avoid unstable condition on the falling of the SCL when the SDA is input; however, this precaution is not supported in this MCU. Also, the edge slope control function for the SCL is not available. Therefore, when the customer designs the MCU, make sure to follow the data hold time (input) in the table above. Note that tr/tf on the SCL/SDA should be included in the data hold time.

Note5: Depends on software.

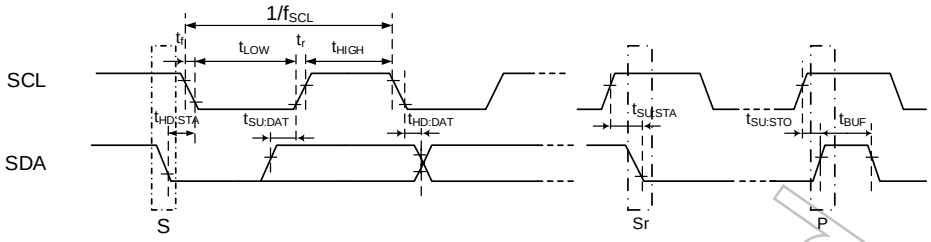


Figure 7.4 AC timing of I²C

7.9.3. 32-bit Timer Event Counter (T32A)

This section describes AC characteristics of T32AxINA0/A1, T32AxINB0/B1, and T32AxINC0/C1.

7.9.3.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.9.3.2. AC Characteristics

"T" in the table below indicates the operation clock cycle of the T32A. The operation clock of the T32A is the same cycle as the ΦT0m clock. This cycle is depending on the Prescaler Clock setting.

(1) Operation other than the pulse count

Parameter	Symbol	Equation		ΦT0m=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{VCKL}	2T + 20	-	45	-	ns
High level pulse width	t_{VCKH}	2T + 20	-	45	-	

(2) At the pulse count

Parameter	Symbol	Equation		ΦT0m =80 MHz		Unit
		Min	Max	Min	Max	
Pulse cycle	t_{DCYC}	1000	-	1000	-	ns
Low level pulse width	t_{PWL}	500	-	500	-	
High level pulse width	t_{PWH}	500	-	500	-	
Input setup	t_{ABS}	(NF+1)×T+20	-	32.5	-	
Input hold	t_{ABH}	(NF+1)×T+20	-	32.5	-	

NF Value is depending on the ***[T32AxPLSCR]***<NF[1:0]> setting as following.

***[T32AxPLSCR]*<NF[1:0]>**	**NF Value of Formula**
00	0
01	2
10	4
11	8

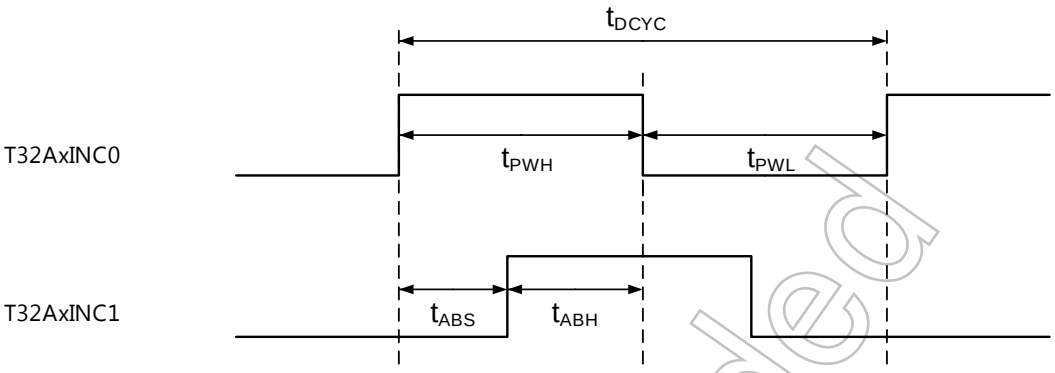


Figure 7.5 Count Pulse input

7.9.4. External Bus Interface(EBIF)

7.9.4.1. AC Measurement Conditions

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C(fsys≤120MHz), Ta= -40 to 70°C (fsys≤160MHz)
- Output level: High = 0.8 × DVDD3, Low = 0.2 × DVDD3
- Input level: High = 0.75 × DVDD3, Low = 0.25 × DVDD3
- Load capacity: CL = 30pF

7.9.4.2. Variable Condition

- RWS: Number of setup cycle insertion before RD, WR asserted.: RWS = 0, 1, 2, 4
- TW: Number of internal wait insertion: TW = 0 to 15
- TWEX: Number of external wait insertion: TWEX = any
- RWH: Number of RD, WR recovery cycle insertion: RWH = 0 to 6 or 8
- CSH: Number of ECSx_N recovery cycle insertion: CSH = 0, 1, 2, 4

7.9.4.3. AC Electrical Characteristics (EEXBCLK asynchronous Separate Mode)

Variable Condition: RWS = 1, TW = 3, TWEX = 4, RWH = 1, CSH =1

Parameter	Symbol	Equation		fsysh = 80MHz		fsysh = 160MHz		Unit
		Min	Max	Min	Max	Min	Max	
System clock cycle (T)	t_{SYS}	T	-	12.5	-	6.25	-	ns
EA[0:23] valid → ERD_N, EWR_N fall	t_{AC}	T (1+RWS) - 15	-	10	-	-2.5	-	
ERD_N, EWR_N rise → EA[0:23] hold	t_{CAR}	T (1+RWH+CSH)-17	-	27.5	-	1.75	-	
EA[0:23] valid → ED/EAD[0:15] input	t_{AD}	-	T (2+RWS+TW+TWEX)-35	-	90.0	-	27.5	
ERD_N fall → EA/EAD[0:15] input	t_{RD}	-	T (1+TW+TWEX)-30	-	70.0	-	20	
ERD_N Low level pulse width	t_{RR}	T (1+TW+TWEX)-15	-	85.0	-	35	-	
ERD_N rise → EA/EAD[0:15] hold	t_{HR}	0	-	0	-	0	-	
ERD_N rise → EA[0:23] output	t_{RAE}	T (1+RWH+CSH)-17	-	22.5	-	1.75	-	
EWR_N Low level pulse width	t_{WW}	T (1+TW+TWEX)-15	-	85.0	-	35	-	
ED/EAD[0:15] valid → EWR_N rise	t_{DW}	T (1+TW+TWEX)-15	-	85.0	-	35	-	
EWR_N rise → EA/EAD[0:15] hold	t_{WD}	T (1+RWH)-17	-	15	-	-4.5	-	
ERD_N/EWR_N fall → EWAIT_N fall	t_{RWW}	-	T (TW)-30	-	7.5	-	-11.25	
EWAIT_N rise → ERD_N/EWR_N rise	t_{WRW}	-	4T+30	-	80	-	55	

1. Read cycle (minimum bus cycle)

(Neither Cycle expander, RD setup, Internal wait, CS recovery nor RD recovery are used)

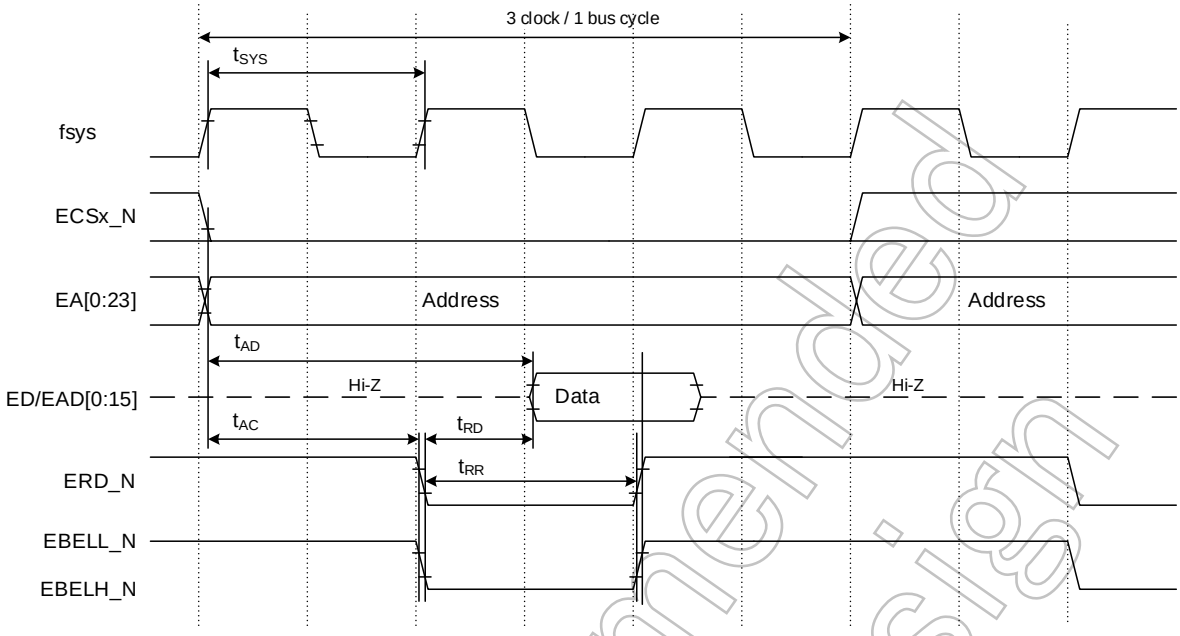


Figure 7.6 Read cycle timing (minimum bus cycle)

2. Read cycle (1 bus cycle per 6 clock)

(Cycle expander is not used, RD setup=1cycle, Internal wait=1cycle, CS recovery=1cycle, RD recovery=1cycle)

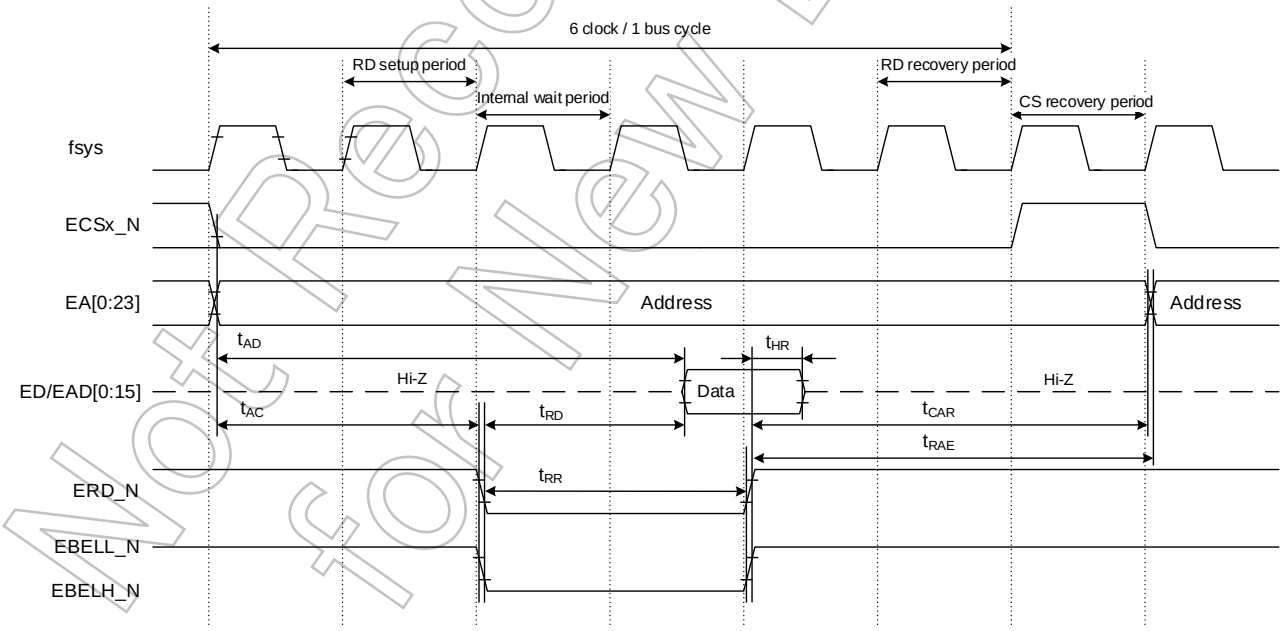


Figure 7.7 Read cycle timing (1 bus cycle per 6 clock)

3. Read cycle (external wait)

(Cycle expander is not used, RD setup=1cycle, Internal wait=3cycles, External wait=any, CS recovery=1cycle, RD recovery=1cycle)

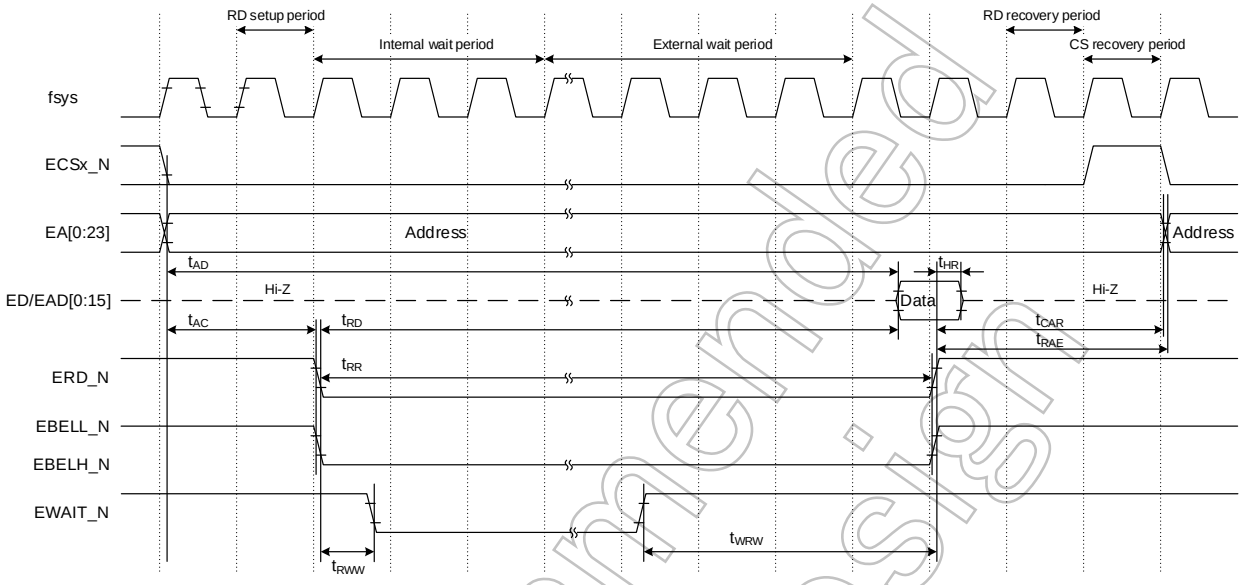


Figure 7.8 Read cycle timing (external wait)

4. Write cycle (minimum cycle)

(Neither Cycle expander, WR setup, Internal wait, CS recovery nor WR recovery are used)

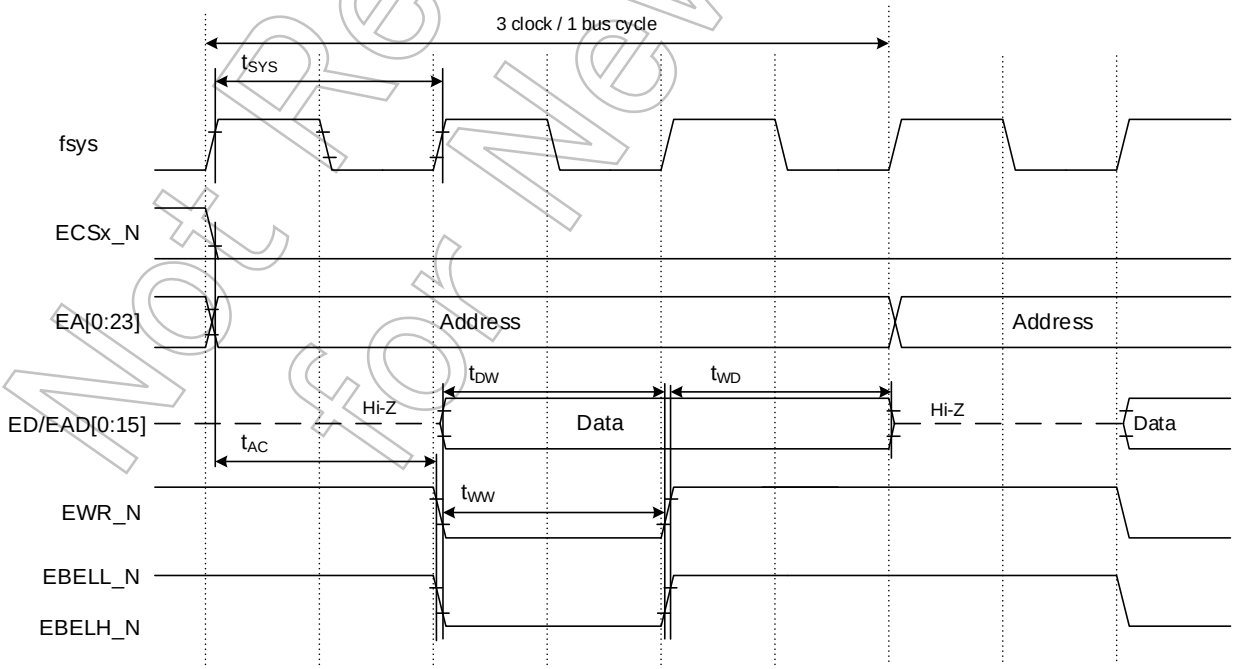


Figure 7.9 Write cycle timing (minimum cycle)

5. Write cycle (1 bus cycle per 6 clock)

(Cycle expander is not used, WR setup=1cycle, Internal wait=1cycle, CS recovery=1cycle, WR recovery=1cycle)

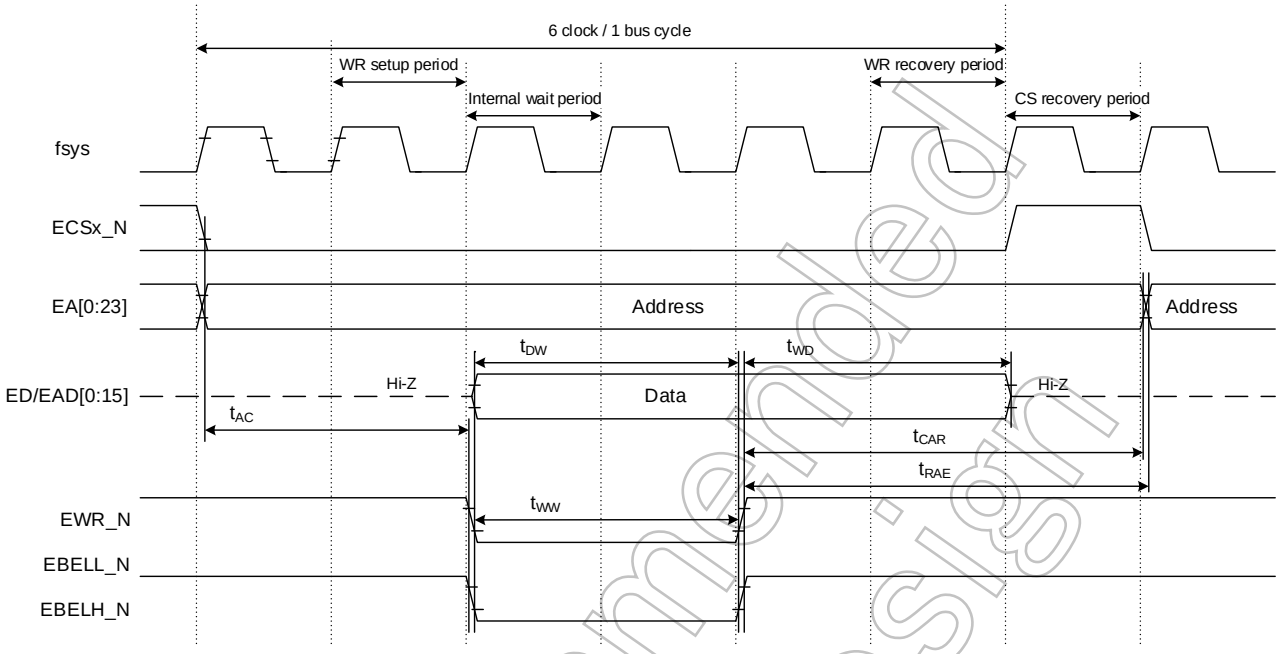


Figure 7.10 Write cycle timing (1 bus cycle per 6 clock)

6. Write cycle (external wait)

(Cycle expander is not used, WR setup=1cycle, Internal wait=3cycles, External wait=any, CS recovery=1cycle, WR recovery=1cycle)

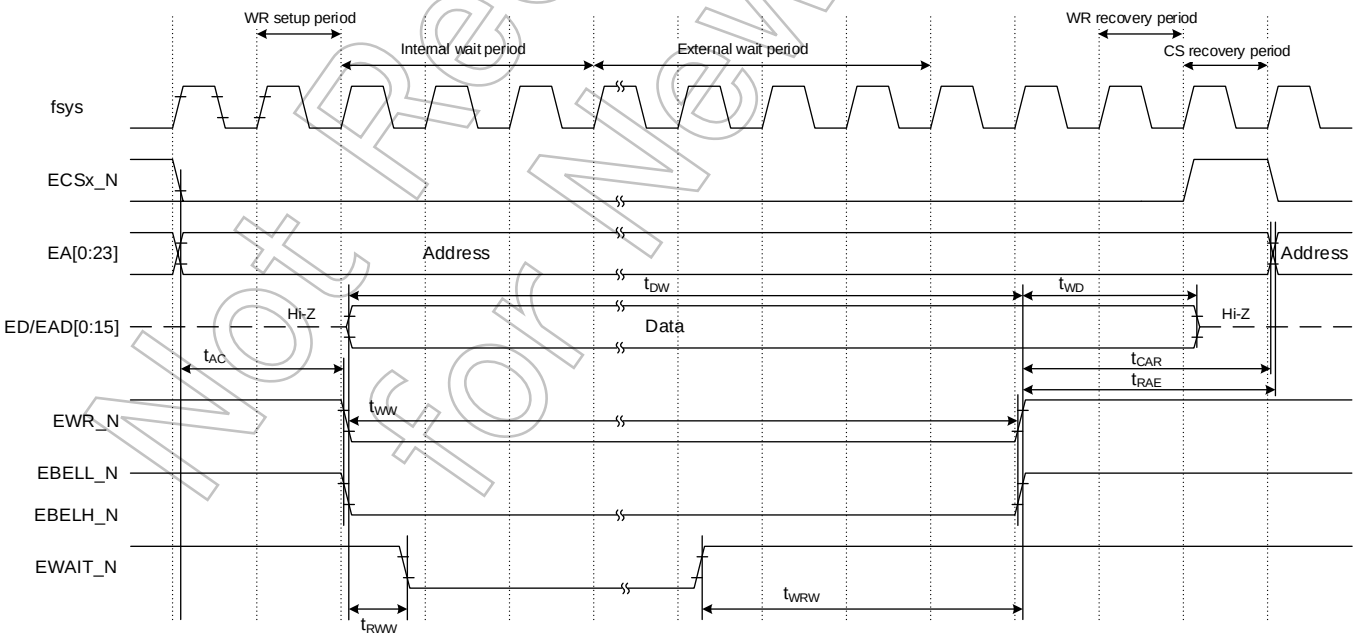


Figure 7.11 Write cycle timing (external wait)

7.9.4.4. AC Electrical Characteristics (EEXBCLK asynchronous multiplex bus mode)

Variable Condition: ALE=1, RWS=1, TW=3, TWEX=4, RWH=1, CSH=1

Parameter	Symbol	Equation		fsysh = 80MHz		fsysh = 160MHz		Unit
		Min	Max	Min	Max	Min	Max	
System clock cycle (T)	t_{SYS}	T	-	12.5	-	6.25	-	ns
EA[0:23] valid → EALE fall	t_{AL}	T (1+ALE)-15	-	10	-	-2.5	-	
EALE fall → EA[0:23] hold	t_{LA}	T (1+RWS)-15	-	15	-	-2.5	-	
EALE High pulse width	t_{LL}	T (1+ALE)-15	-	10	-	-2.5	-	
EALE fall → ERD_N, EWR_N fall	t_{LC}	T(1+RWS)-15	-	15	-	-2.5	-	
ERD_N, EWR_N rise → EALE rise	t_{CL}	T (1+RWH+CSH)-15	-	22.5	-	3.75	-	
EA[0:15] valid →ERD_N,EWR_N fall EA[16:23] valid →ERD_N,EWR_N fall	t_{ACL} t_{ACH}	T (2+ALE+RWH)-15	-	35	-	10.0	-	
ERD_N, EWR_N rise → EA[16:23] hold	t_{CAR}	T (1+RWH+CSH)-15	-	22.5	-	3.75	-	
EA[0:15] valid → ED/EAD[0:15] input EA[16:23] valid → ED/EAD[0:15] input	t_{ADL} t_{ADH}	-	T (3+ALE+RWS+TW+TWEX) -35	-	115	-	40	
ERD_N fall → ED/EAD[0:15] input	t_{RD}	-	T (1+TW+TWEX)-30	-	70	-	20	
ERD_N Low level pulse width	t_{RR}	T (1+TW+TWEX)-15	-	85.0	-	35	-	
ERD_N rise → ED/EAD[0:15] hold	t_{HR}	0	-	0	-	0	-	
ERD_N rise → EA[0:23] output	t_{RAE}	T (1+RWH+CSH)-19	-	22.5	-	-0.25	-	
EWR_N Low pulse width	t_{WW}	T (1+TW+TWEX)-15	-	85.0	-	35	-	
EA/EAD[0:15] valid → EWR_N rise	t_{DW}	T (1+TW+TWEX)-15	-	85.0	-	35	-	
EWR_N rise → ED/EAD[0:15] hold	t_{WD}	T (1+RWH)-17	-	15	-	-4.5	-	
ERD_N/EWR_N fall → EWAIT_N fall	t_{RWW}	-	T (TW)-30	-	7.5	-	-11.25	
WAIT rise → ERD_N/EWR_N rise	t_{WRW}	-	4T+30	-	80	-	55	

1. Read cycle (minimum cycle)

(Neither Cycle expander, ALE wait, RD setup, Internal wait, CS recovery nor RD recovery are used)

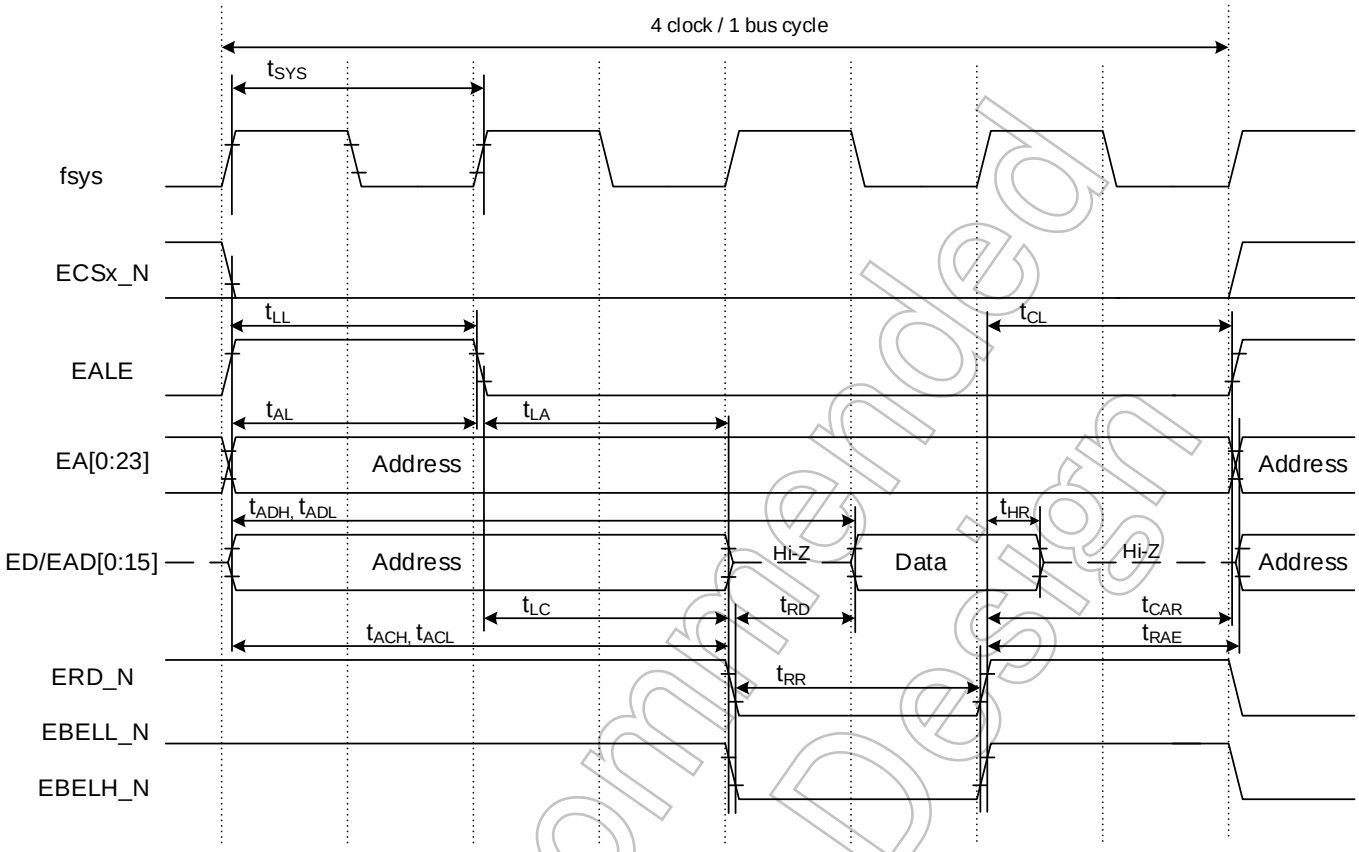


Figure 7.12 Read cycle timing (minimum cycle)

2. Read cycle (1 bus cycle per 8 clock)

(Cycle expander is not used, ALE wait=1cycle, RD setup=1 cycle, Internal wait=1cycle, CS recovery=1cycle, RD recovery=1cycle)

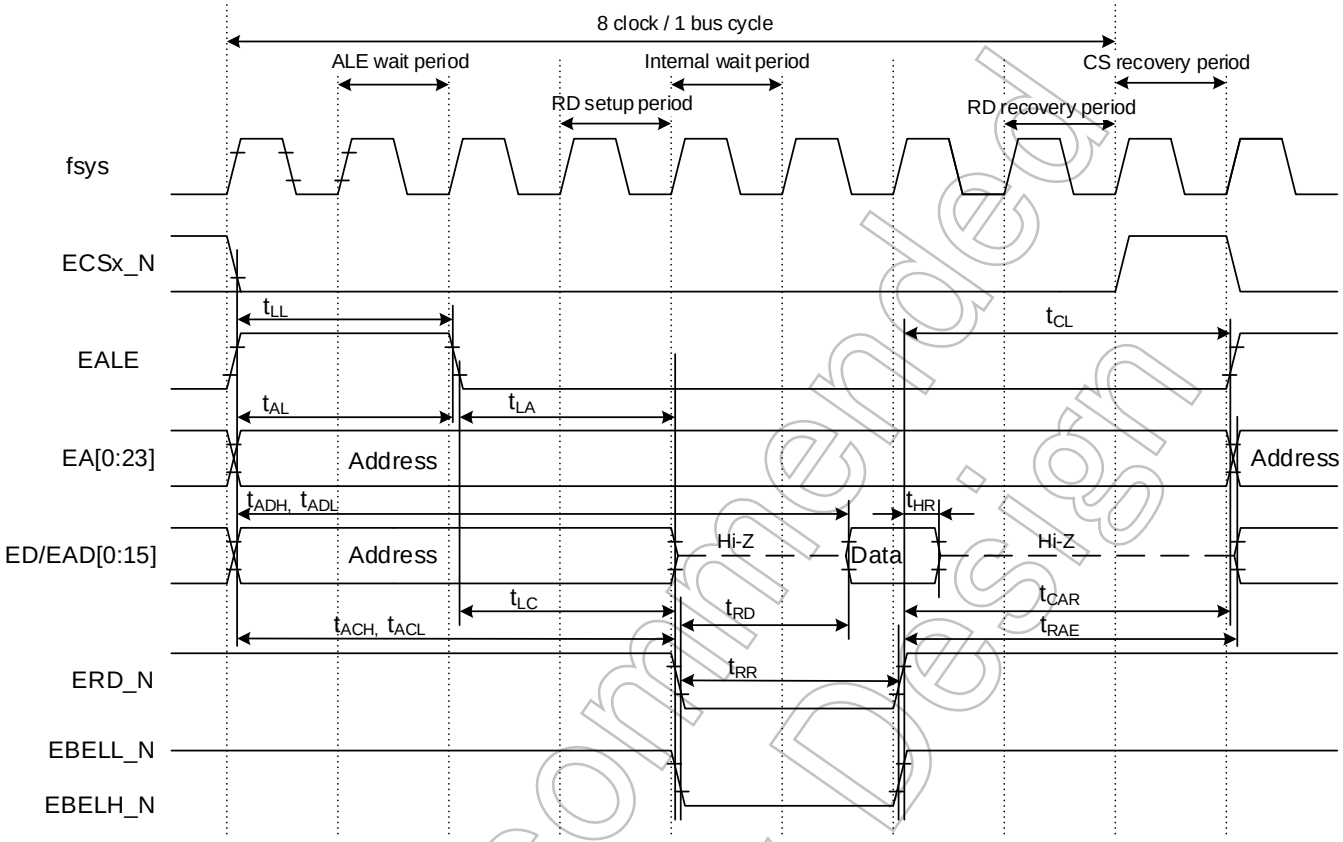


Figure 7.13 Read cycle timing (1 bus cycle per 8 clock)

3. Read cycle (1bus cycle per 10 clock)

(Cycle expander=double, ALE wait=1cycle, RD setup is not used, Internal wait=1cycle, CS recovery=1cycle, RD recovery=1cycle)

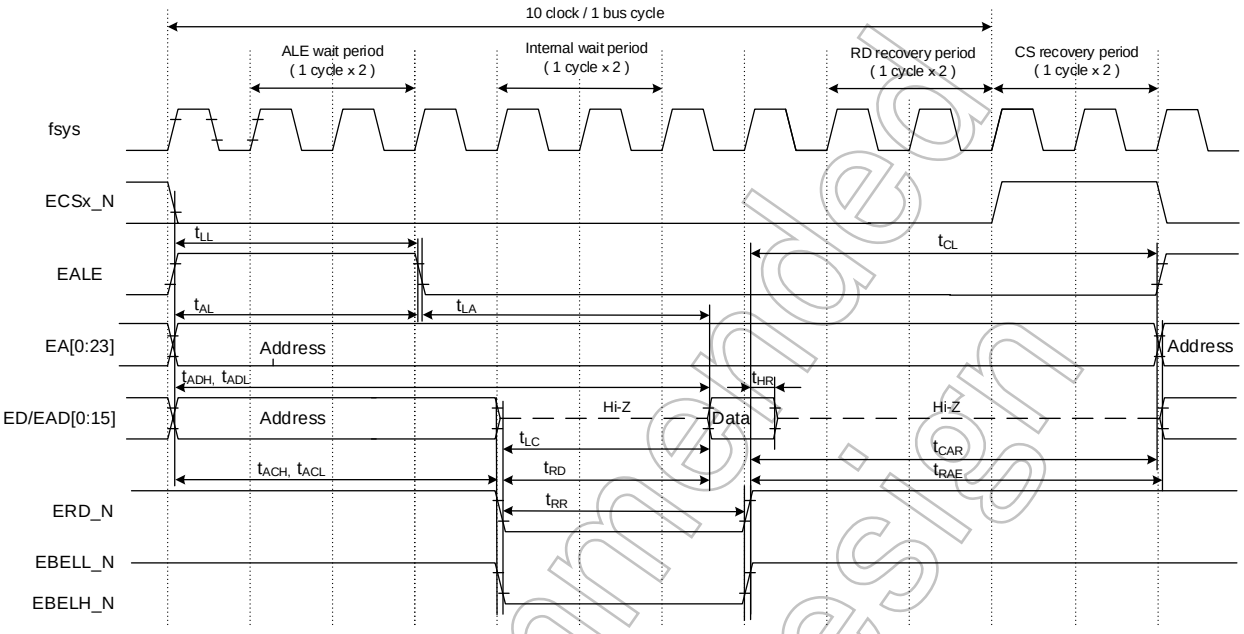


Figure 7.14 Read cycle timing (1 bus cycle per 10 clock)

4. Read cycle (external wait)

(Cycle expander is not used, ALE wait=1cycle, RD setup=1cycle, Internal wait=3cycles, External wait=any, CS recovery=1cycle, RD recovery=1cycle)

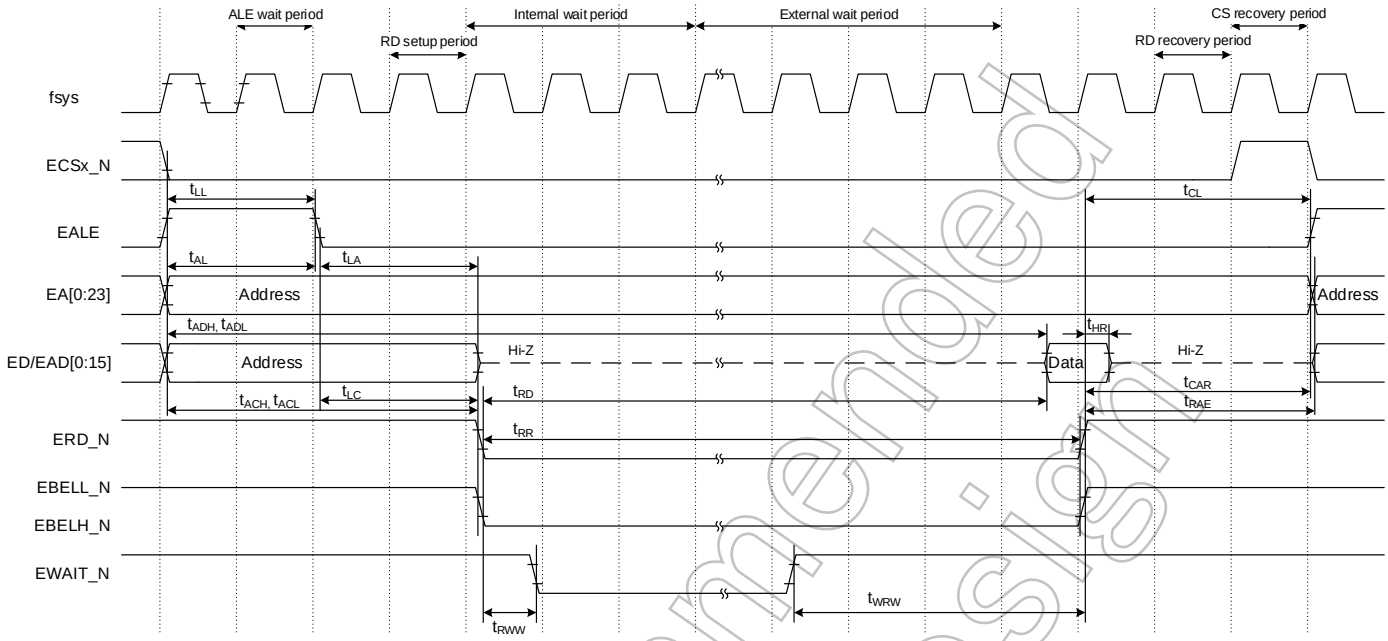


Figure 7.15 Read cycle timing (external bus wait)

5. Write cycle (minimum bus cycle)

(Neither Cycle expander, ALE wait, WR setup, Internal wait, CS recovery nor WR recovery are used.)

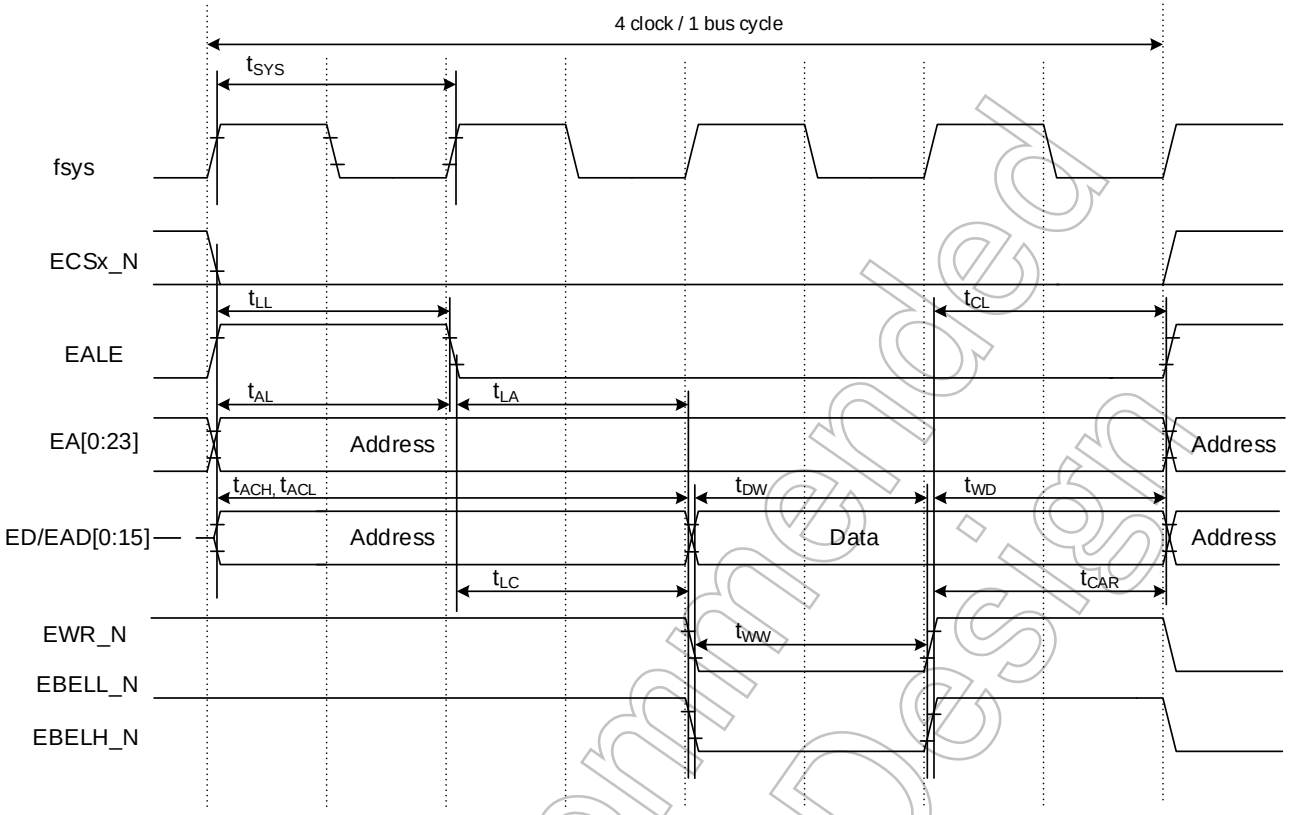


Figure 7.16 Write cycle timing (minimum bus cycle)

6. Write cycle (1 bus cycle per 8 clock)

(Cycle expander is not used, ALE wait=1cycle, WR setup=1cycle, Internal wait=1cycle, CS recovery=1cycle, WR recovery=1cycle)

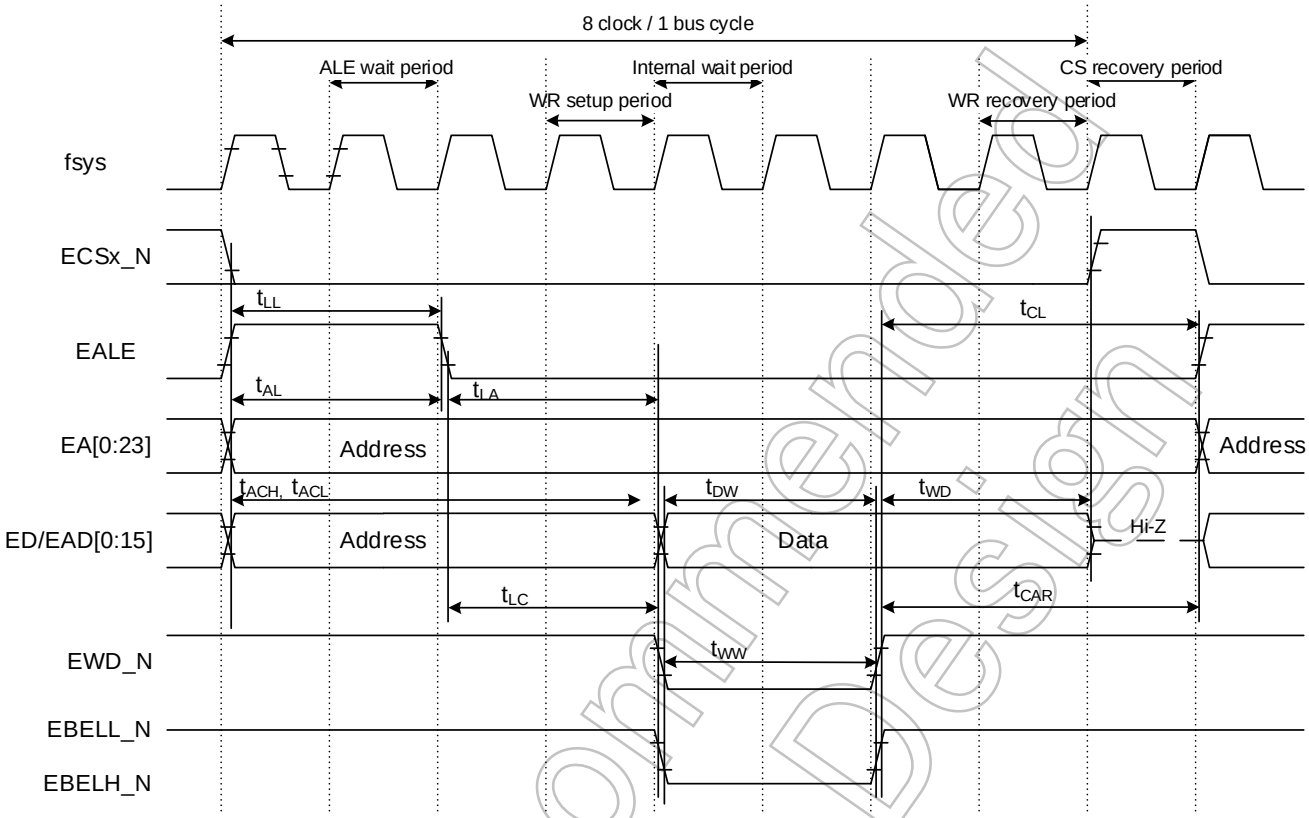


Figure 7.17 Write cycle timing (1 bus cycle per 8 clock)

7. Write cycle (external wait)

(Cycle expander is not used, ALE wait=1cycle, WR setup=1cycle, Internal wait=3cycles, External wait=any, CS recovery=1cycle, WR recovery=1cycle)

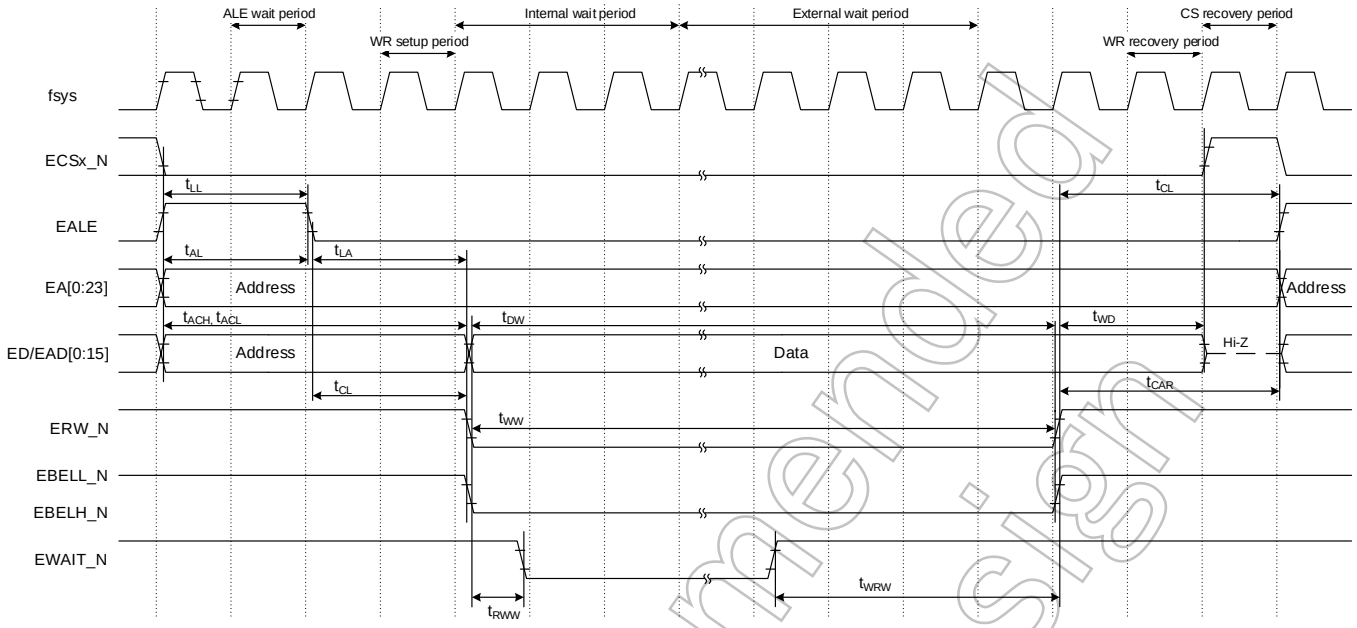


Figure 7.18 Write cycle timing (external wait)

7.9.4.5. AC Electrical Characteristics (EEXBCLK synchronous separate bus mode / multiplex bus mode)

Parameter	Symbol	Equation		fsysh=160MHz		Unit
		Min	Max	Min	Max	
External bus clock cycle(EEXBCLK)	X	33.3	-	33.3	-	ns
Output pin fix → EEXBCLK fall	t_S	2	-	2	-	
EEXBCLK fall → Output pin hold	t_H	7	-	7	-	
ED/EAD[15:0] input fix → EEXBCLK rise	t_{DS}	20	-	20	-	
EEXBCLK rise → ED/EAD[15:0] input hold	t_{DH}	0	-	0	-	
EWAIT_N input fix → EEXBCLK rise	t_{WS}	20	-	20	-	
EEXBCLK rise → EWAIT_N input hold	t_{WH}	0	-	0	-	

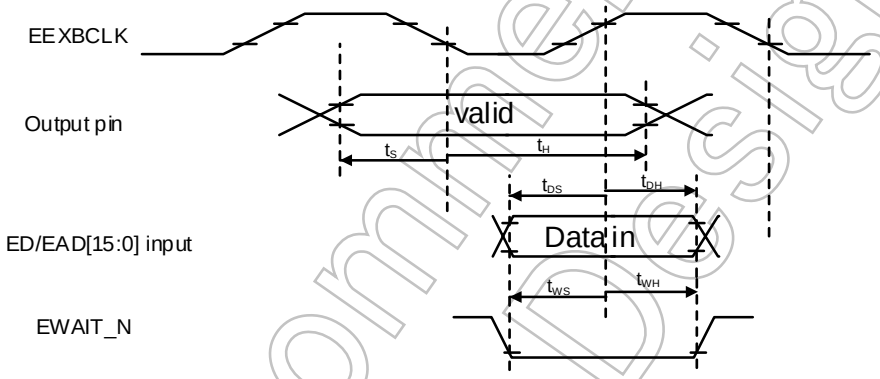


Figure 7.19 EEXBCLK synchronous separate bus mode / multiplex bus mode timing

7.9.5. Serial Memory Interface (SMIF)

7.9.5.1. AC Measurement Conditions

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C(fsysh ≤120MHz), Ta= -40 to 70°C (fsysh≤160MHz)
- Output level: High = 0.8 × DVDD3, Low = 0.2 × DVDD3
- Input level: High = 0.75 × DVDD3, Low = 0.25 × DVDD3
- Load capacity:CL = 30pF

Parameter	Symbol	Equation	Min	Max	Unit
SMIxCLK clock frequency	f_{CK}	-	20	-	MHz
Data setup time	t_{SU}	-	4	-	ns
Data hold time	t_{HD}	-	25	-	
Output valid	t_V	-	-	9	
Output hold time	t_{HO}	-	-11	-	
CS Setup time	t_{CSS}	1.5T-20	55	-	
CS hold time	t_{CSH}	1.0T-20	30	-	

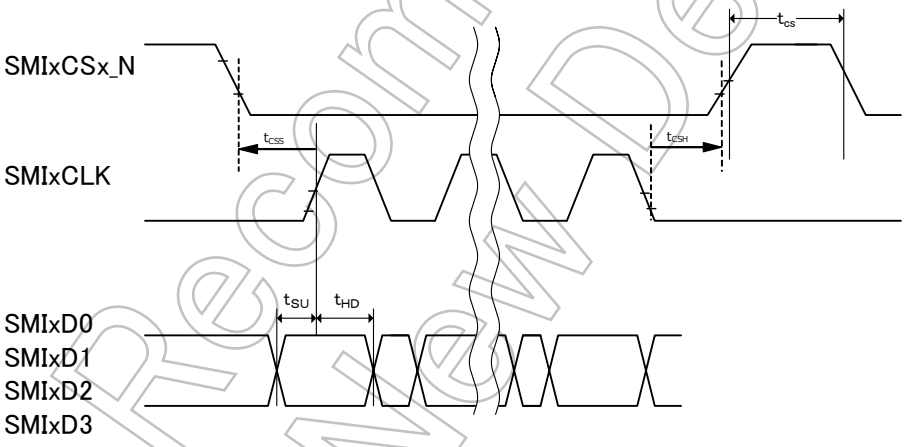


Figure 7.20 SMIF Input timing

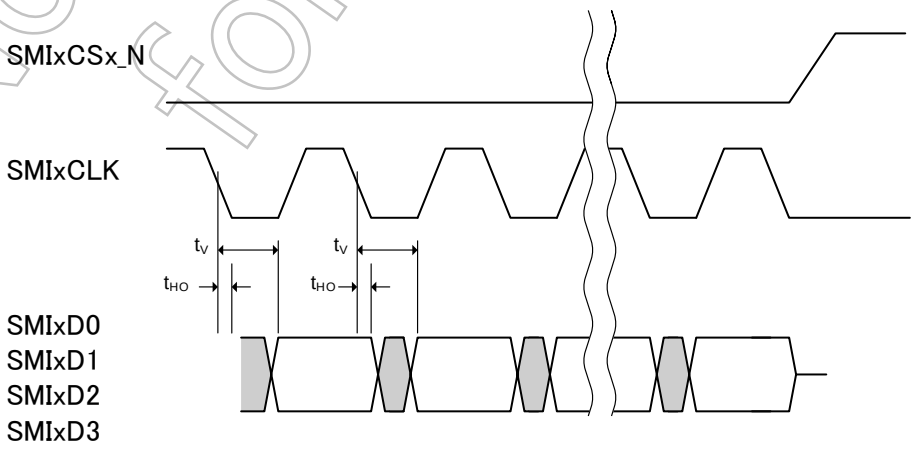


Figure 7.21 SMIF Output timing

7.9.6. External Interrupt

7.9.6.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C(fsysh ≤ 120MHz), Ta= -40 to 70°C (fsysh≤160MHz)
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.9.6.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

(1) NORMAL, IDLE mode

Parameter	Symbol	Equation		fsysh=160 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTAL1}	T + 100	-	106.25	-	ns
High level pulse width	t_{INTAH1}	T + 100	-	106.25	-	

(2) STOP1, STOP2 mode

Parameter	Symbol	Equation		fsysh=160 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{INTCL2}	500	-	500	-	ns
High level pulse width	t_{INTCH2}	500	-	500	-	

7.9.7. Trigger Input (TRGINx)

7.9.7.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.9.7.2. AC Electrical Characteristics

"T" in the table below indicates the cycle of the system clock (fsys).

Parameter	Symbol	Equation		fsysm=80 MHz		Unit
		Min	Max	Min	Max	
Low level pulse width	t_{ADL}	2T + 20	-	45	-	ns
High level pulse width	t_{ADH}	2T + 20	-	45	-	

7.9.8. Debug Communication

7.9.8.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C(fsys≤120MHz), Ta= -40 to 70°C (fsysh≤160MHz)
- Output level: High = 0.8×DVDD3, Low = 0.2×DVDD3
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.9.8.2. SWD Interface

Parameter	Symbol	Min	Max	Unit
CLK cycle	T_{dck}	100	-	ns
Output data hold time from the rising edge of CLK	T_{d1}	4	-	
Output data valid time from the rising edge of CLK	T_{d2}	-	30	
From input data valid time to the rising edge of CLK	T_{ds}	20	-	
Input data hold time from the rising edge of CLK	T_{dh}	15	-	

7.9.8.3. JTAG Interface

Parameter	Symbol	Min	Max	Unit
CLK cycle	T_{dck}	100	-	ns
Output data hold time from the falling edge of CLK	T_{d3}	4	-	
Output data valid time from the falling edge of CLK	T_{d4}	-	50	
From input data valid time to the rising edge of CLK	T_{ds}	20	-	
Input data hold time from the rising edge of CLK	T_{dh}	15	-	

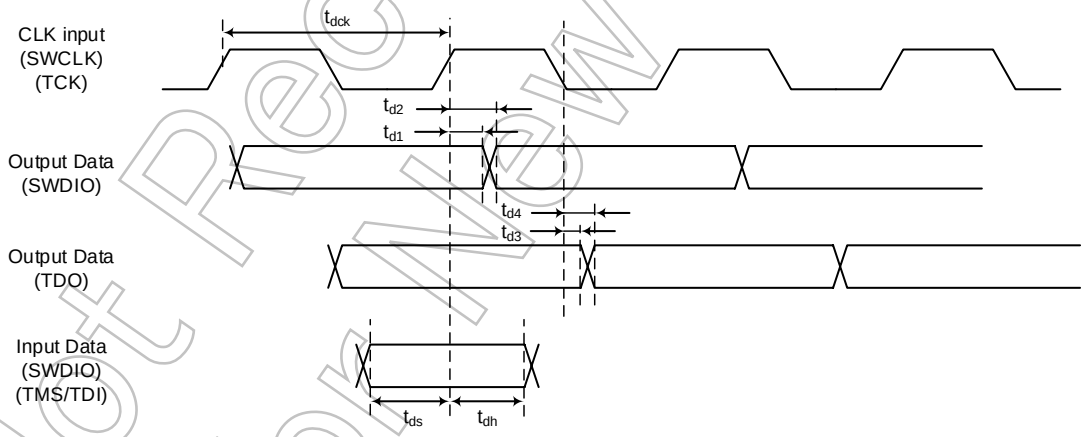


Figure 7.22 JTAG/SWD waveform

7.9.8.4. ETM Trace

Parameter	Symbol	Min	Max	Unit
TRACECLK cycle	t_{tclk}	25	-	ns
Data valid time from rising on TRACECLK	t_{setupr}	2	-	
TRACEDATA hold time from the rising edge of TRACECLK	t_{holdr}	1	-	
TRACEDATA valid time from the falling edge of TRACECLK	t_{setupf}	2	-	
TRACEDATA hold time from the falling edge of TRACECLK	t_{holdf}	1	-	

Note: When fsys > 100MHz, the condition is DVDD3=3.3V, CL=10pF.

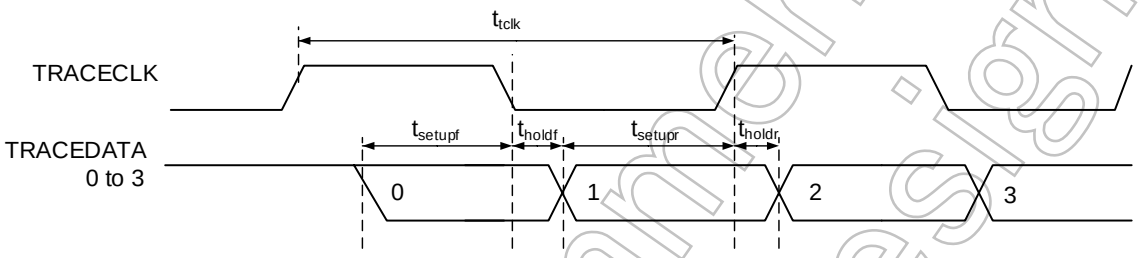


Figure 7.23 Trace signal waveform

7.9.8.5. Non Break Debug Interface (NBDIF)

Parameter	Symbol	Min	Max	Unit
NBDCLK Cycle Time	t_{NDCYC}	80	-	ns
NBDCLK Low Pulse width	t_{NDL}	35	-	
NBDDATA Output Delay Time	t_{NDD}	-	t_{NDCYC} - 20	
NBDDATA Output Hold Time	t_{NDHD}	5	-	
NBDDATA Setup Time	t_{NDS}	20	-	
NBDDATA Hold Time	t_{NDH}	5	-	
NBDSYNC Setup Time	t_{NDSYS}	20	-	
NBDSYNC Output Hold Time	t_{NDSYH}	5	-	

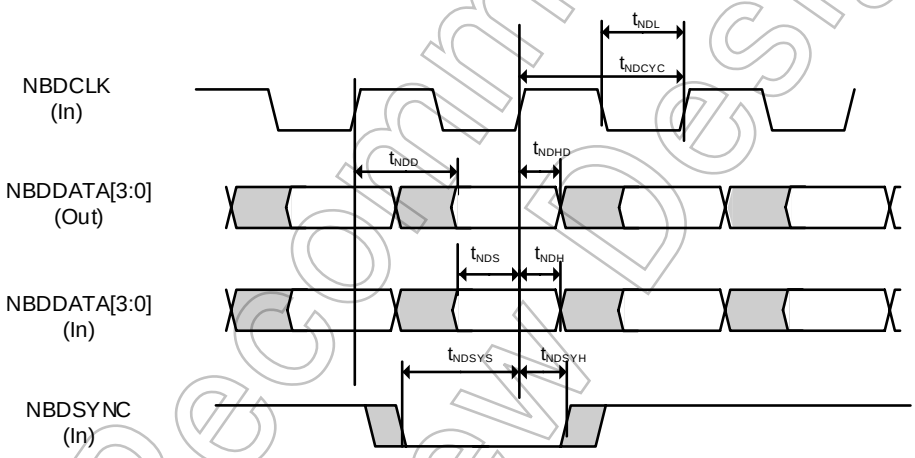


Figure 7.24 NBDIF waveform

7.9.8.6. Noise Filter Characteristics

Parameter	Condition	Min	Typ.	Max	Unit
Noise cancel width		15	30	60	ns

7.9.9. External Clock Input

7.9.9.1. AC Measurement Conditions

The AC characteristics are the result under the measurement conditions below:

- DVDD3 = AVDD3 = 2.7V to 3.6V
- Ta = -40 to 85°C
- Input level: High = 0.75×DVDD3, Low = 0.25×DVDD3
- Load capacity: CL = 30pF

Note: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

7.9.9.2. AC Electrical Characteristics

(1) High speed clock input

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency	t_{ehcin}	8	-	20	MHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	10	ns
Clock fall time	t_f	-	-	10	ns

(4) Low speed clock input

Parameter	Symbol	Min	Typ.	Max	Unit
Clock frequency	t_{ehcin}	30	-	34	kHz
Clock duty	-	45	-	55	%
Clock rise time	t_r	-	-	100	ns
Clock fall time	t_f	-	-	100	ns

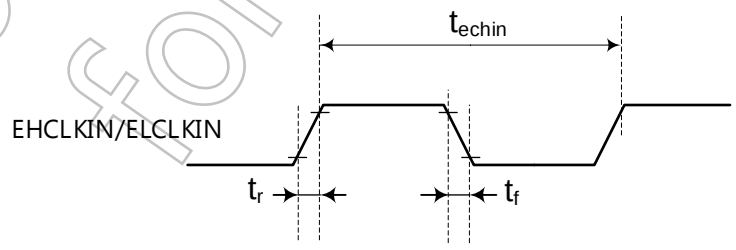


Figure 7.25 External clock input waveform

7.10. Flash Memory Characteristics

7.10.1. Code Flash

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance		-	-	10,000	cycles
Programming time	Word Program time	-	29.5	-	μs
Erase time	Page Erase time	-	18.1	-	ms
	Block Erase time	-	144.2	-	
	Area Erase time(Note2)	-	18.1	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: No block with effective protection.

7.10.2. Data Flash

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Endurance		-	-	100,000	cycles
Programming time		-	64.7	-	μs
Erase time	Page Erase time	1	-	3.9	ms
	Block Erase time	15.4	-	62.1	
	Area Erase time(Note2)	-	9.2	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: No block with effective protection.

7.10.3. Chip Erase

Item	Products
Code Flash 1.5MB	TMPM4G9F15FG, TMPM4G9F15XBG, TMPM4G8F15FG, TMPM4G8F15XBG
Code Flash 1.0MB or less	TMPM4G9F10FG, TMPM4G9FEFG, TMPM4G9FDFG, TMPM4G9F10XBG, TMPM4G9FEXBG, TMPM4G9FDXBG, TMPM4G8F10FG, TMPM4G8FEFG, TMPM4G8FDFG, TMPM4G8F10XBG, TMPM4G8FEXBG, TMPM4G8FDXBG, TMPM4G7F10FG, TMPM4G7FEFG, TMPM4G7FDFG, TMPM4G6F10FG, TMPM4G6FEFG, TMPM4G6FDFG

For the newest status of each product, Please contact your sales representative.

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Code Flash 1.5MB			Code Flash 1.0MB or less			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Chip Erase time	Erasing of Code Flash, Data Flash, Protect Bits(Code), Protect Bits(Data), and Security bits	-	100.1	-	-	82.0	-	ms

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: When Chip Erase command executes, no block with effective protection.

7.11. Regulator

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Condition	Min	Typ.	Max	Unit
Capacitance of REGOUT1 capacitor		-	1.0	-	µF

7.12. Oscillation Circuit

7.12.1. Internal Oscillator

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{IHOSC1}	Factory out, IC data	-	10	-	MHz
	f_{IHOSC2}		-	10	-	

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: Not included the influence depend on the variations after Factory shipping. Please execute oscillator adjustment by the trimming register, if trimming of IHOSC1 is required. However, IHOSC2 cannot execute trimming.

7.12.2. External Oscillator

DVDD3=2.7V to 3.6V
Ta= -40 to 85°C

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Oscillation frequency	f_{EHOSC}		8	-	20	MHz
	f_{ELOSC}		30	-	34	kHz

Note1: DVDD3 is generic name for DVDD3A, DVDD3B, DVDD3C, DVDD3D, DVDD3E, DVDD3F, DVDD3G, DVDD3H.

Note2: Please contact the oscillator vendor, regarding the matching data of the device and the oscillator.

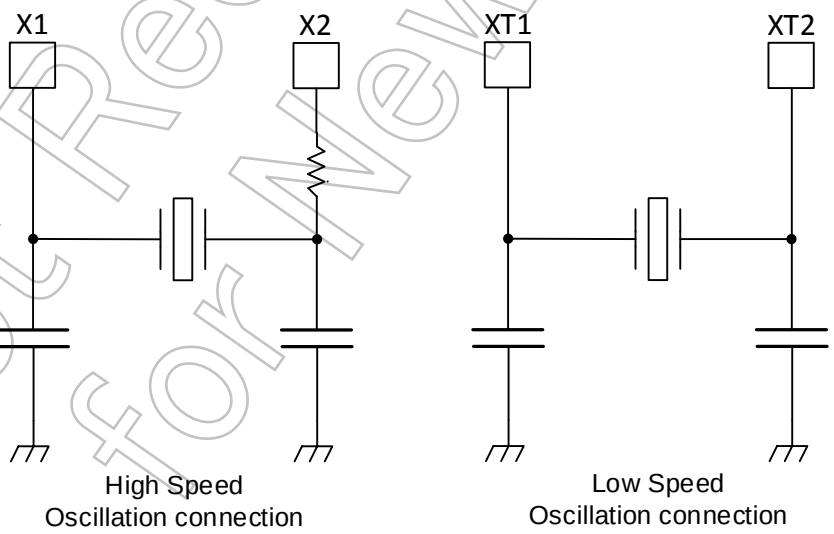


Figure 7.26 Oscillation circuit sample

To obtain a stable oscillation, load capacity and the position of the oscillator must be configured properly.

Since these factors are strongly affected by substrate patterns, please evaluate oscillation stability using the substrate you use.

This product has been evaluated by the oscillator vendor below. Please refer this information when selecting external parts.

7.12.3. Ceramic Oscillator

This product has been evaluated by the ceramic oscillator by Murata Manufacturing Co., Ltd.
Please refer to the Murata Website for details.

7.12.4. Crystal Oscillator

This product has been evaluated by the crystal oscillator by KYOCERA Corporation.
Please refer to the KYOCERA Website for details.

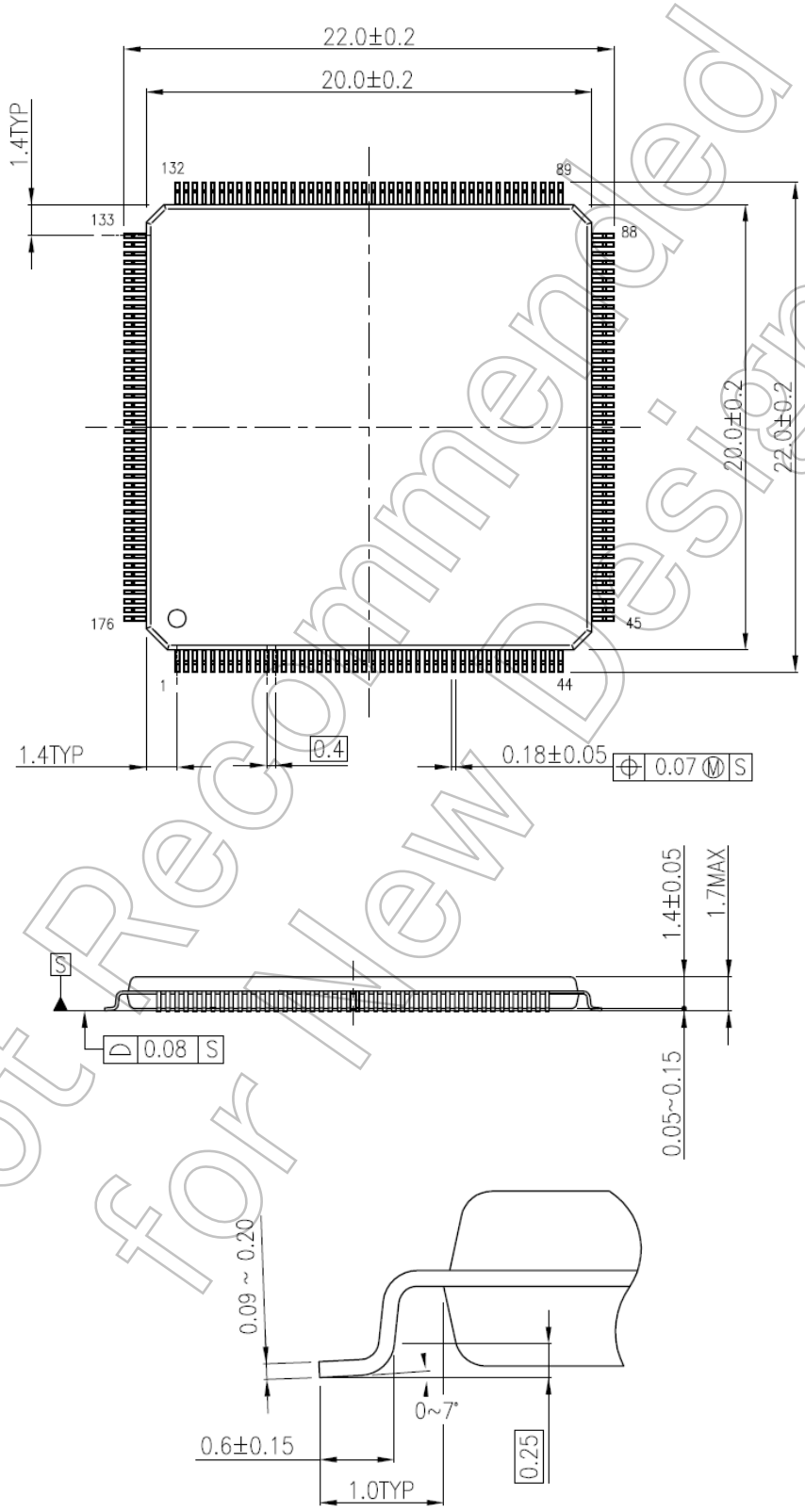
7.12.5. Precautions for designing printed circuit board

Be sure to design printed circuit board patterns that connect a crystal unit with other oscillation elements so that the length of such patterns become shortest possible to prevent deterioration of characteristics due to stray capacitances and wiring inductance. For multi-layer circuit boards, it is important not to wire the ground and other signal patterns right beneath the oscillation circuit. For more information, please refer to the URL of the oscillator vendor.

8. Package Dimensions

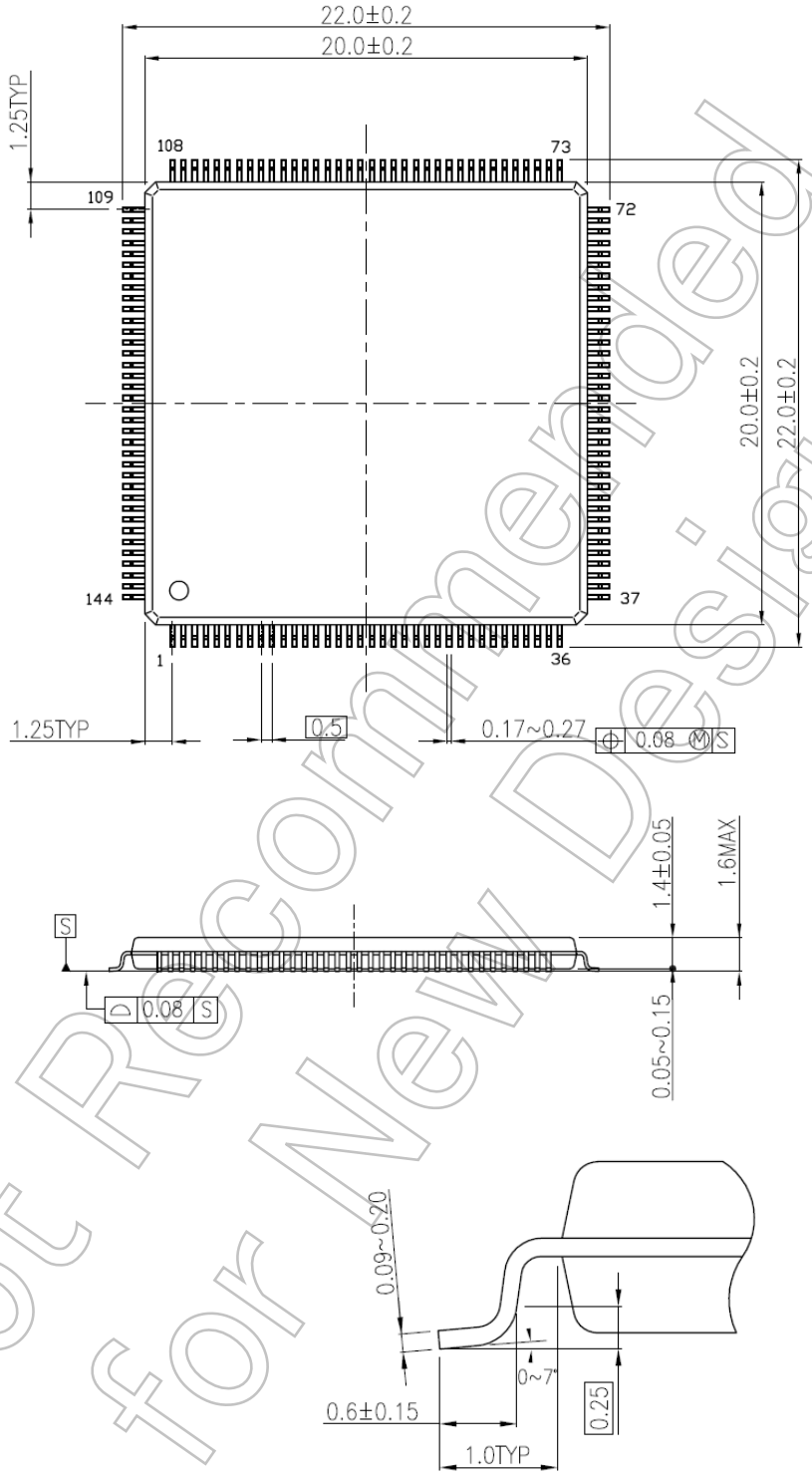
8.1. P-LQFP176-2020-0.40-002

Unit: mm



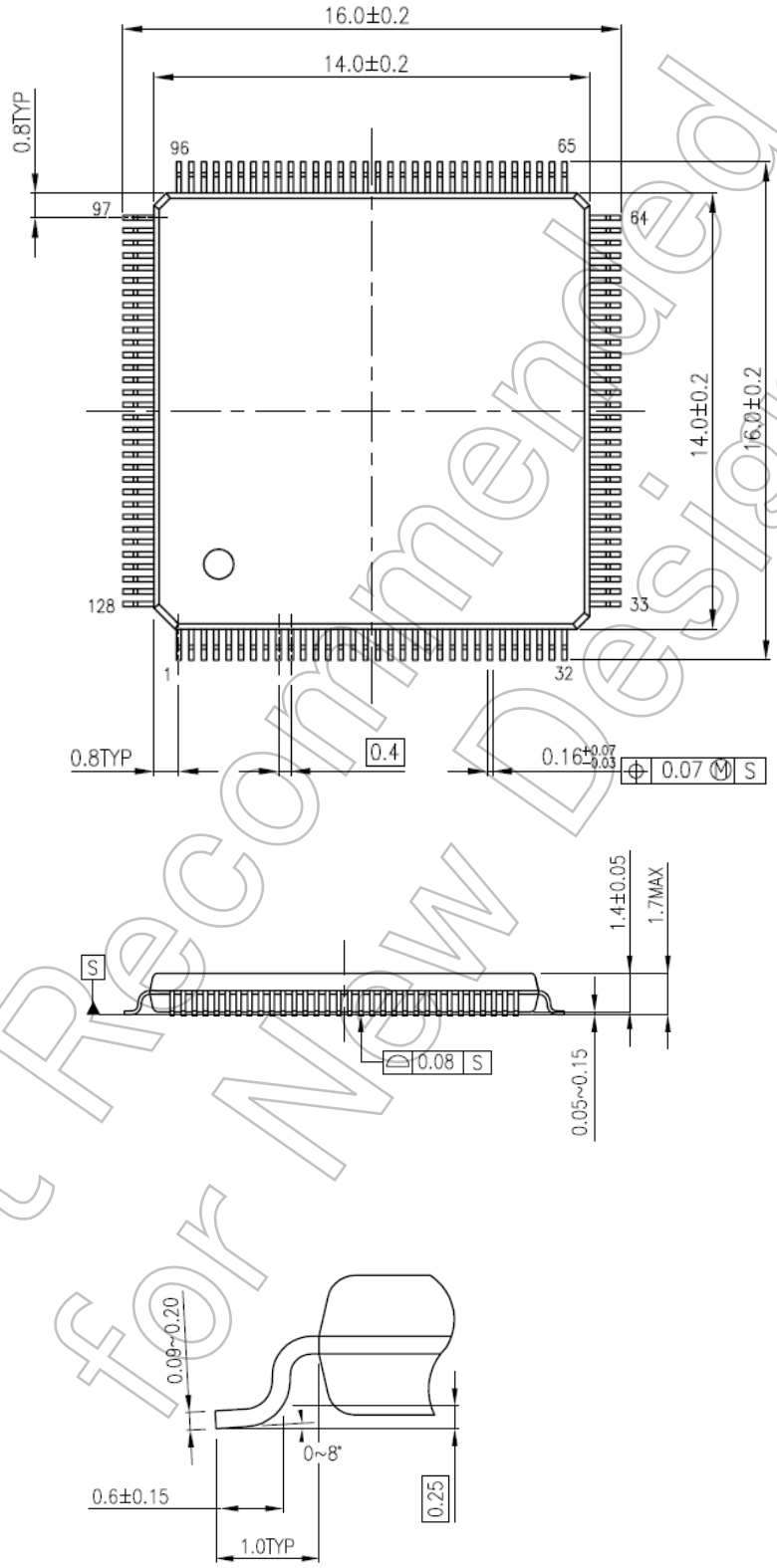
8.2. P-LQFP144-2020-0.50-002

Unit: mm



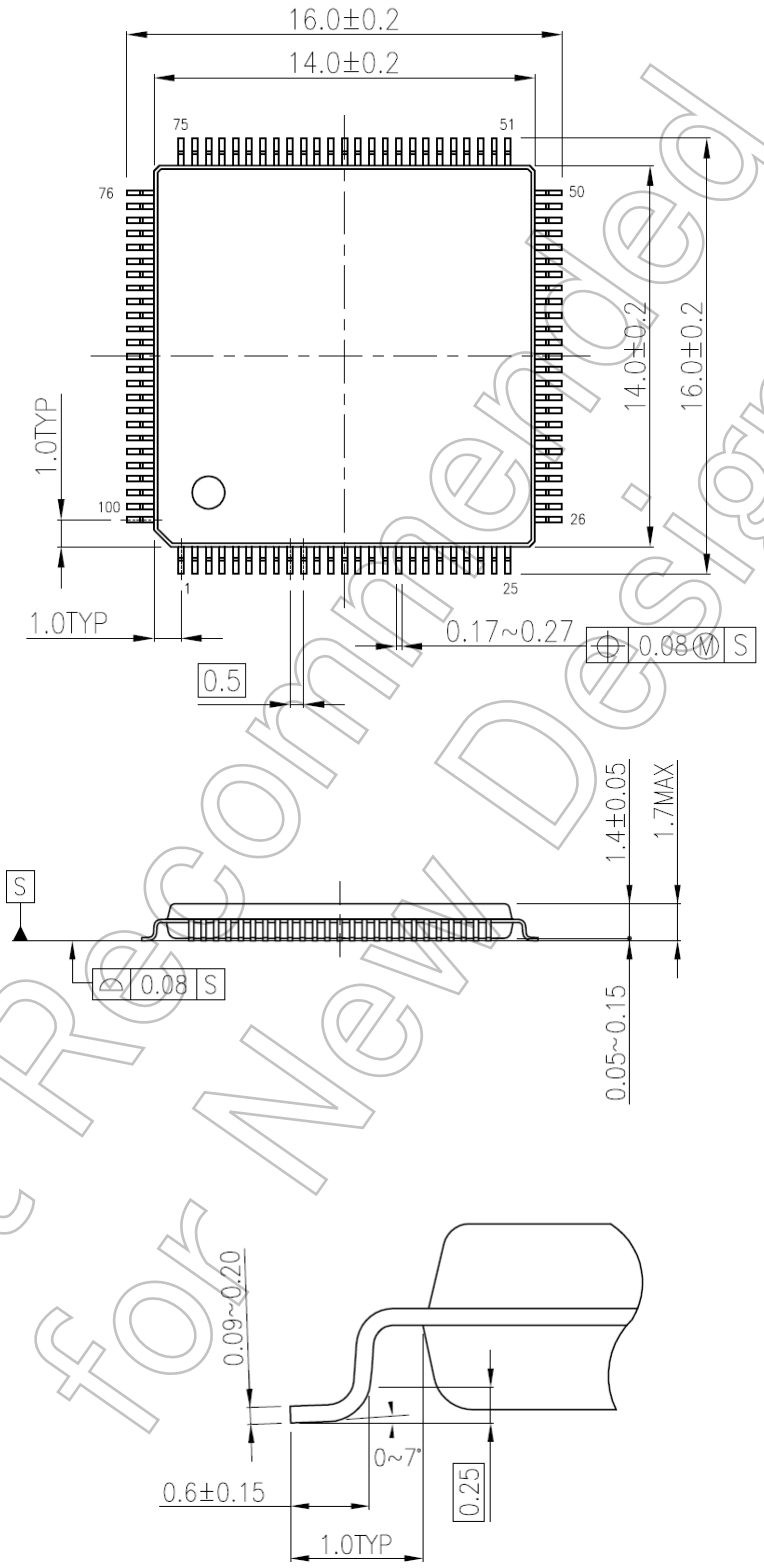
8.3. P-LQFP128-1414-0.40-001

Unit: mm



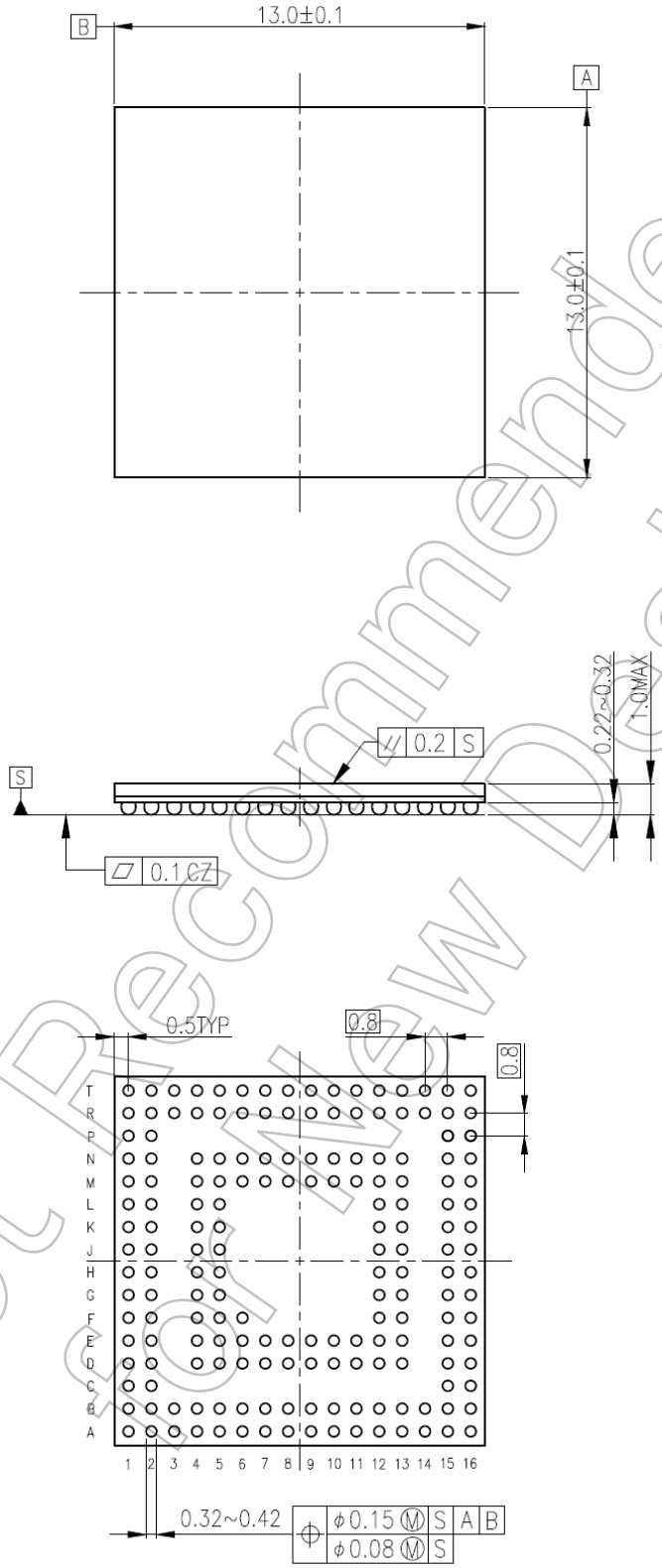
8.4. P-LQFP100-1414-0.50-002

Unit: mm



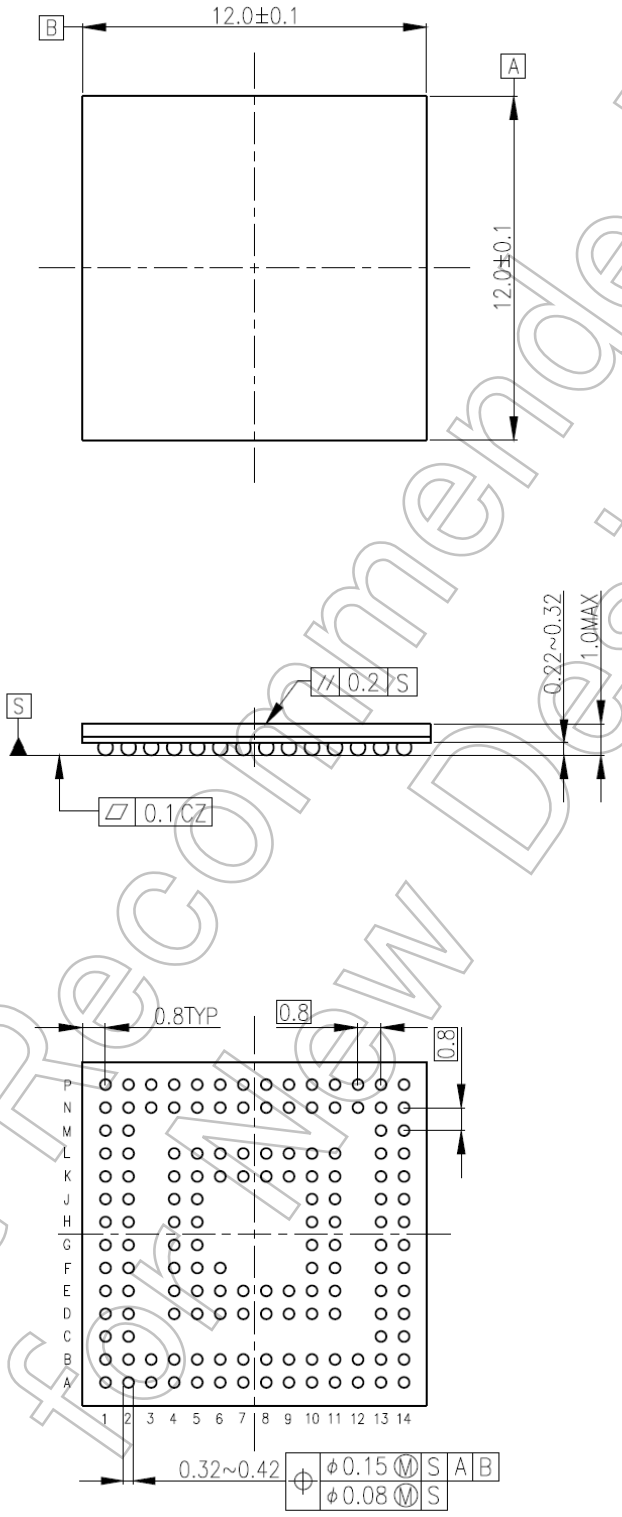
8.5. P-VFBGA177-1313-0.80-001

Unit: mm



8.6. P-VFBGA145-1212-0.80-001

Unit: mm



9. Precautions

This Page explains general precautions on the use of our MCUs.

Note that if there is a difference between the general precautions and the description in the body of the document, the description in the body of document has higher priority.

(1) The MCUs' operation at power-on

At power-on, internal state of the MCUs is unstable. Therefore, state of the pins is undefined until reset operation is completed.

When a reset is performed by an external reset pin, pins of the MCUs that use the reset pin are undefined until reset operation by the external pin is completed.

Also, when a reset is performed by the internal power-on reset, pins of the MCUs that use the internal power-on reset are undefined until power supply voltage reaches the voltage at which power- on reset is valid.

(5) Unused pins

Unused input/output ports of the MCUs are prohibited to use. The pins are high-impedance.

Generally, if MCUs operate while the high-impedance pins left open, electrostatic damage or latch- up may occur in the internal LSI due to induced voltage influenced from external noise.

We recommend that each unused pin should be connected to the power supply pins or GND pins via resistors.

(6) Clock oscillation stability

A reset state must be released after the clock oscillation becomes stable. If the clock is changed to another clock while the program is in progress, wait until the clock is stable.

10. Revision History

Table 10.1 Revision History

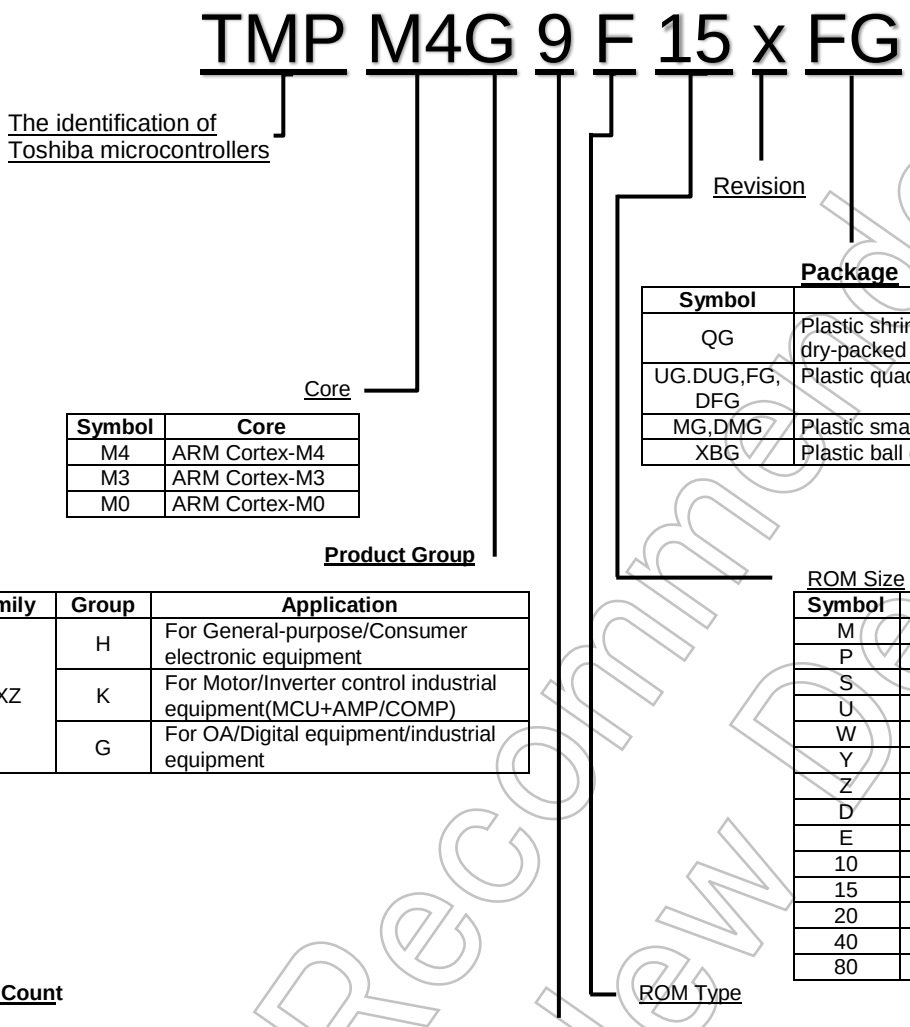
Revision	Date	Description
1.0	2018-02-02	First Release
2.0	2018-03-13	- Features Modified maximum baud rate of FUART Added maximum data rate for IrDA of FUART - Terms and Abbreviations Corrected spelling of “Circuit” of TRM - Products Lists Categorized by Functions Changed “UNIT” to “ch” of ISD in Table1 to Table6 - 1. Block Diagram Changed “UNIT” to “ch” of MDMAC, “UNIT” to “ch” of HDMAC in Figure 1.1 Changed “4 to 12 ch” to “1 to 3 units” of ISD in Figure 1.1 - 4.2 Functional Pin and Port Assignment (Pin Number) - 5.12 Interval Sensor Detection Circuit(ISD) Modified “UNIT” to “unit” in Table5.12 Added TMS/SWCLK/SWV in Table4.21 - 5.13.1 Multi-Function DMA Controller (MDMAC) Modified explanation Modified “UNIT” to “unit” in Table5.13 - 5.13.2 High Speed DMA Controller(HDMAC) Modified explanation Modified “UNIT” to “unit” in Table5.14 - 5.21 12-bit Analog to Digital Converter (ADC) Modified explanation Modified “UNIT” to “unit” in Table5.21 - 6.1 Port Equivalent circuit of port with external interrupt input are written separately Modified Note of PY4/BOOT_N - 6.4 Clock control Modified EHCLKIN/ELCLKIN circuit - 7.1 Absolute Maximum Ratings Changed port name description - 7.2 DC Electrical Characteristics (1/2) Changed port name description of I_{OL1}/I_{OH1} Changed “V_{iH1}” to “V_{IH1}” - 7.3 DC Electrical Characteristics (2/2) (Consumption current) Added specification of code flash 1.0MB or less Added 0 to ch0/ 3 to ch3 of TSPI in Table 7.3. - 7.4 12-bit AD Converter Characteristics Added specification of code flash 1.0MB or less (All products same specification) - 7.9.2.1 AC Measurement Conditions Temperature range of Ta was modified - 7.9.3.1 AC Measurement Conditions Temperature range of Ta was modified - 7.9.4.5 AC Electrical Characteristics Modified “EA/EAD[15:0] input” to “ED/EAD[15:0] input” in Figure 7.20 - 7.9.5.1 AC Electrical Characteristics Modified “fsys” of Ta to “fsysh” - 7.9.6.1 AC Electrical Characteristics Modified “fsys” of Ta to “fsysh” - 7.9.7.1 AC Measurement Conditions Temperature range of Ta was modified - 7.9.9.1 AC Measurement Conditions Temperature range of Ta was modified - 7.10.3 Chip Erase Added specification of code flash 1.0MB or less

3.0	2018-05-28	- Features Modified maximum baud rate of FUART, 921.6kbps to 2.5Mbps Modified 1st line explanation of A-PMD - Changed order of section, "contents" and "Preface" - 3.1 List of Memory Sizes Modified code flash start address of TMPM4GxDF, 0x5E00000 to 0x5E000000 - 7.4 12-bit AD Converter Characteristics Deleted "-" from Conditions - 7.5 8-bit DA Converter Characteristics Deleted "-" from Conditions - 7.6 Characteristics of Internal processing at RESET Deleted "-" from Conditions - 7.7 Characteristics of Power on Reset Deleted "-" from Conditions
4.0	2018-08-21	- Conventions Modified explanation of Trademark -2.1 LQFP176 Modified RTC0CLK to RTCOUT of PT3 -2.2 LQFP144 Modified RTC0CLK to RTCOUT of PT3 -2.3 LQFP128 Modified RTC0CLK to RTCOUT of PT3 -2.4 LQFP100 Modified RTC0CLK to RTCOUT of PT3 -4.1.3Control Pins Deleted Control pin from headline in Table 4.3 - 4.2 Functional Pin and Port Assignment Modified RTCCLK to RTCOUT in Table4.21 - 6.3 Control Pin Added explanation in MODE,BS - 7.9.1.2 AC Electrical Characteristics Corrected Value of t_{WDIS} in (2) Slave mode Corrected <CSnPOL>=0 to1, <CSnPOL>=1 to 0 in Figure 7.1,7.2,7.3 Deleted 1st clock edge sampling(Slave) - 7.9.4 External Bus Interface(EBIF) Added (EBIF) in title - 7.9.4.4 AC Electrical Characteristics(EEXBCLK asynchronous multiplex bus mode) Corrected Figure 7.14
4.1	2018-11-12	-Features Modified FIFO description of TSPI Modified "Trigger Start/Stop" to "Trigger Start" of T32A - 1 Block Diagram Modified JTAG to BSC in Figure 1.1 Modified Figure1.1 title -4.1.1 Peripheral Function Pins Modified function description of UTxCTS_N/ UTxRTS_N - 5.1 Reference Manuals Corrected "Mempry" to "Memory" in Table 5.1. - 5.10 Debug Interface Added Port information in Table 5.9. Deleted Previous Table5.10. - 5.16.2 Full Universal Asynchronous Receiver Transmitter Curcuit (FUART) Corrected chapter number 5.6.1 to 5.16.2. -5.21 12-bit Analog to Digital Converter (ADC) Corrected spelling error of 3rd line, "highset" to "highest". - 5.23 32-bit Timer Event Counter (T32A) Corrected spelling error of 4th line, "a interval" to "an interval". - 5.28 Boundary-scan Corrected Table title of Table5.30 - 7.1 Absolute Maximum Ratings Modified "Operational temperature" description in Table 7.1 -7.2 DC Electrical Characteristics(1/2)

		2nd table Condition added at the top right of the table 3rd table Modified the description of voltage at the top right of the table -7.3 DC Electrical Characteristics (2/2) (Consumption current) Corrected some spelling error in Table 7.3 -7.6 Characteristics of Internal processing at RESET Corrected "T_{IINIT}" to "t_{IINIT}", "T_{IRST}" to "t_{IRST}", "T_{pup}" to "t_{pup}", "T_{CPUWT}" to "t_{CPUWT}". -7.9.1.1 AC Measurement Condition Modified Ta condition -7.9.1.2 AC Electrical Characteristics Corrected value of t_{WL},t_{WH} 35 to 40, Corrected symbol of TSPIxSCK high level output pulse width "t_{WL}" to "t_{WH}" -7.9.2 I^2C Interface Corrected Title -7.9.3.2 AC Characteristics Corrected fsysm to ΦT0m in table Corrected symbol t_{PWH} to t_{PWL}, t_{PWL} to t_{PWH} Deleted T32AxINA0/T32AxINB0/T32AxINB0/T32AxINB1 from Figure 7.5 -7.9.4.1 AC Measurement Condition Modified Ta condition -7.9.4.3 AC Electrical Characteristics (EEXBCLK asynchronous Separate Mode) Corredted spelling error "rize" to "rise", Corrected spelling error "wiat" to "wait" in 6. Write cycle(external wait) -7.9.4.4 AC Electrical Characteristics (EEXBCLK asynchronous multiplex bus mode) Corredted spelling error "rize" to "rise" -7.9.4.5 AC Electrical Characteristics (EEXBCLK synchronous separate bus mode / multiplex bus mode) Corredted spelling error "rize" to "rise" -7.9.5.1 AC Measurement Condition Modified Ta condition -7.9.6.1 AC Measurement Condition Modified Ta condition -7.9.8.1 AC Measurement Condition Modified Ta condition -7.9.8.3 JTAG Interrupt Corrected Parameter of T_{d3} and T_{d4} -7.10.3 Chip Erase Delete User Information Area from Condition. Corrected 82.0 to 100.1 of Code Flash 1.5MB, Corrected 64.0 to 82.0 of Code Flash 1.0MB -7.12.1 Internal Oscillator Modified Symbl "IHOSC1" to "f_{IHOSC1}", "IHOSC2" to "f_{IHOSC2}" Modified description of Note2 -7.12.2 External Oscillator Modified Symbl "EHOSC" to "f_{EHOSC}", "ELOSC" to "f_{ELOSC}"
4.2	2019-03-26	- Added Commercial Product Data - Terms and Abbreviations Added BSC - 6.3 Control Pin Added R_{RST} to Pull-up - 7.9.8.2 SWD Interface Modified Parameter of T_{ds} - 7.9.8.3 JTAG Interface Modified Parameter of T_{ds}

Appendix

Part Naming Conventions



Package

Symbol	Package
QG	Plastic shrink quad outline non-leaded package; dry-packed
UG.DUG,FG, DFG	Plastic quad flat package; dry-packed
MG,DMG	Plastic small-outline package; dry-packed
XBG	Plastic ball grid array; dry-packed

Core

Symbol	Core
M4	ARM Cortex-M4
M3	ARM Cortex-M3
M0	ARM Cortex-M0

Product Group

Family	Group	Application
TXZ	H	For General-purpose/Consumer electronic equipment
	K	For Motor/Inverter control industrial equipment(MCU+AMP/COMP)
	G	For OA/Digital equipment/industrial equipment

ROM Size

Symbol	Size[KB]
M	32
P	48
S	64
U	96
W	128
Y	256
Z	384
D	512
E	768
10	1,023
15	1,536
20	2,048
40	4,096
80	8,192

Pin Count

Symbol	Pin count	Symbol	Pin count
0, G	Under 32pin	8, Q	129pin to 144pin
1, H	33pin to 44pin	9, R	145pin to 176pin
2, J	45pin to 48pin	A, S	177pin to 200pin
3, K	49pin to 52pin	B, T	201pin to 224pin
4, L	53pin to 64pin	C, U	225pin to 250pin
5, M	65pin to 80pin	D, V	251pin to 300pin
6, N	81pin to 100pin		
7, P	101pin to 128pin		

ROM Type

Symbol	Type
F	Flash
C	Mask

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, lifesaving and/or life supporting medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, and devices related to power plant. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative or contact us via our website.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

单击下面可查看定价，库存，交付和生命周期等信息

>>Toshiba(东芝)