TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (π -MOSVII)

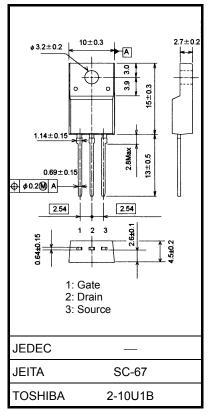
TK14A55D

Switching Regulator Applications

- Low drain-source ON-resistance: R_{DS (ON)} = 0.31 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}| = 6.5 \text{ S}$ (typ.)
- Low leakage current: I_{DSS} = 10 μ A (max) (V_{DS} = 550 V)
- Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1 mA)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V _{DSS}	550	V	
Gate-source voltage		V _{GSS}	±30	V	
Drain current	DC (Note 1)	۱ _D	14	А	
	Pulse (Note 1)	I _{DP}	56	A	
Drain power dissipation (Tc = 25°C)		PD	50	W	
Single pulse avalanche energy (Note 2)		E _{AS}	521	mJ	
Avalanche current		I _{AR}	14	А	
Repetitive avalanche energy (Note 3)		E _{AR}	5.0	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	–55 to 150	°C	



Weight: 1.7 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high

temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

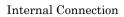
Thermal Characteristics

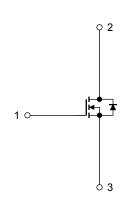
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	2.5	°C/W
Thermal resistance, channel to ambient	R _{th (ch-a)}	62.5	°C/W

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 4.6 mH, R_G = 25 Ω , I_{AR} = 14 A

This transistor is an electrostatic-sensitive device. Handle with care.





Start of commercial production 2008-10

Unit: mm

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

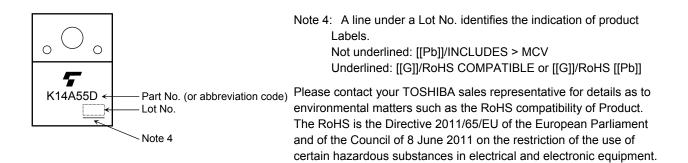
Electrical Characteristics (Ta = 25°C)

Char	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cu	rrent	I _{GSS}	$V_{GS}=\pm 30~V,~V_{DS}=0~V$			±1	μA
Drain cut-off curr	rent	I _{DSS}	$V_{DS} = 550 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			10	μA
Drain-source bre	akdown voltage	V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	550			V
Gate threshold v	oltage	V _{th}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 1 \text{ mA}$	2.0		4.0	V
Drain-source ON	l-resistance	R _{DS (ON)}	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 7 \text{ A}$		0.31	0.37	Ω
Forward transfer	admittance	Y _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 7 \text{ A}$	1.8	6.5		S
Input capacitance		C _{iss}			2300		
Reverse transfer capacitance		C _{rss}	$V_{DS} = 25 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$		10		pF
Output capacitance		C _{oss}]		250		
Switching time	Rise time	tr	$I_D = 7 \text{ A } V_{OUT}$		50	_	
	Turn-on time	t _{on}	$0 \vee \square \square \square \qquad \qquad$		100		ns
	Fall time	t _f			25		
	Turn-off time	t _{off}	Duty \leq 1%, t _W = 10 μ s	—	140	_	
Total gate charge		Qg			40		
Gate-source charge		Q _{gs}	$V_{DD} \approx 400 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 14 \text{ A}$		25		nC
Gate-drain charge		Q _{gd}			15		

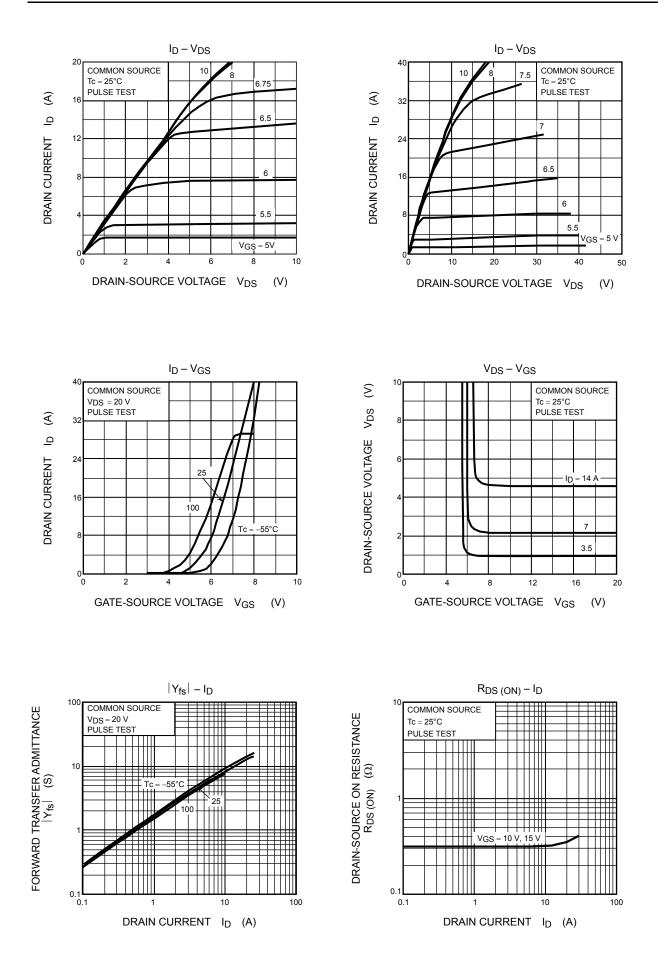
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	—	_	_	14	А
Pulse drain reverse current (Note 1)	I _{DRP}	—	_	_	56	А
Forward voltage (diode)	V _{DSF}	$I_{DR} = 14 \text{ A}, V_{GS} = 0 \text{ V}$	_	_	-1.7	V
Reverse recovery time	t _{rr}	$I_{DR} = 14 \text{ A}, V_{GS} = 0 \text{ V},$	_	1600	_	ns
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 100 A/μs	_	20	_	μC

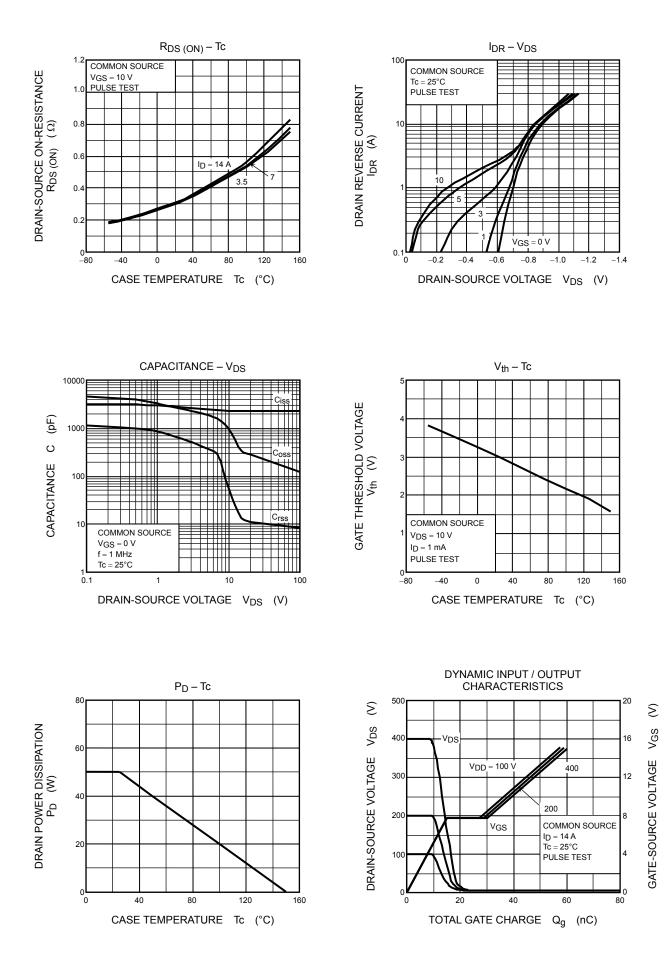
Marking

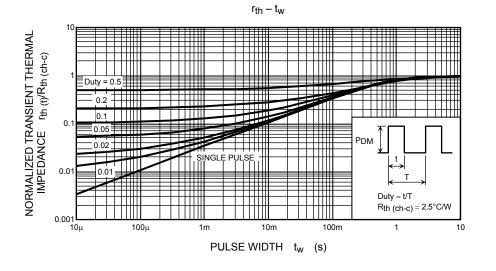


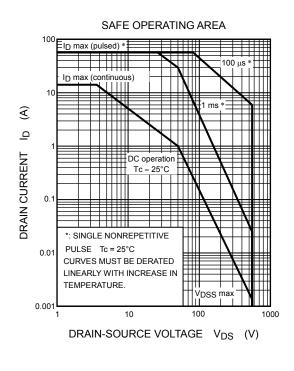
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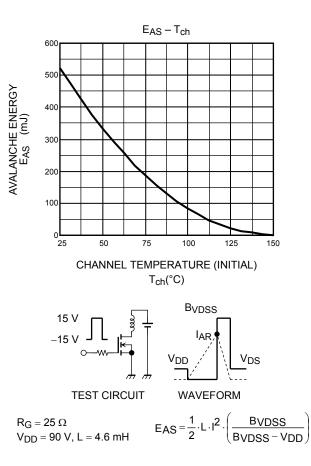


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