TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

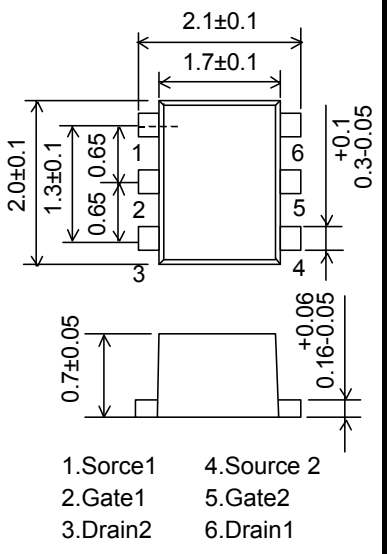
SSM6P54TU

○ High-Speed Switching Applications

○ Power Management Switch Applications

- 1.5 V drive
- Suitable for high-density mounting due to compact package
- Low on-resistance : R_{on} = 228 mΩ (max) (@ V_{GS} = -2.5 V)
  : R_{on} = 350 mΩ (max) (@ V_{GS} = -1.8 V)
  : R_{on} = 555 mΩ (max) (@ V_{GS} = -1.5 V)

Unit : mm



UF6	
JEDEC	—
JEITA	—
TOSHIBA	2-2T1B

Weight: 7.0 mg (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	-20	V
Gate-Source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	-1.2	A
	Pulse	I_{DP}	-2.4	
Drain power dissipation		P_D(Note 1)	500	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board.
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm^2)

Electrical Characteristics (Ta = 25°C)

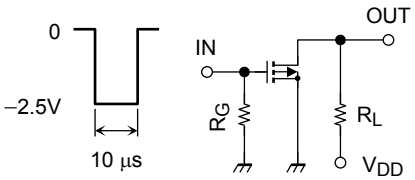
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−20	—	—	V
		$V_{(BR)\ DSX}$	I_D = −1 mA, V_{GS} = +8 V	−12	—	—	
Drain cut-off current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0	—	—	−10	μA
Gate leakage current		I_{GSS}	V_{GS} = ± 8 V, V_{DS} = 0	—	—	± 1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3 V, I_D = −1 mA	−0.3	—	−1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = -3 V, I_D = -0.6 A (Note 2)	1.7	3.4	—	S
Drain-Source on-resistance		$R_{DS\ (ON)}$	I_D = -0.6 A, V_{GS} = -2.5 V (Note 2)	—	162	228	mΩ
			I_D = -0.6 A, V_{GS} = -1.8 V (Note 2)	—	212	350	
			I_D = -0.1 A, V_{GS} = -1.5 V (Note 2)	—	249	555	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0, f = 1 MHz	—	331	—	pF
Output capacitance		C_{oss}		—	48	—	
Reverse transfer capacitance		C_{rss}		—	39	—	
Switching time	Turn-on time	t_{on}	V_{DD} = −10 V, I_D = −0.6 A, V_{GS} = 0 ~ −2.5 V, R_G = 4.7 Ω	—	19	—	ns
	Turn-off time	t_{off}		—	18	—	
Total gate charge		Q_g	V_{DS} = −16 V, I_{DS} = -1.2 A, V_{GS} = − 4 V	—	7.7	—	nC
Gate-Source charge		Q_{gs}		—	4.9	—	
Gate-Drain charge		Q_{gd}		—	2.8	—	
Drain-Source forward voltage		V_{DSF}	I_D = 1.2 A, V_{GS} = 0 (Note 2)	—	0.8	1.2	V

Note 2: Pulse test

Start of commercial production
2005-08

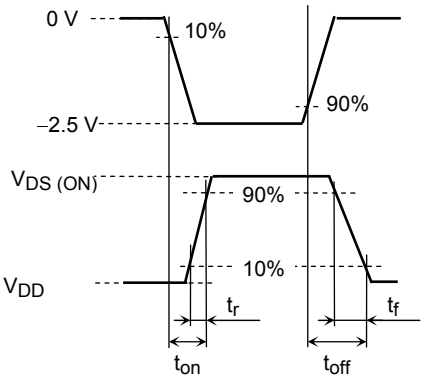
Switching Time Test Circuit

(a) Test Circuit



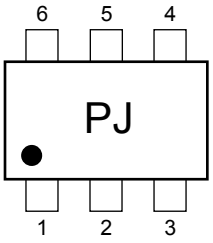
V_{DD} = -10 V
R_G = 4.7 Ω
Duty ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25 °C

(b) V_{IN}

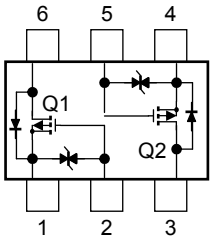


(c) V_{OUT}

Marking



Equivalent Circuit (top view)



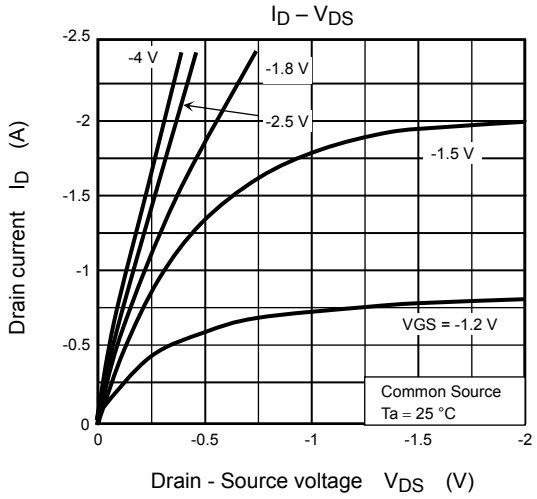
Precaution

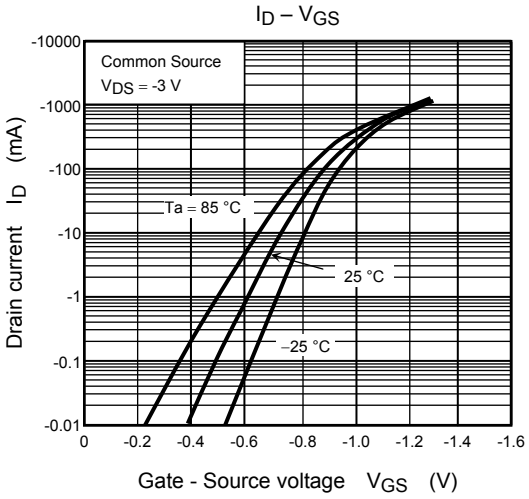
V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = -1mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than V_{th} and $V_{GS\ (off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

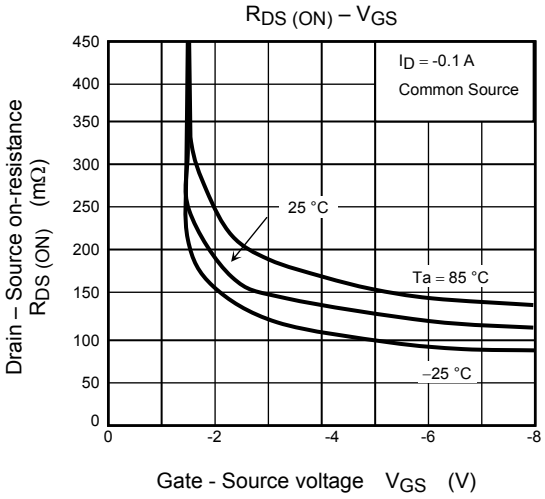
Be sure to take this into consideration when using the device.

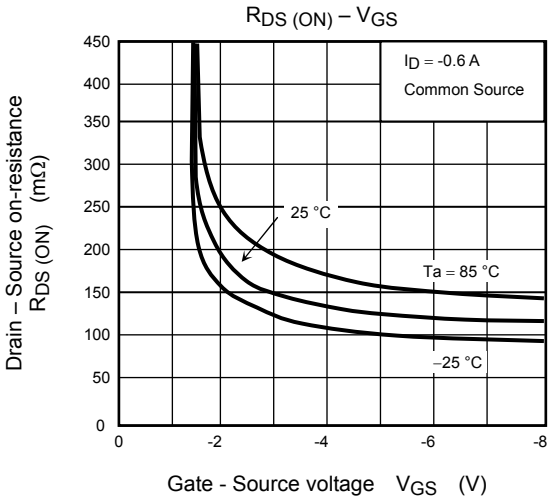
Handling Precaution

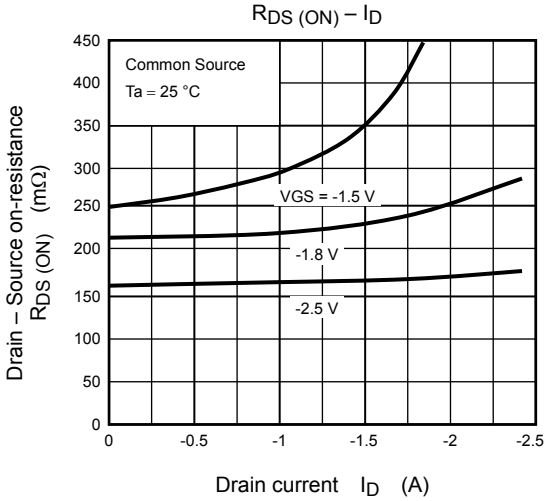
When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

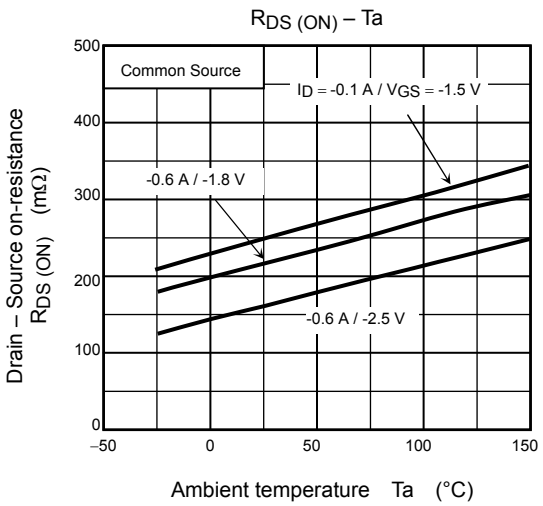




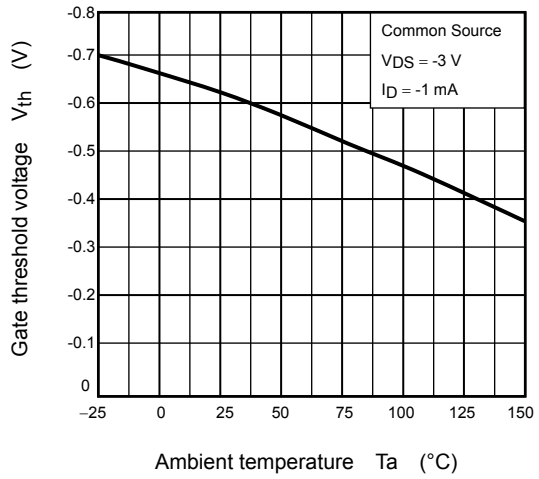




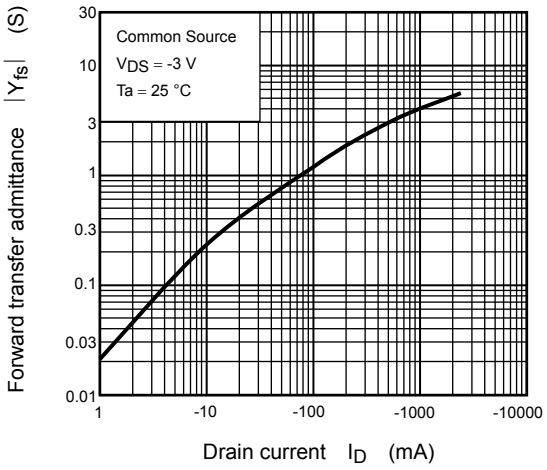




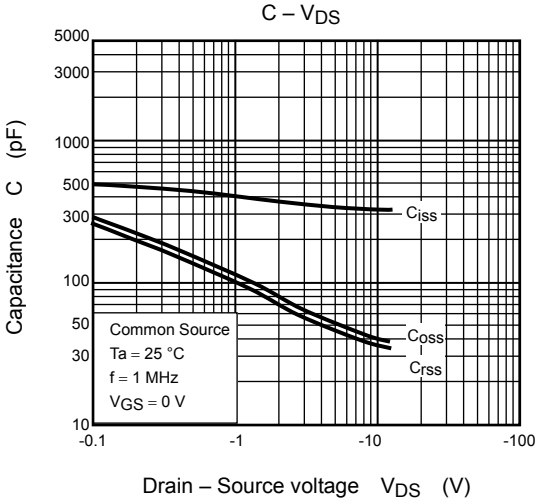
V_{th} – Ta



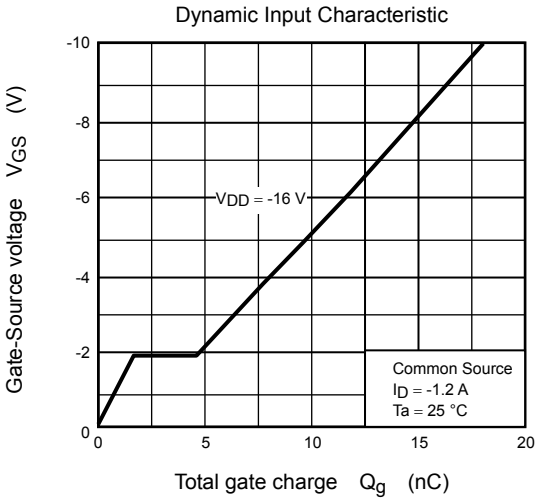
$|Y_{fs}|$ – I_D



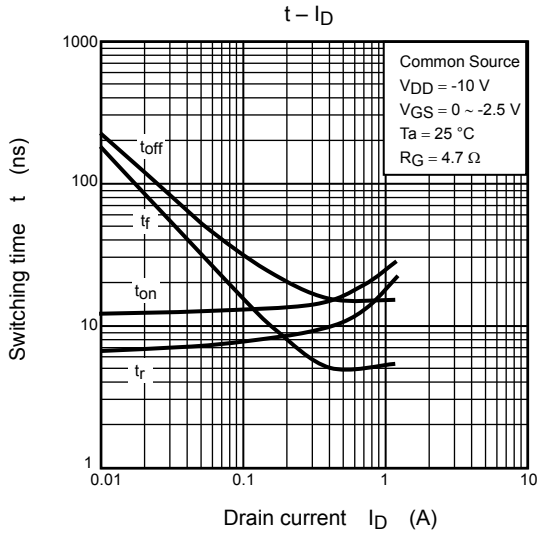
C – V_{DS}



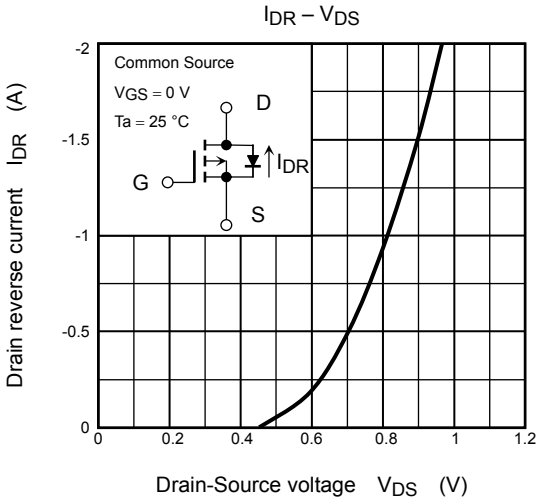
Dynamic Input Characteristic

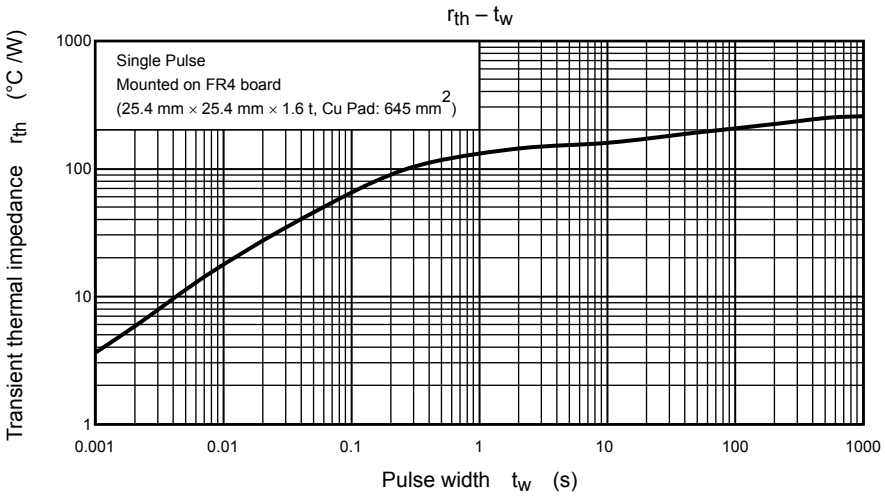


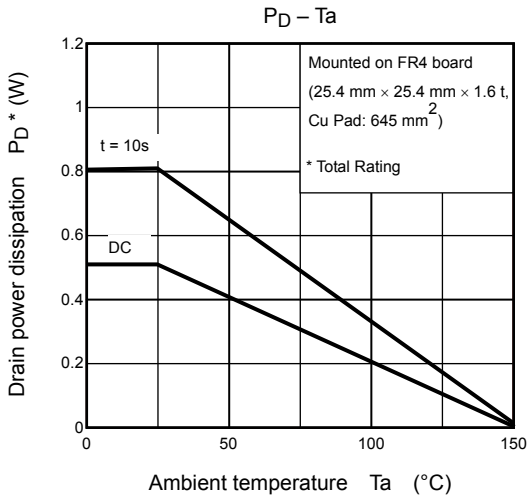
t – I_D



I_{DR} – V_{DS}







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