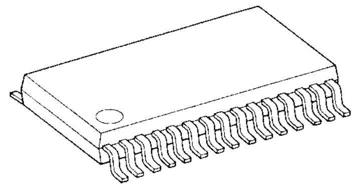
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB6634FNG

3-Phase Full-Wave Sine-Wave PWM Brushless Motor Controller

The TB6634FNG is designed for motor fan applications for three-phase brushless DC (BLDC) motors.

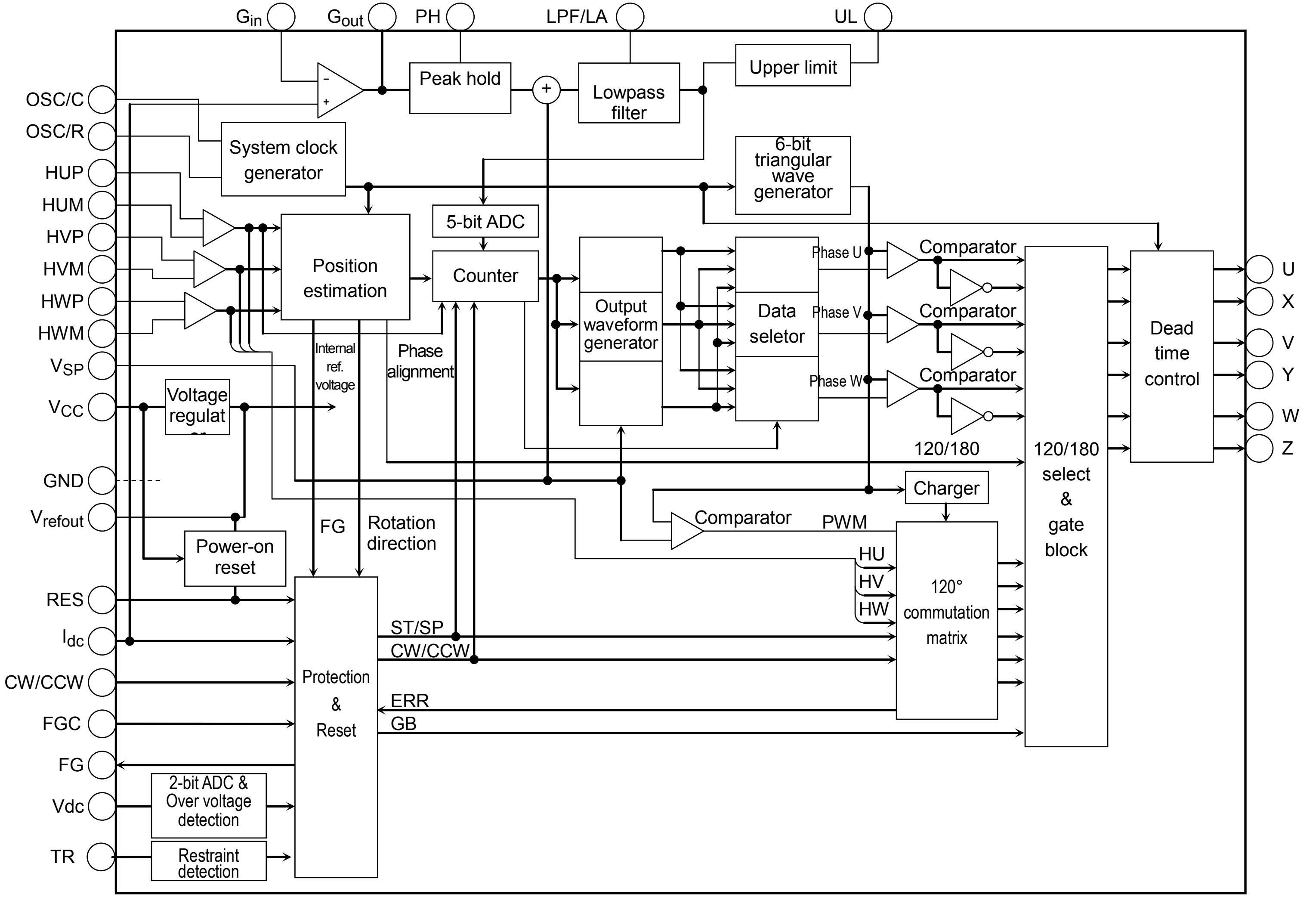


Weight: 0.17 g (typ.)

Features

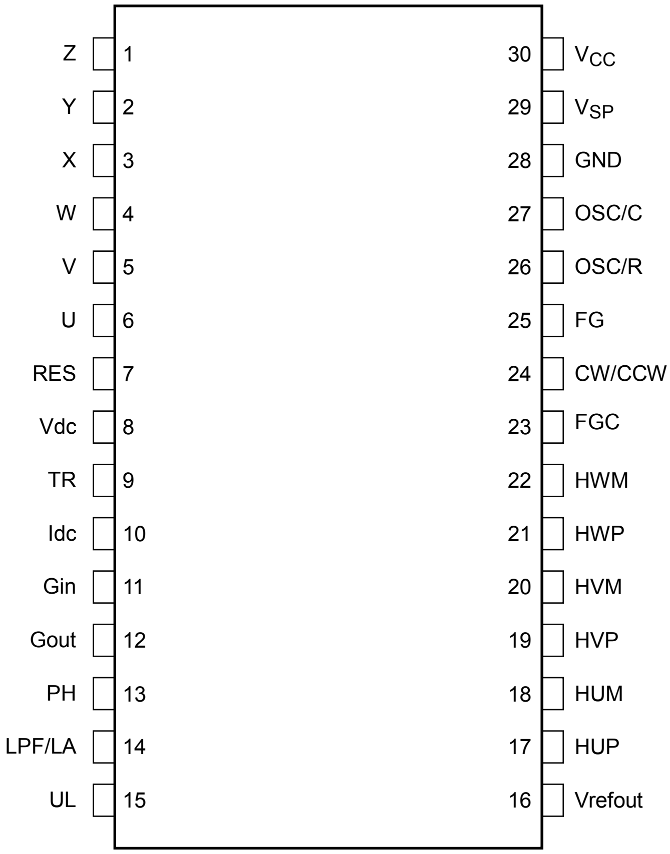
- Sine-wave PWM control
- Triangular-wave generator
  (with a carrier frequency of f_{OSC}/252 Hz)
- Lead angle control (0° to 58° in 32 separate steps)
- Lead angle external setting or automatic internal control
- Current-limiting input pin
- Voltage regulator (V_{refout} = 5 V (typ.), 30 mA (max))
- Operating supply voltage range: V_{CC} = 6 V to 16.5 V
- Motor restrained detection
- Motor supply voltage detection

Block Diagram



In the above block diagram, part of the functional blocks or constants may be omitted or simplified for explanatory purposes.

Pin Configuration

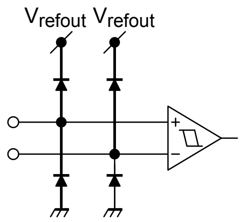
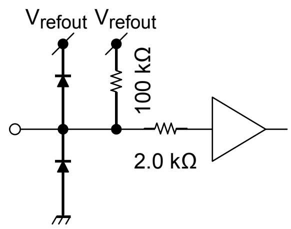
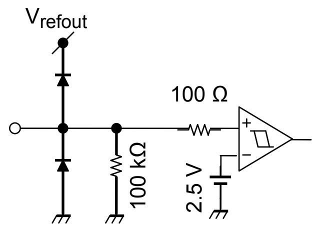
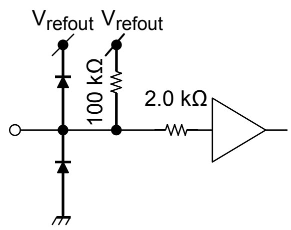
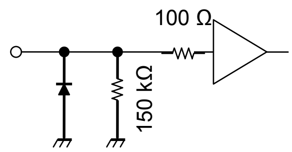
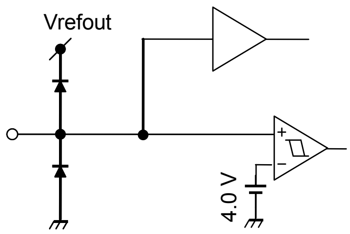


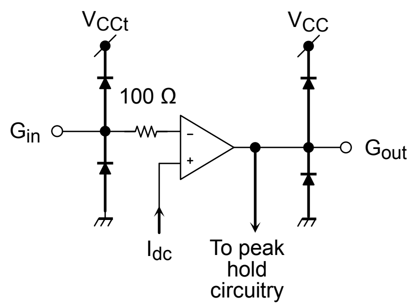
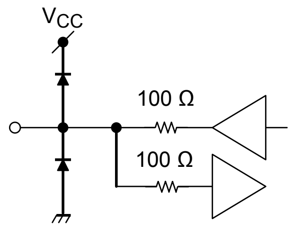
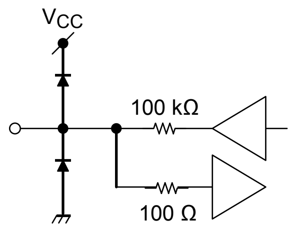
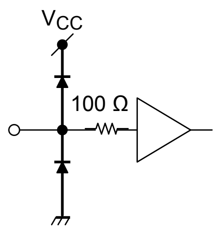
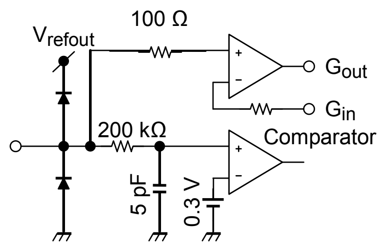
Pin Description

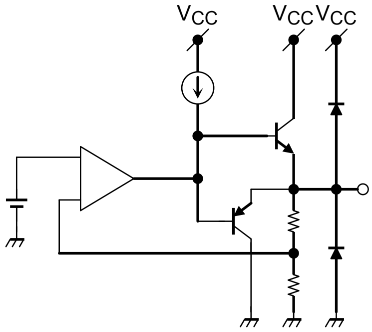
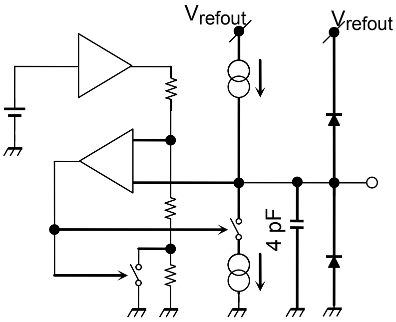
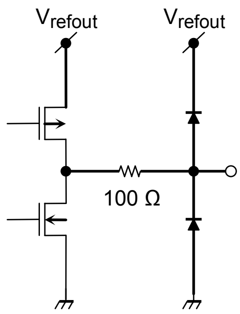
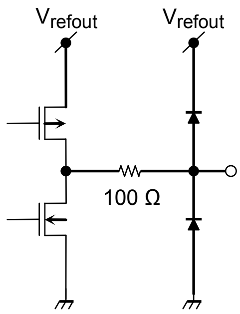
Pin No.	Symbol	Function	Description
1	Z	Commutation signal output, Z (low-side of W-phase)	High-active
2	Y	Commutation signal output, Y (low-side of V-phase)	
3	X	Commutation signal output, X (low-side of U-phase)	
4	W	Commutation signal output, W (high-side of W-phase)	
5	V	Commutation signal output, V (high-side of V-phase)	
6	U	Commutation signal output, U (high-side of U-phase)	
7	RES	Abnormal detection input	H: Runs the motor L: Stops the motor. (The commutation output signals are forced Low.) The RES input has an internal pull-down resistor.
8	Vdc	Motor supply voltage detection	Adjusting the number of steps addition of the lead angle by input voltage (2-bit AD) Over voltage detection Hysteresis: ± 0.1 V (typ.) 3.9 V (typ.) or less: Runs the motor. 4.1 V (typ.) or more: Stops the motor (The commutation output signals are forced Low).
9	TR	Motor restrained detection	Ratio of the driving term and the stopping term: 1:6.
10	Idc	Current limit control input	The DC-link current is applied to the Idc input. The reference voltage is 0.3 V. The Idc input has an internal RC filter and a digital filter.
11	Gin	Gain setting	The G_{IN} and G_{OUT} pins are used to amplify the Idc level so that the lead angle will be optimal.
12	Gout		
13	PH	Peak hold	A peak-hold capacitor and a discharge resistor are connected to this pin.
14	LPF/LA	Low pass filter/ Input lead angle setting	Connecting the capacitor for RC low pass filter (Built-in resistance of 100 kΩ) 0° to 58° in 32 separate steps.
15	UL	Upper limit of lead angle	Setting upper limit of the lead angle (UL = 0 V to 5.0 V)
16	Vrefout	Reference voltage output	5 V (typ.), 30 mA (max) A capacitor for oscillation prevention is connected to the V_{refout} output.
17	HUP	Position signal input, U	Gate block protection is activated when UVW = 111 or 000. These inputs have internal pull-up resistors and digital filters.
18	HUM		
19	HVP	Position signal input, V	
20	HVM		
21	HWP	Position signal input, W	
22	HWM		
23	FGC	FG output signal switch input	H or OPEN: FG = 3 ppr L: FG = 1 ppr The FGC input has an internal pull-up resistor.
24	CW/CCW	Clockwise/counterclockwise rotation	L: Clockwise rotation H: Counterclockwise rotation The CW/CCW input has an internal pull-up resistor.
25	FG	FG signal output	FGC = H or OPEN: 3 ppr output. FGC = L: 1 ppr output. ppr: one pulse per electrical angle
26	OSC/R	Oscillator resistor	CR oscillation
27	OSC/C	Oscillator capacitor	
28	GND	Ground	—
29	V_{SP}	Voltage command input	The V_{SP} input has an internal pull down resistor.
30	V_{CC}	Power supply	V_{CC} = 6 to 16.5 V

Input/Output Equivalent Circuits

Equivalent circuit diagrams may be partially omitted or simplified for explanatory purposes.

Pin	Symbol	Input/Output Signal	Internal Circuit
Position signal input U Position signal input V Position signal input W	HUP HUM HVP HVM HWP HWM	Analog Hysteresis: ±10.5 mV (typ.) Built-in digital filter 4 CLK@f_{OSC}	
Clockwise/counterclockwise rotation	CW/CCW	Digital H: V_{refout} -1 V (min) L: 0.8 V (max) H/open: Counterclockwise (CCW) L: Clockwise (CW)	
Abnormal detection	RES	Hysteresis comparator Hysteresis ± 0.1 V (typ.) Built-in digital filter 4 CLK@f_{OSC} H: 2.6 V (typ.) or more. L: 2.4 V (typ.) or less. H: Runs the motor L/open: Stops the motor (The commutation output signals are forced Low.)	
FG output signal switch input	FGC	Digital H: V_{refout} -1 V (min) L: 0.8 V (max) H/open: FG = 3 ppr L: FG = 1 ppr	
Voltage command signal	V_{SP}	Analog Input range: 0 to 10 V	
Motor supply voltage detection	V_{dc}	Adjusting the number of steps addition of the lead angle by input voltage (2-bit AD) Hysteresis ± 0.1 V (typ.) Over voltage detection Hysteresis ± 0.1 V (typ.) Built-in digital filter4 CLK@f_{OSC} 4.1 V (typ.) or more: Stops the motor. (Gate block protection) 3.9 V (typ.) or less: Runs the motor.	

Pin	Symbol	Input/Output Signal	Internal Circuit
Gain setting (Lead angle control circuitry)	Gin Gout	Non-inverting amplifier 25 dB max G_{out} output voltage Low: GND High: V_{CC} - 1.7 V	
Peak hold (Lead angle control circuitry)	PH	A peak-hold capacitor and a discharge resistor are connected to the PH pin. Recommended R/C: 100 kΩ/0.1 μF	
Lowpass filter/ Lead angle control input (Lead angle control circuitry)	LPF/LA	A capacitor for the RC lowpass filter is connected to this pin. A 100-kΩ (typ.) resistor is contained on-chip. Recommended C value: 0.1 μF In case lead angle is fixed externally, UL is connected to V_{refout}. Setting voltage is input to LA pin. Input range 0 to 5.0 V (V_{refout}) Input voltage of V_{refout} or more is fixed to maximum lead angle of 58°. Lead angle (5-bit AD) 0 V: 0° 5 V: 58°	
Upper limit for LA	UL	If the voltage applied to the LA input exceeds the upper limit set by this input, it is clipped to limit the lead angle. UL = 0 to 5.0 V	
Current limit control input	Idc	Analog filter time constant 1 μs (typ.) Digital filter 5 CLK@f_{OSC} When the Idc voltage exceeds 0.3 V (typ.), the commutation signal outputs low. (It is deactivated after a carrier cycle) If Ids is open, all the commutation outputs are disabled.	

Pin	Symbol	Input/Output Signal	Internal Circuit
Reference voltage output	V_{refout}	5 ± 0.5 V (30 mA (max))	
Motor restrained detection	TR	Capacitor connection for motor restrained detection 0.01 μF: Run: Stop (The commutation signal outputs low.) = 5 s: 30 s	
FG signal output	FG	Digital Push-pull output (±1 mA (max)) FGC = H/open 3 PPR output (3 pulses/electrical angle) FGC = L 1 PPR output (1 pulse/electrical angle)	
Commutation signal output U Commutation signal output V Commutation signal output W Commutation signal output X Commutation signal output Y Commutation signal output Z	U V W X Y Z	Digital Push-pull output (± 2 mA (max)) L: 0.78 V (max) H: V_{refout} - 0.78 V (min)	

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	18	V
Input voltage	V_{IN1}	-0.3 to V_{CC} (Note 1)	V
	V_{IN2}	-0.3 to V_{refout} +0.3 (Note 2)	
Output voltage	Vout	V_{refout} +0.3 (Note 3)	V
Input/Output voltage	Vinout	V_{CC} (Note 4)	
Output current	I_{OUT1}	1 (Note 5)	mA
	I_{OUT2}	2 (Note 3)	mA
Vrefout output current	I_{refout}	30 (Note 6)	mA
Power dissipation	P_D	1.1 (Note 7)	W
Operating temperature	T_{opr}	-30 to 115 (Note 8)	°C

Note 1: $V_{IN\ 1}$ pin: V_{SP}

Note 2: $V_{IN\ 2}$ pins:
HUP, HVP, HWP, HUM, HVM, HWM CW/CCW, RES, Idc, FGC, Gin, TR, OSC/R, OSC/C, and Vdc

Note 3: U, V, W, X, Y, and Z

Note 4: Gout, PH, LPF/LA, and UL

Note 5: FG

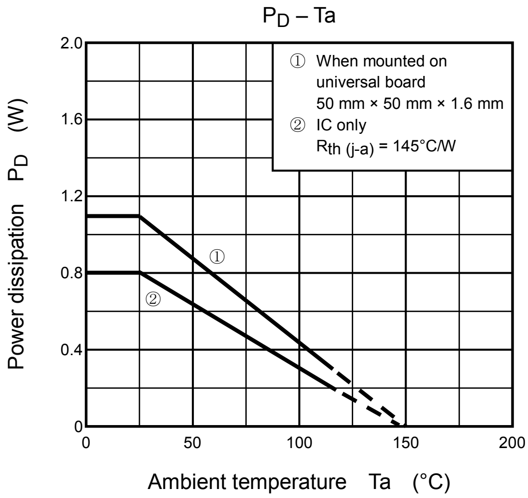
Note 6: Since the V_{refout} pin delivers a maximum output current of 30 mA, care should be exercised to the output impedance.

Note 7: When mounted on a universal board (50 mm × 50 mm × 1.6 mm, Cu 40 %)

Note 8: The operating temperature range is determined by the P_D - Ta characteristics.

Operating Ranges (Ta = 25°C)

Characteristics	Symbol	Min	Typ.	Max	Unit
Supply voltage	V_{CC}	6	15	16.5	V
Oscillation frequency	F_{osc}	3	4.5	6	MHz



Electrical Characteristics (Ta = 25°C, V_{CC} = 15 V)

Characteristics		Symbol		Test Condition	Min	Typ.	Max	Unit
Supply current		I_{CC}		V_{refout} = OPEN	—	6	9	mA
Input current		I_{IN1}		V_{IN} = 5 V V_{SP}	—	35	70	μA
		$I_{IN\ 2}$		V_{IN} = 5 V RES	—	50	100	
		$I_{IN\ 3}$		V_{IN} = 0 V CW/CCW, FGC	−100	−50	—	
Input voltage		V_{IN}	H	RES Stop → Drive	2.4	2.6	2.8	V
			L	RES Drive → Stop	2.2	2.4	2.6	
			Hys	RES	—	±0.1	—	
		V_{IN}	High	CW/CCW, FGC	V_{refout} −1	—	V_{refout}	V
			Low		—	—	0.8	
		V_{SP}	T	Sine-wave commutation ON duty = 92% (typ.)	8.2	—	10	V
			H	PWM duty 92%	5.1	5.4	5.7	
			M	Refresh → Motor startup	1.8	2.1	2.4	
			L	Commutation OFF → Refresh	0.7	1.0	1.3	
Hall effect inputs	Input sensitivity	V_S		Differential inputs	40	—	—	mVpp
	Common-mode input voltage	V_W			1.5	—	3.5	V
	Input hysteresis	V_H		Reference data (Note 1)	3	10.5	21	mV
Input delay time		T_{DT}		Hall sensor inputs (f_{OSC} = 4.5 MHz)	—	1.0	—	μs
		T_{DC}		I_{dc} (f_{OSC} = 4.5 MHz)	—	2.0	—	
Output voltage		$V_{OUT\ (H)\text{-}1}$		I_{OUT} = 2 mA U, V, W, X, Y, Z	V_{refout} −0.78	V_{refout} −0.3	—	V
		$V_{OUT\ (L)\text{-}1}$		I_{OUT} = −2 mA U, V, W, X, Y, Z	—	0.3	0.78	
		$V_{FG\ (H)}$		I_{OUT} = 1 mA FG	V_{refout} −1.0	V_{refout} −0.2	—	
		$V_{FG\ (L)}$		I_{OUT} = −1 mA FG	—	0.2	1.0	
		V_{refout}		I_{OUT} = 30 mA V_{refout}	4.5	5.0	5.5	
Output leakage current		$I_{L\ (H)}$		V_{OUT} = 0 V U, V, W, X, Y, Z	—	0	10	μA
		$I_{L\ (L)}$		V_{OUT} = V_{refout} U, V, W, X, Y, Z	—	0	10	
Dead time (cross conduction protection)		T_{OFF}		(f_{OSC} = 4.5 MHz), I_{OUT} = ± 2 mA,	1.7	2.0	2.3	μs
Current limit detection voltage		Vldc		I_{dc}	0.285	0.3	0.315	V
LA gain setting amp		AMP_{OUT}		GIN, G_{OUT} 100 kΩ/10 kΩ I_{dc} = Input 0.2 V I_{OUT} = 1 mA	2.0	2.2	2.4	V
		AMP_{OFS}		GIN, G_{OUT} 100 kΩ/10 kΩ I_{dc} = Input 0.2 V	—	5	—	mV
LA limit setting error		$T_{UL\ (2.5)}$		UL = 2.5 V, Hall IN = 100 Hz	26	30	33	°
LA peak hold output voltage		PHOUT		GIN, G_{OUT} 100 kΩ/10 kΩ I_{dc} = Input 0.2 V I_{OUT} = 5 mA	2.0	2.2	2.4	V
Lead angle correction		$T_{LA\ (0)}$		LPF/LA = 0 V, Hall IN = 100 Hz	—	0	—	°
		$T_{LA\ (2.5)}$		LPF/LA = 2.5 V, Hall IN = 100 Hz	26	30	33	
		$T_{LA\ (5)}$		LPF/LA = 5 V, Hall IN = 100 Hz	52	57	60	

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
V_{CC} monitor	V_{CC} (H)	Output turn-on threshold	4.2	4.5	4.8	V
	V_{CC} (L)	Output turn-off threshold	3.7	4.0	4.3	
	V_H	Input hysteresis width	—	0.5	—	
PWM oscillation frequency (Carrier frequency)	F_C (20)	OSC/C = 330 pF, OSC/R = 9.1 kΩ	18.45	20.5	22.55	kHz
	F_C (18)	OSC/C = 330 pF, OSC/R = 10 kΩ	16.65	18.5	20.35	
Maximum conduction duty cycle	T_{on} (max)	OSC/C = 330 pF, OSC/R = 10 kΩ V_{SP} = 5.7 V	89	92	95	%
Motor restrained detection	TONTR	TR = 0.01 μF Drive time Reference data (Note 1)	3.33	4.76	8.33	s
	TOFFTR	TR = 0.01 μF Stop time Reference data (Note 1)	20	28.57	50	s
	FTR	TR = 0.01 μF Frequency	65	105	150	Hz
Motor supply voltage detection	V_{dc3H}	V_{dc} Lead angle + 5.625° → Stop	3.9	4.1	4.3	V
	V_{dc3L}	V_{dc} Stop → Lead angle + 5.625°	3.7	3.9	4.1	V
	V_{dc2H}	V_{dc} Lead angle + 3.75° → Lead angle + 5.625°	2.9	3.1	3.3	V
	V_{dc2L}	V_{dc} Lead angle + 5.625° → Lead angle + 3.75°	2.7	2.9	3.1	V
	V_{dc1H}	V_{dc} Lead angle + 1.875°→ Lead angle + 3.75°	2.5	2.7	2.9	V
	V_{dc1L}	V_{dc} Lead angle + 3.75°→ Lead angle + 1.875°	2.3	2.5	2.7	V
	V_{dc0H}	V_{dc} Lead angle + 0°→ Lead angle + 1.875°	2.1	2.3	2.5	V
	V_{dc0L}	V_{dc} Lead angle + 1.875°→ Lead angle + 0°	1.9	2.1	2.3	V
	V_{dchys}	V_{dc} Input hysteresis width	—	±100	—	mV

Note 1: Not tested in production

Function Description

1. Basic Operation

In startup, the motor is driven by square-wave commutation signals that are generated according to the position signals. When the position signals indicate a rotational speed (f) of 1 Hz, the TB6634FNG estimates the rotor positions from the position signals and modulate them. The TB6634FNG then generates sine-wave by comparing the modulated signals against a triangular waveform.

From startup to 1 Hz: square-wave drive (120° commutation); $f = f_{OSC}/(750000 \times 6)$

Over 1 Hz: Sine-wave PWM drive (180° commutation); f will be approximately 1 Hz when f_{OSC} = 4.5 MHz

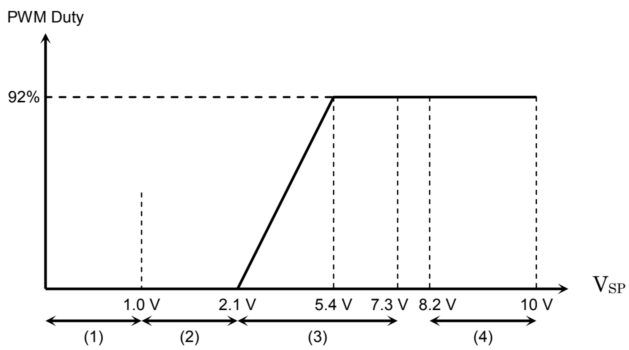
2. Voltage Command (V_{SP}) Signal and Bootstrap Voltage Regulation

(1) When $V_{SP} \le 1.0$ V:
The commutation signal outputs are disabled (i.e., gate protection is activated).

(2) When 1.0 V < $V_{SP} \le 2.1$ V:
The low-side transistors are turned on at a regular (PWM carrier) frequency. (The conduction duty cycle is approx. 8 %.) (Refresh)

(3) When 2.1 V < $V_{SP} \le 7.3$ V:
During sine-wave PWM drive, the commutation signals directly appear externally. During square-wave drive, the low-side transistors are forced on at a regular (PWM carrier) frequency. (The conduction duty cycle is approx. 8 %.)

(4) When 8.2 V ≤ V_{SP} ≤ 10 V (test mode):
The TB6634FNG operates in sine-wave mode at lead angle of zero. However, it operates in square-wave mode while it detects upwind.
The drive mode switches from square-wave drive to sine-wave PWM at a V_{SP} of 7.9 V typical.
The conduction duty cycle keeps the state as follows; 5.4 V typical ≤ V_{SP}. It is calculated as PWM_carrier_frequency × 92 % typical.

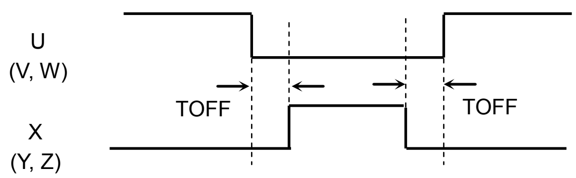


3. Dead Time Insertion (cross conduction protection)

To prevent a short-circuit between external low-side and high-side power elements during sine-wave PWM drive, a dead time is digitally inserted between the turn-on of one side and the turn-off of the other side. (The dead time is also implemented at the full duty cycle during square-wave drive.)

$T_{OFF} = 9/f_{OSC}$

$T_{OFF} \simeq 2.0$ μs when f_{OSC} = 4.5 MHz, where f_{OSC} is the reference clock frequency (i.e., CR oscillator frequency).



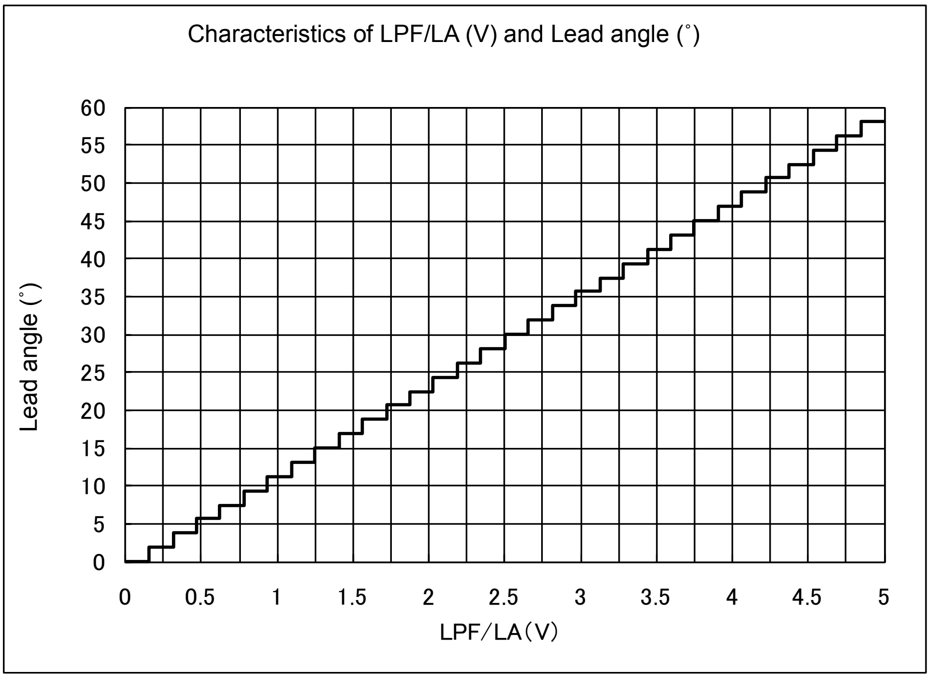
4. Lead Angle Control

The lead angle can be adjusted between 0° and 58° in 32 separate steps according to the induced voltage level on the LPF/LA input, which works with 0 to 5 V.

0 V = 0°

5 V = 58° (A lead angle of 58° is assumed when the LA voltage exceeds 5 V.)

Steps	LPF/LA (V)	Lead angle (°)	Steps	LPF/LA (V)	Lead angle (°)	Steps	LPF/LA (V)	Lead angle (°)
0	0.000	0.000	11	1.719	20.625	22	3.438	41.250
1	0.156	1.875	12	1.875	22.500	23	3.594	43.125
2	0.313	3.750	13	2.031	24.375	24	3.750	45.000
3	0.469	5.625	14	2.188	26.250	25	3.906	46.875
4	0.625	7.500	15	2.344	28.125	26	4.063	48.750
5	0.781	9.375	16	2.500	30.000	27	4.219	50.625
6	0.938	11.250	17	2.656	31.875	28	4.375	52.500
7	1.094	13.125	18	2.813	33.750	29	4.531	54.375
8	1.250	15.000	19	2.969	35.625	30	4.688	56.250
9	1.406	16.875	20	3.125	37.500	31	4.844	58.125
10	1.563	18.750	21	3.281	39.375	32	5.000	58.125



Note: Be careful in using the TB6634FNG because the upper of lead angle is limited to about 25 steps when the range of the power supply voltage V_{CC} is 6 V to 7 V.

5. PWM Carrier Frequency

The triangular waveform generator provides a carrier frequency of $f_{OSC}/252$ necessary for PWM generation. (The triangular wave is also used to force the switch-on of low-side transistors during square-wave drive.)

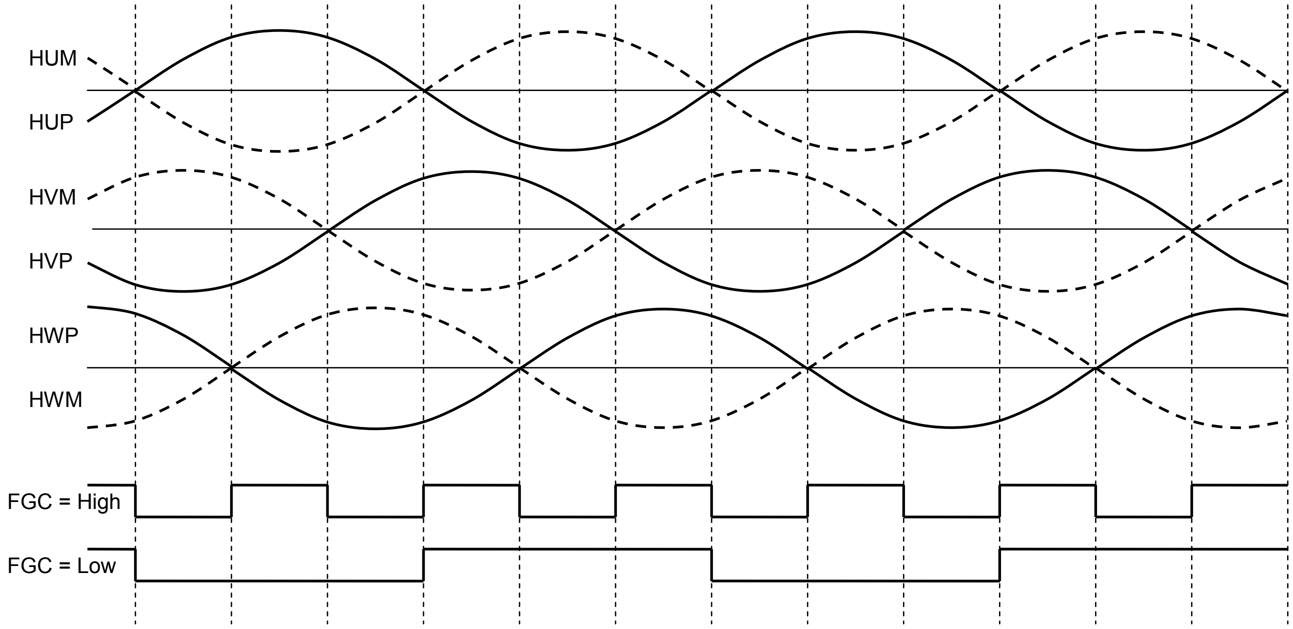
Carrier frequency: FC = $f_{OSC}/252$ (Hz), where f_{OSC} = reference clock (crystal oscillator) frequency

6. Rotation Pulse Output

Rotation pulse based on the hall signal is outputted. FGC terminal switches 1 pulse/electrical angle and 3 pulses/electrical angle. One pulse/electrical angle is generated by the hall signal of U phase. Three pulses/electrical angle are generated by combined each up-down edge of U phase, V phase, and W phase.

FGC	FG
High or Open	3 pulses/electrical angle
Low	1 pulse/electrical angle

Timing Chart of FG Signal



7. Abnormal Detection Input Pins

(1) Overcurrent protection (Idc pin)

If the voltage of the DC-link current exceeds the internal reference voltage, the commutation signals are forced Low. Overcurrent protection is disabled after every carrier period.

Reference voltage = 0.3 V (typ.)

(2) Abnormal detection input (RES pin)

When the RES input is Low, the commutation outputs are disabled. When the RES input is then set High, abnormal detection is disabled after every carrier period and the commutation outputs are re-enabled.

Any irregular conditions of the motor should be detected by external hardware; such indications should be presented to the RES input.

RES Pin	Commutation Output Signals (U, V, W, X, Y, Z)
High	The motor can be driven
Low or Open	Low (Gate block protection)

When RES is Low, charging of the bootstrap capacitor stops.

In order to charge the bootstrap capacitor in recovering, input the voltage as follows;

$1.0\ V < V_{SP} \leq 2.1\ V$

(3) Abnormal position signal protection

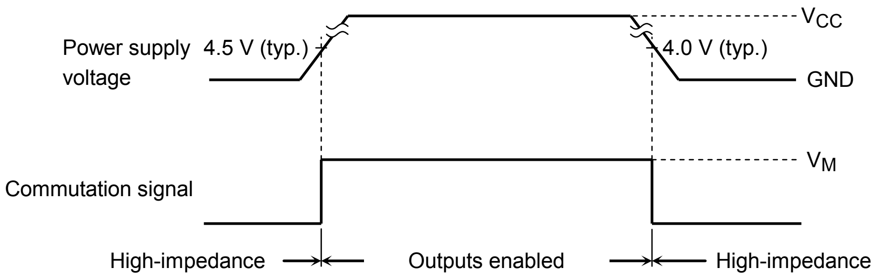
When the position signal inputs (UVW) are all Highs or all Lows, the commutation outputs are forced off (i.e., Gate block protection). When these inputs are then set to any other combination, the commutation outputs are re-enabled. (The all-High and all-Low conditions are Hall sensor outputs.)

Position detection signal (internal hall amplifier output) in sine-wave PWM drive mode is constructed with latch circuit.

So, some noise or chattering do not invite errors in driving because prior mode is kept in case the position detection signal outputs different voltage from the expected one.

(4) Undervoltage lockout (V_{CC} monitor)

While the power supply voltage is outside the rated range during power-on or power-off, the commutation outputs are set to the high-impedance state to prevent external power elements from damage due to short-circuits.



8. Motor Restrained Protection

When hall signal continues to detect below state, intermittent operation (period of operation: period of halt = 1:6) is repeated.

<State of motor restrained protection>

Operation starts and the restrained protection starts counting when V_{SP} exceeds 2.1 V. In case rotation direction of the motor is the same as the set direction (CW: 180° conduction mode), the motor restrained protection operates under the condition that the hall signal outputs with 1 Hz (f_{osc} = 4.5 MHz) or less in the square-wave drive mode (120° conduction).

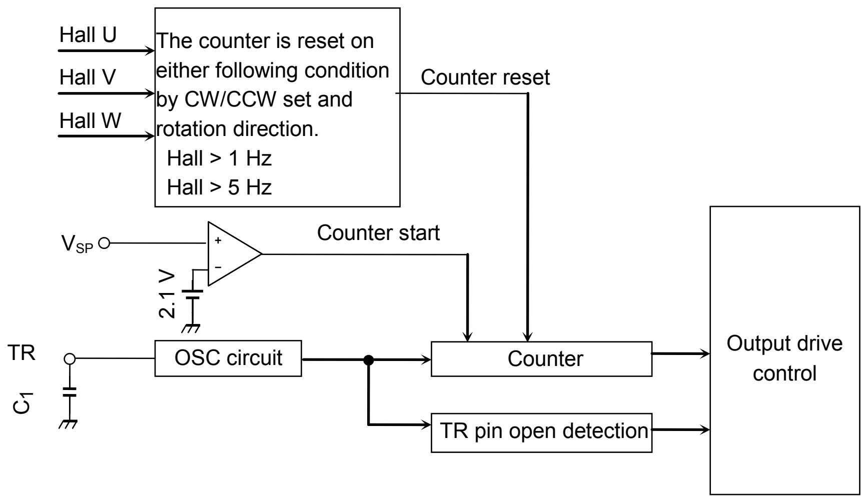
In case rotation direction of the motor is opposite of the set direction (CCW: 120° conduction mode of the inverted hall input), the motor restrained protection operates under the condition that the hall signal outputs with about 5 Hz (f_{osc} = 4.5 MHz) or less.

When motor restrained protection operates, conducting output is set low during turning off.

In case V_{SP} is set 2.1 V or less during operation, the counter starts from initial state after reset. However, the counter does not reset and the term of turning off continues though V_{SP} is set 2.1 V or less during turning off.

Operation of motor restrained protection

CW/CCW	V_{SP} > 2.1 V		V_{SP} ≤ 2.1 V
	Motor rotation direction		-
	CW	CCW	
Low (CW)	Operation ≤ 1 Hz (Same as set direction by CW/CCW pin)	Operation ≤ 5 Hz (Opposite of set direction by CW/CCW pin)	Non active
High (CCW)	Operation ≤ 5 Hz (Opposite of set direction by CW/CCW pin)	Operation ≤ 1 Hz (Same as set direction by CW/CCW pin)	Non active



<Setting>

Term of detection and that of turning off can be set by the external capacitor (C1) of TR terminal.

- Setting time

Operation term Ton[s] = C1 × (VH — VL) × 2/I × 500 counters

Turning off term Toff [s] = C1 × (VH — VL) × 2/I × 3000 counters (Note 1)

- Ex: When C1 is 0.01 μF, I is 3.15 μA (typ.), VH is 2 V (typ.), and VL is 0.5 V (typ.). And so, Ton[s] is 4.76 s (typ.) and Toff[s] is 28.57 s (typ.).

Note 1: In turning off term, the boot strap capacitor is not charged (refresh).
In order to charge the boot strap capacitor in recovering operation, input command voltage as follows; 1.0 V < V_{SP} ≤ 2.1 V.

Note 2: Conducting output is low (turning off state) when open detection operates under the condition that TR pin is open.

Note 3: The counter is not increased any more by applying fixed voltage (GND) to TR pin. And operation state continues because the motor restrained protection stops operation.

9. Motor supply voltage detection

The change of the motor power supply voltage can be monitored because lead angle can be corrected (Four levels of lead angle are increased based on LPF/LA) and the operation can be halted (gate block protection) by inputting voltage to Vdc pin.

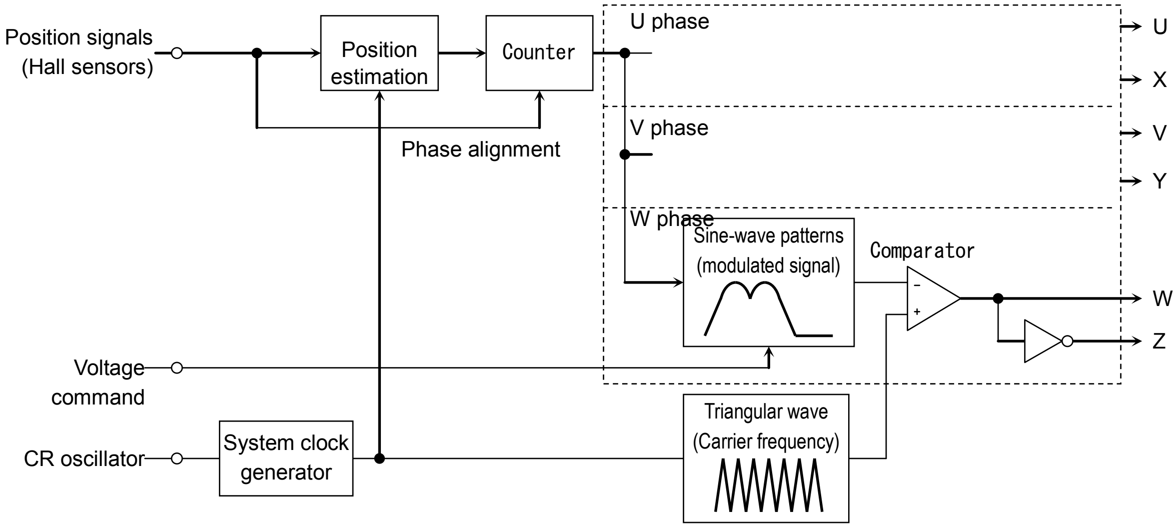
Voltage of Vdc pin (typ.) (Note 1)	Functions
4.0 V to Vref+0.3 V	Conducting signal output is Low(gate block protection) (Note 2)
3.0 V to 4.0 V	Lead angle (LPF/LA) + 3 levels (5.625°)
2.6 V to 3.0 V	Lead angle (LPF/LA) + 2 levels (3.75°)
2.2 V to 2.6 V	Lead angle (LPF/LA) + 1 level (1.875°)
0 V to 2.2 V	Lead angle (LPF/LA) + 0 level

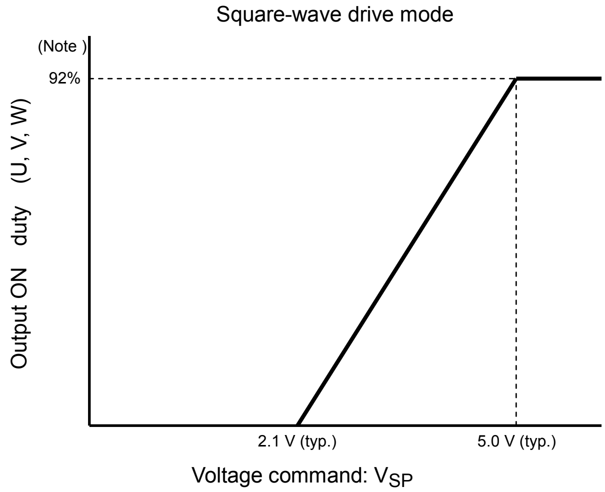
Note 1: Threshold voltage of Vdc is different between rising state and falling state because it has the hysteresis width of 100 mV (typ.).

Note 2: It is released on every carrier frequency.

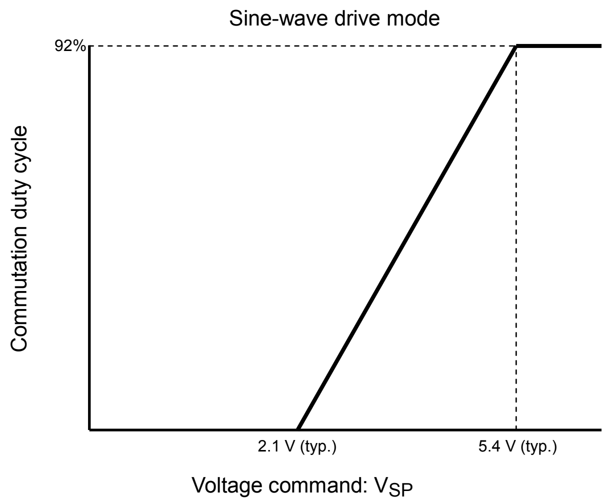
The boot strap capacitor is not charged (refresh) in turning off.
In order to charge the boost strap capacitor in recovering, input the command voltage as follows; $1.0\ V < V_{SP} \leq 2.1\ V$.

Operation Flow





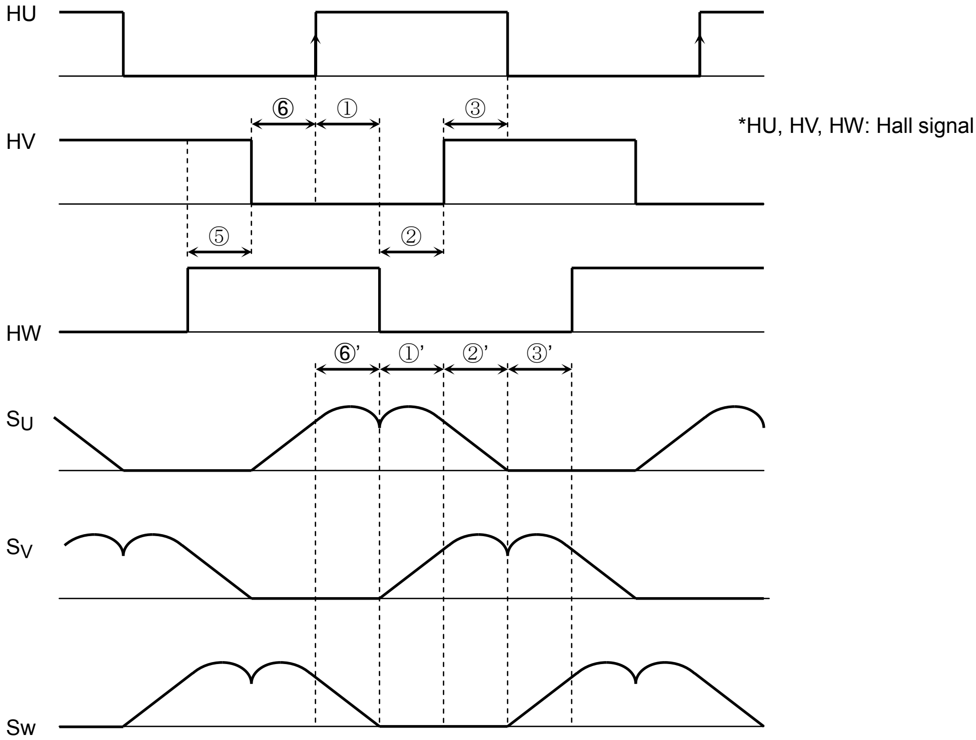
Note: The conduction period is reduced by the dead time. (carrier_frequency × 92% − Td × 2)



The position signals from Hall sensors are modulated, and the modulated signals are then compared against a triangular waveform to generate a sine-wave PWM.

The counter measures the period from given rising (or falling) edges of three hall signals to their next falling (or rising) edges (60 electrical degrees). This period is then used as 60° phase data for the next modulation.

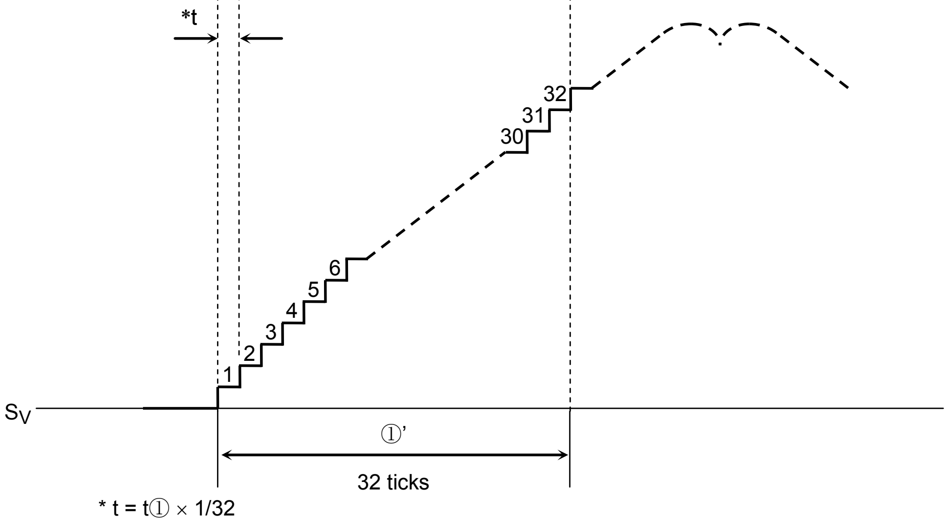
A total of 32 ticks comprise 60 electrical degrees; the length of a tick equals 1/32nds the time period of the immediately preceding 60° phase.



In the above diagram, the modulated waveforms have an interval (①') equal to 1/32nds of the interval between a rising edge of HU to a falling edge of HW (①) of the previous cycle.

Likewise, the modulated waveforms have an interval (②') equal to 1/32nds of the interval between a falling edge of HW to a rising edge of HV (②) of the previous cycle.

If 32 ticks finish modulated before ①' or ②' ends, next 32 ticks modulate with the same time width until the next falling edge.



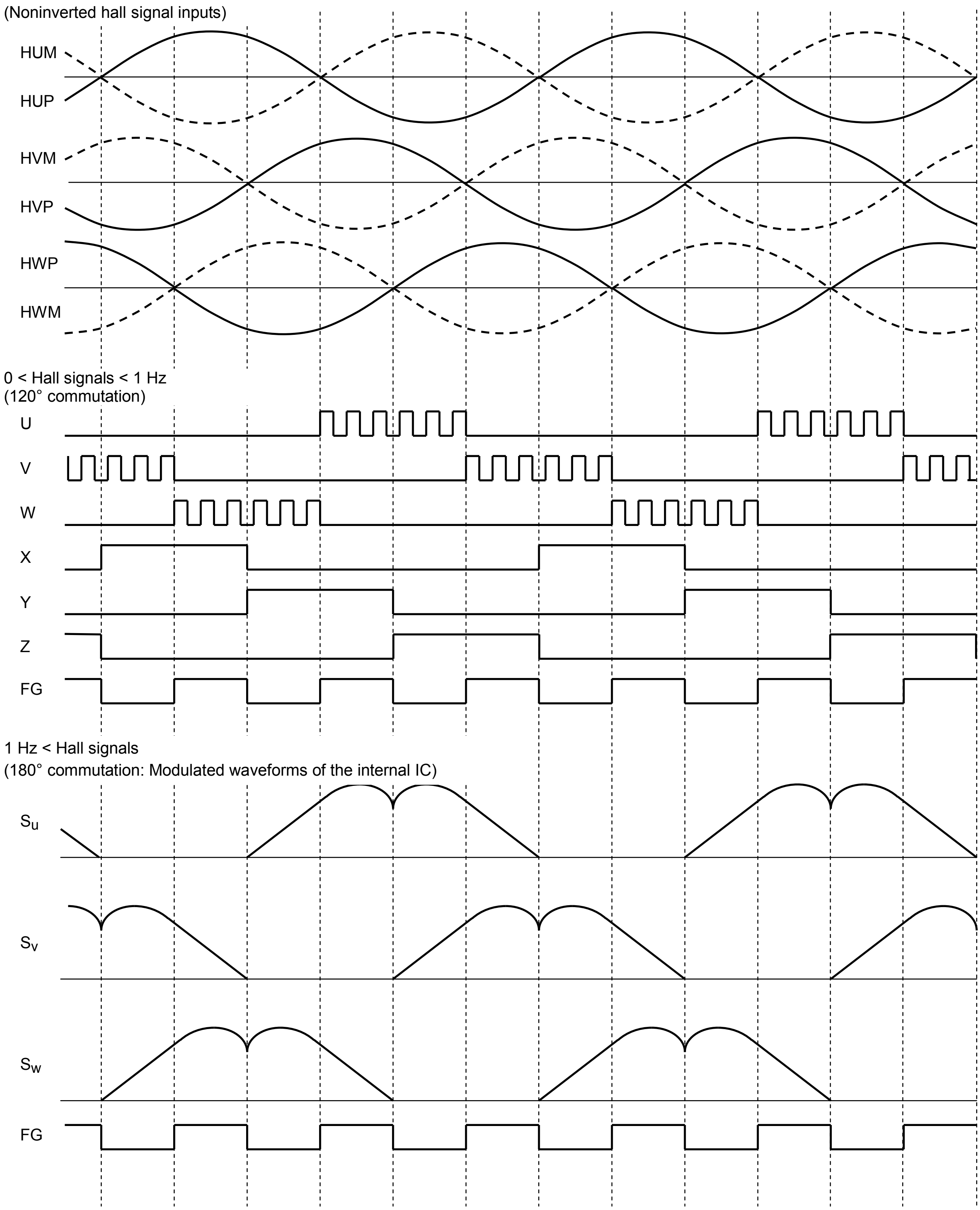
Moreover, the phase match with the modulated waveform is done at every zero crossing of the positional detection signal.

The modulated waveform is reset on each falling or rising edge of the positional detection signal, which occurs every 60° electrical degrees.

Therefore, the modulated waveform becomes discontinuous at each reset while the position of the hall signal misaligns or the motor is accelerating or decelerating.

Note: In the above diagram, HU is shown as square waveforms for the sake of simplicity.

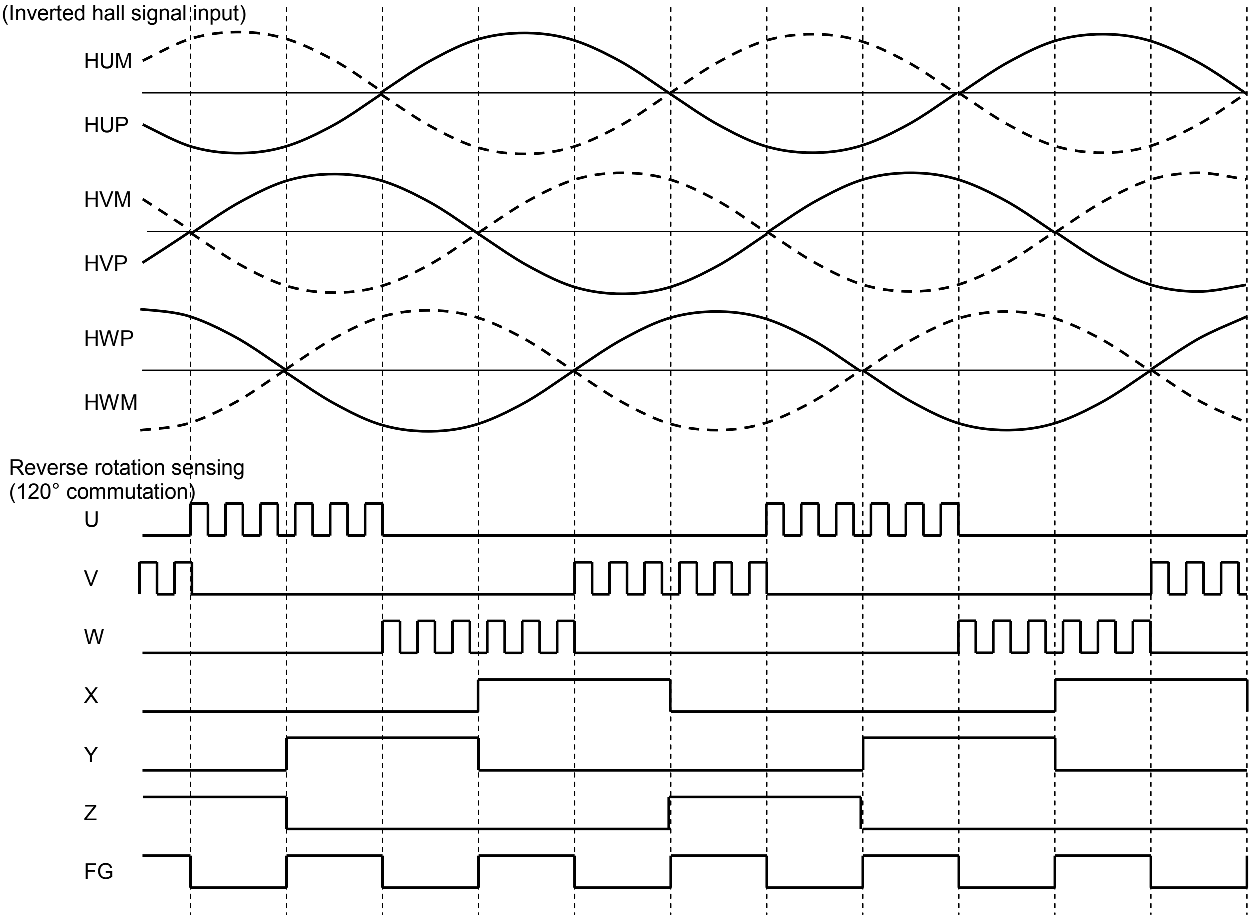
Forward Rotation Timing Chart (CW/CCW = Low, LPF/LA = GND, FGC=High)



*: When the Hall input frequency is equal to or greater than 1 Hz (@ f_{OSC} = 4.5 MHz), lead angle control is activated according the LPF/LA input.

The above timing chart is simplified to illustrate the function and behavior of the device.

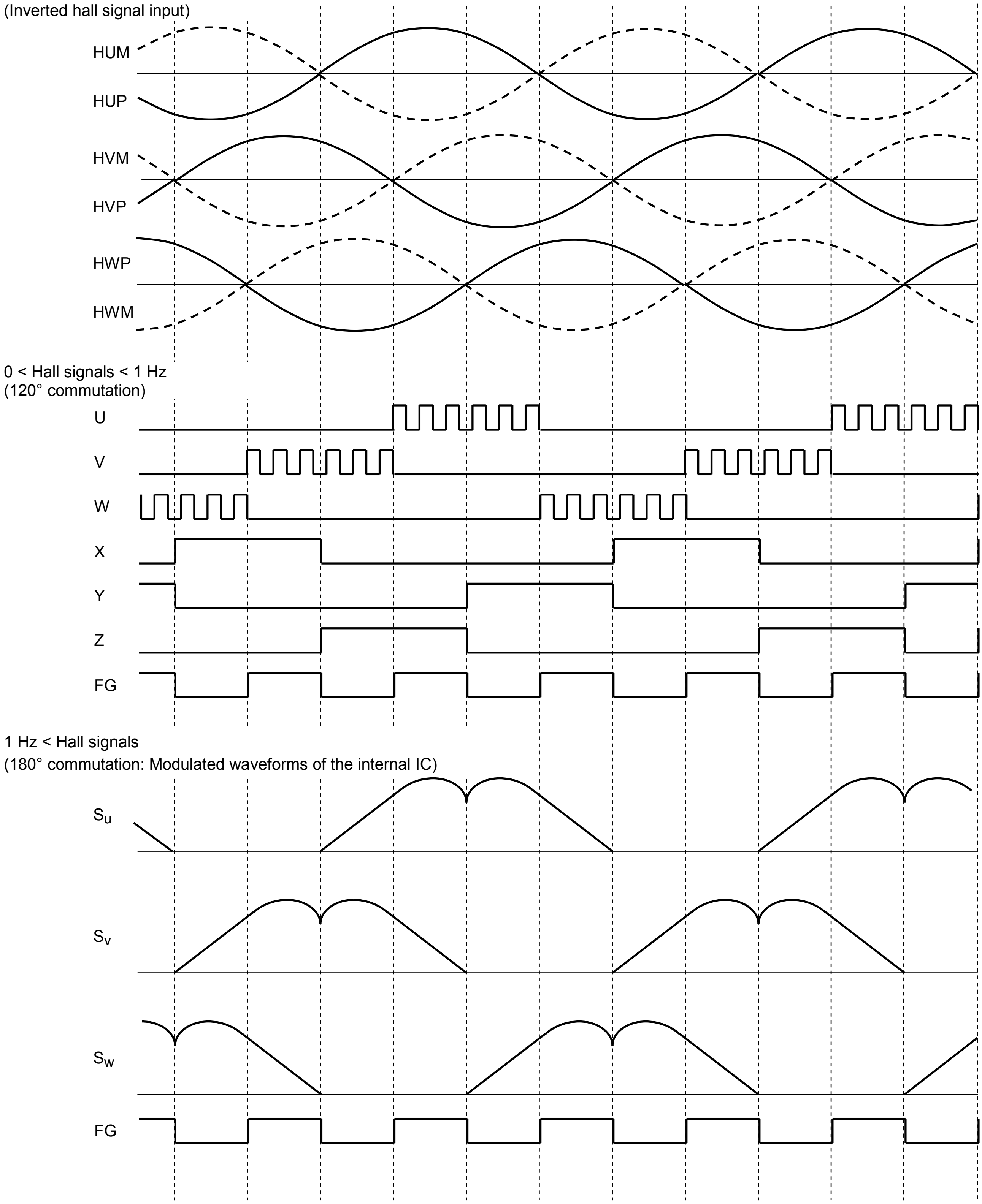
Forward Rotation Timing Chart (CW/CCW = Low, LPF/LA = GND, FGC = High)



*: When the inverted Hall signal is inputted while CW/CCW is Low, The IC drives in 120° commutation mode with a lead angle of 0° (reverse rotation).

The above timing chart is simplified to illustrate the function and behavior of the device.

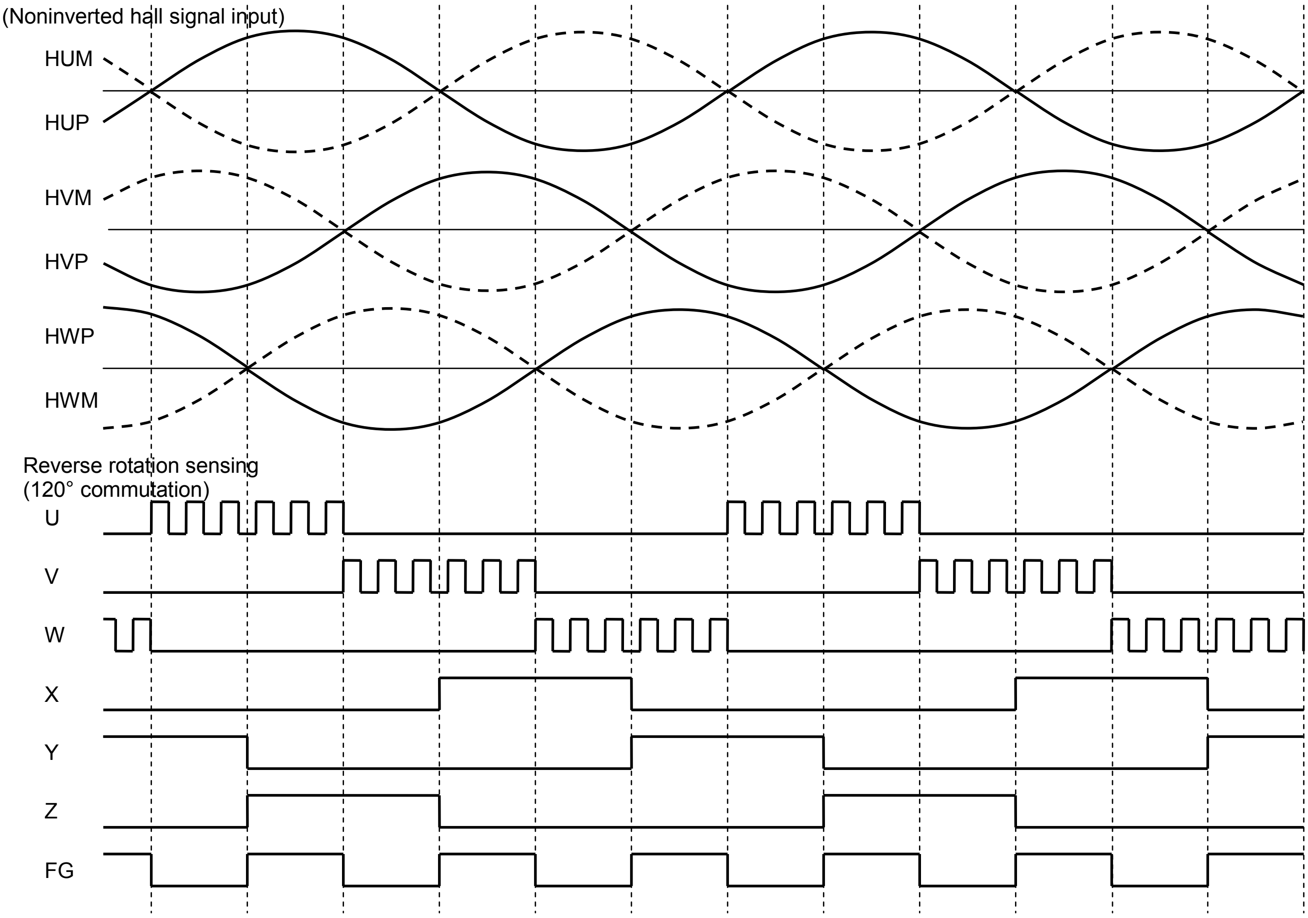
Reverse Rotation Timing Chart (CW/CCW = High, LPF/LA = GND, FGC = High)



*: When the Hall input frequency is equal to or greater than 1 Hz (@ f_{OSC} = 4.5 MHz), lead angle control is activated according the LPF/LA input.

The above timing chart is simplified to illustrate the function and behavior of the device.

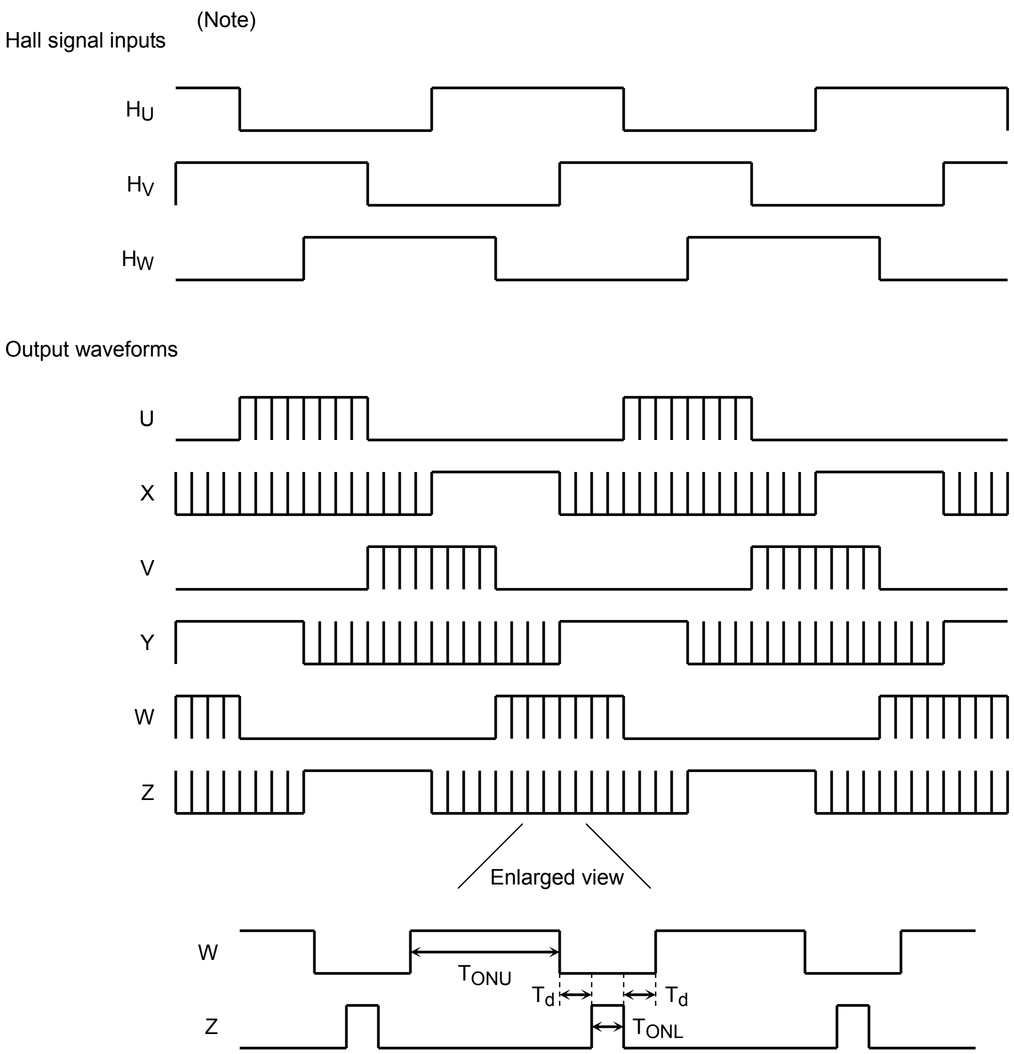
Reverse Rotation Timing Chart (CW/CCW = High, LPF/LA = GND, FGC = High)



*: When the noninverted Hall signal is inputted while CW/CCW is High, the IC drives in 120° commutation mode with a lead angle of 0° (reverse rotation).

The above timing chart is simplified to illustrate the function and behavior of the device.

Square-Wave Drive Waveform (CW/CCW = Low)



Note: Square waveforms are used in the above diagram for the sake of simplicity.

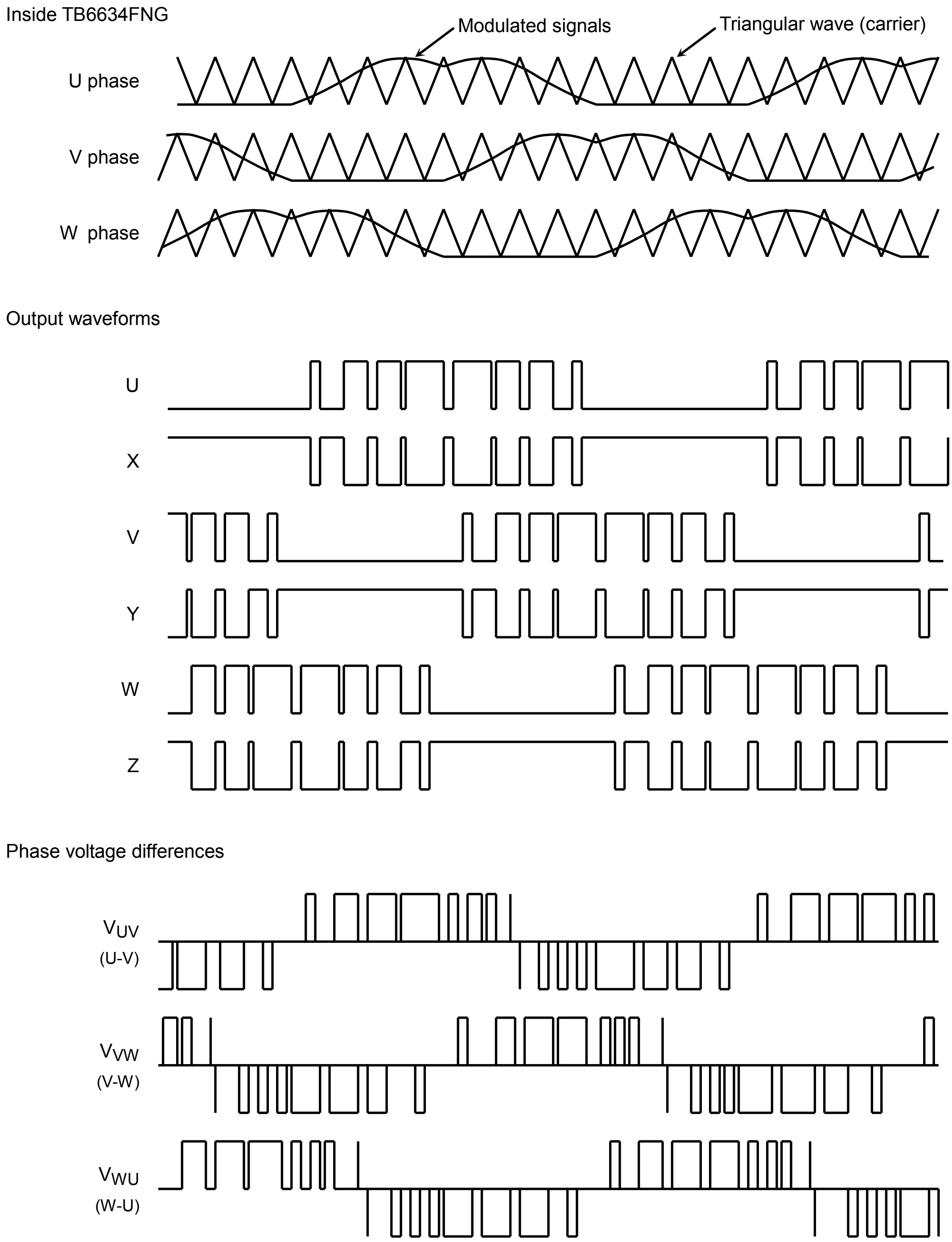
To obtain an adequate bootstrap voltage, the low-side outputs (X, Y and Z) are always turned on for eight percent of the carrier period (T_{ONL}) even during the off time of the low side in 120° commutation mode. As shown in the enlarged view, the high-side outputs (U, V and W) are turned off for a dead time period while the low-side outputs are on. (Td varies with the V_{SP} input.)

Carrier frequency = $f_{osc}/252$ (Hz) Dead time: Td = $9/f_{osc}$ (s) ($V_{SP} \geq 5.0$ V, Td = Low)
TONL = carrier_frequency × 8% (s) (Constant regardless of the V_{SP} input)

In square-wave drive mode, the changing of the motor speed is enabled, depending on the V_{SP} voltage; the motor speed is determined by the duty cycle of TONU.

Note: At startup, the motor is driven by a square wave when the Hall signal frequency is 1 Hz or lower (@ f_{osc} = 4.5 MHz) and when the motor is rotating in the direction reverse to the settings of the TB6634FNG.

Sine-Wave Drive Waveform (CW/CCW = Low)

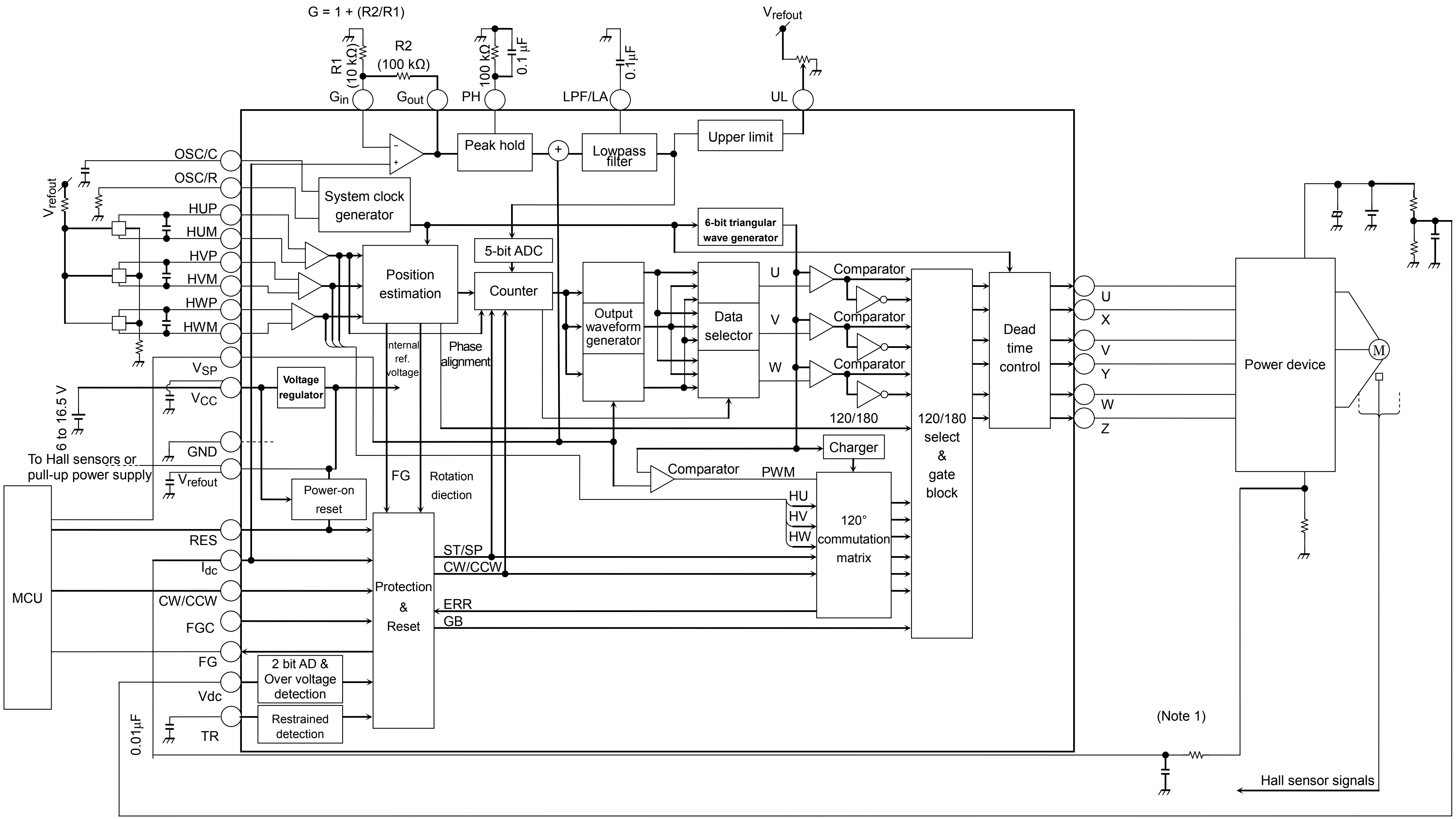


In sine-wave drive mode, the amplitude of the modulated signals varies with the V_{SP} voltage and the motor speed changes with the conduction duty cycle of the output waveforms.

Triangular wave frequency = carrier frequency = $f_{osc}/252$ (Hz)

Note: At startup, the motor is driven by a sine wave when the Hall signal frequency is 1 Hz or higher (@ f_{osc} = 4.5 MHz) and when the motor is rotating in the same direction as settings of the TB6634FNG.

Application Circuit Example

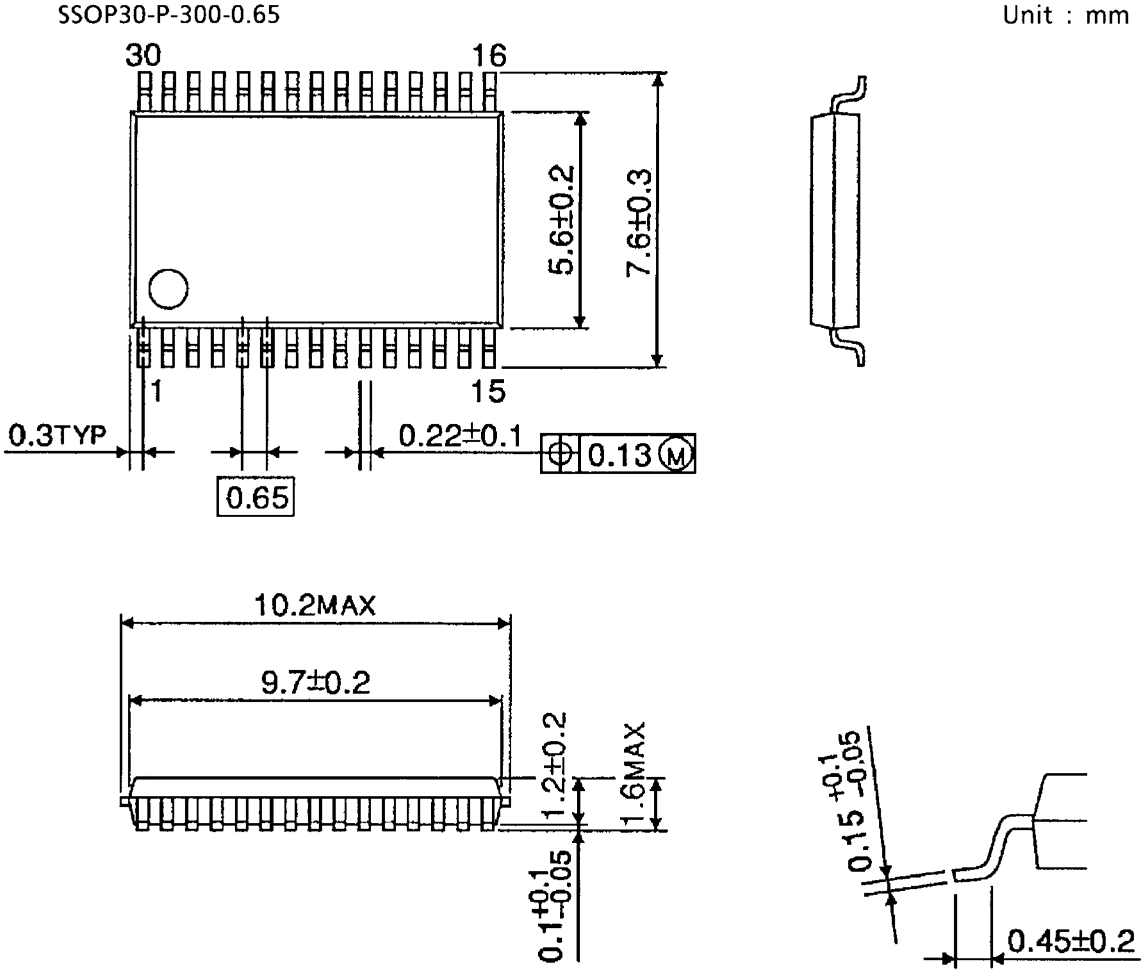


Note 1: Connect to ground as necessary to prevent IC malfunction due to noise.

Note 2: Connect GND to signal ground on the application circuit.

Note 3: Utmost care is required in the design of the output, V_{CC}, and GND lines since the IC may shatter or explode due to short-circuits between outputs, short to V_{CC} or short to ground. The IC may also shatter or explode when it is installed in a wrong orientation.

Package Dimensions



Weight: 0.17 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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