TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

SSM3K127TU

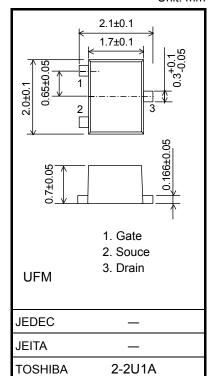
○ Power Management Switch Applications

- High-Speed Switching Applications
- 1.8V drive
- Low ON-resistance: R_{on} = 286 m Ω (max) (@V_{GS} = 1.8V)
 - : R_{on} = 167 m Ω (max) (@V_{GS} = 2.5V)

: R_{on} = 123 m Ω (max) (@V_{GS} = 4.0V)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
Drain-Source voltage		V _{DSS}	30	V	
Gate-Source voltage		V _{GSS}	±12	V	
Drain current	DC	I _D	2.0	A	
	Pulse	I _{DP}	4.0		
Drain power dissipation		P _D (Note 1)	800	mW	
		P _D (Note 2)	500		
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	–55 to 150	°C	



Weight: 6.6mg (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the

reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

- Note 1: Mounted on a ceramic board. (25.4 mm \times 25.4 mm \times 0.8 t, Cu Pad: 645 mm 2)
- Note 2: Mounted on an FR4 board. (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 645 mm 2)

Start of commercial production 2007-04

Unit: mm

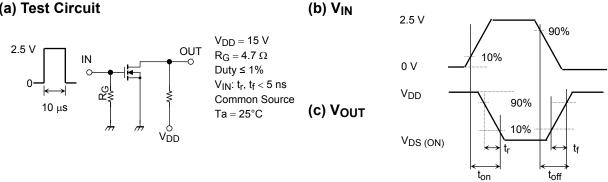
Electrical Characteristics (Ta = 25°C)

Chara	acteristic	Symbol	Test Conditions		Min	Тур.	Max	Unit
Drain-Source breakdown voltage	V (BR) DSS	$I_{D} = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	$_{\rm D} = 1 {\rm mA}, {\rm V}_{\rm GS} = 0 {\rm V}$ 30		_	_	V	
Drain-Source breakdown vollage		V (BR) DSX	$I_D = 1 \text{ mA}, V_{GS} = -12 \text{ V}$	18				
Drain cut-off curre	nt	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$		_		1	μA
Gate leakage curr	ent	I _{GSS}	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0 \text{ V}$		_		±1	μA
Gate threshold vo	Itage	V _{th}	$V_{DS} = 3 V, I_D = 1 mA$		0.4		1.0	V
Forward transfer a	admittance	Y _{fs}	$V_{DS} = 3 V, I_D = 1.0 A$	(Note3)	2.1	4.2		S
Drain–source ON-resistance	R _{DS (ON)}	$I_D = 1.0 \text{ A}, V_{GS} = 4.0 \text{ V}$	(Note3)	_	93	123	mΩ	
		$I_D = 0.8 \text{ A}, V_{GS} = 2.5 \text{ V}$	(Note3)	_	115	167		
		$I_D = 0.5 \text{ A}, V_{GS} = 1.8 \text{ V}$	(Note3)	_	155	286		
Input capacitance		C _{iss}			_	123		
Output capacitance		C _{oss}	$V_{DS} = 15V, V_{GS} = 0 V, f = 1 MHz$		_	43		pF
Reverse transfer of	capacitance	C _{rss}			_	18		
Total Gate Charge	9	Qg			_	1.5		
Gate-Source Charge		Q _{gs}	V _{DS} = 15V, I _D = 2.0 A, V _{GS} = 4 V		_	0.9		nC
Gate-Drain Charge		Q _{gd}			_	0.6		
Switching time	Turn-on time	t _{on}	V _{DD} = 15 V, I _D = 1.0 A,	_	9.2	_	ns	
	Turn-off time	t _{off}	V_{GS} = 0 to 2.5 V, R_{G} = 4.7 Ω		_	6.4		_
Drain-Source forward voltage		V _{DSF}	$I_D = -2.0 \text{ A}, V_{GS} = 0 \text{ V}$	(Note3)	_	-0.82	-1.2	V

Note 3: Pulse test

Switching Time Test Circuit

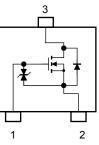




Marking

Equivalent Circuit (top view)





Usage Considerations

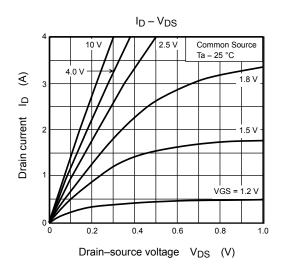
Let Vth be the voltage applied between gate and source that causes the drain current (ID) to below (1 mA for the SSM3K127TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th,}$ and $V_{GS(off)}$ must be lower than V_{th.} This relationship can be expressed as: V_{GS(off)} < V_{th} < V_{GS(on)}.

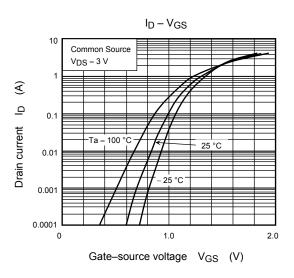
Take this into consideration when using the device.

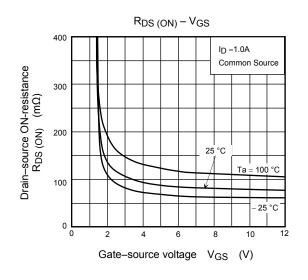
Handling Precaution

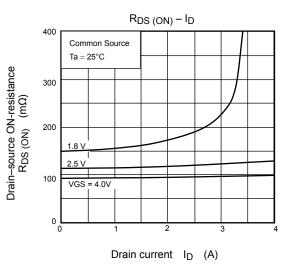
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

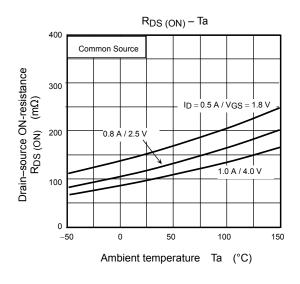
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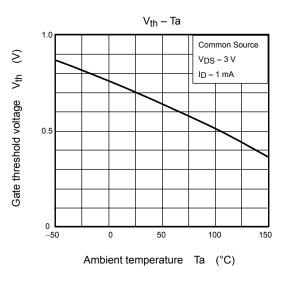




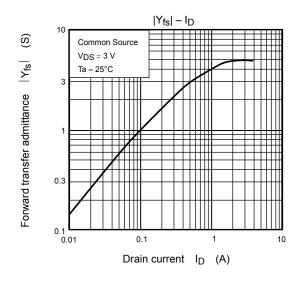


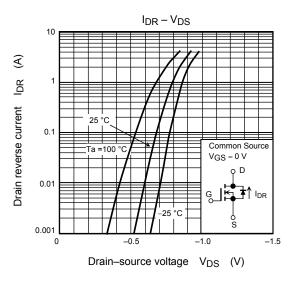


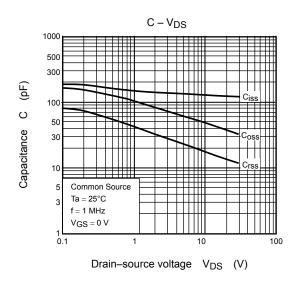


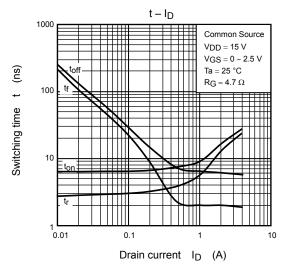


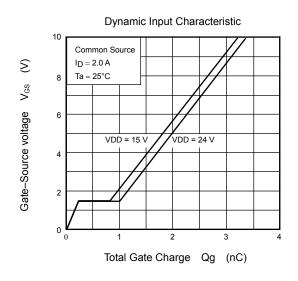
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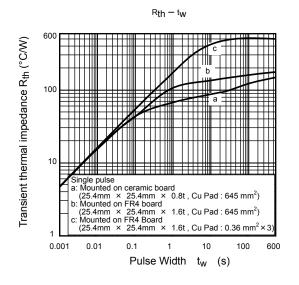


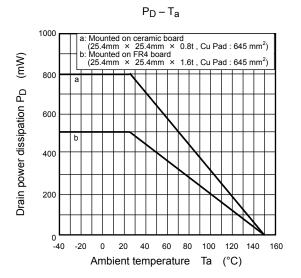




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