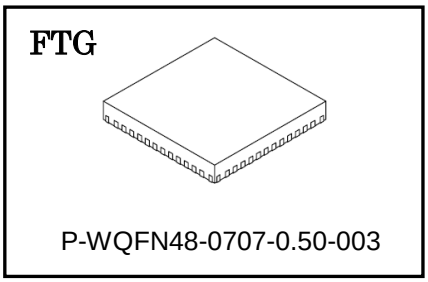
Toshiba BiCD process integrated circuit silicon monolithic

TB67S265FTG

8bit Serial controlled bipolar stepping motor driver

The TB67S265FTG is a two phase bipolar stepping motor driver using a PWM chopper, controlled by 8 bit serial.
Fabricated by the BiCD process, the TB67S265FTG is rated at 50V/2.0A(Maximum current).
The internal voltage regulator allows to control the device with a single VM power supply.



P-WQFN48-0707-0.50-003

Weight: 0.10 g (Typ.)

Features

・BiCD process integrated monolithic IC.

・Capable of controlling one bipolar stepping motor.

・PWM controlled constant-current drive.

・Built-in serial-parallel convert circuit (8bit shift register)

・3-line (Data, Clock, Latch) serial output function for cascade connection

・Allows full, half step operation

・4 bit (16 steps) adjustable torque function (TRQ1,TRQ2,TRQ3,TRQ4).

・Low on-resistance MOSFET output stage.(Ron(D-S))

・High voltage and current (for specification, please refer to the absolute maximum ratings and operation ranges).

・Built-in error detection circuits (Thermal shutdown (TSD), over current shutdown (ISD), and power on reset(POR)).

・Built-in VCC regulator for internal use.

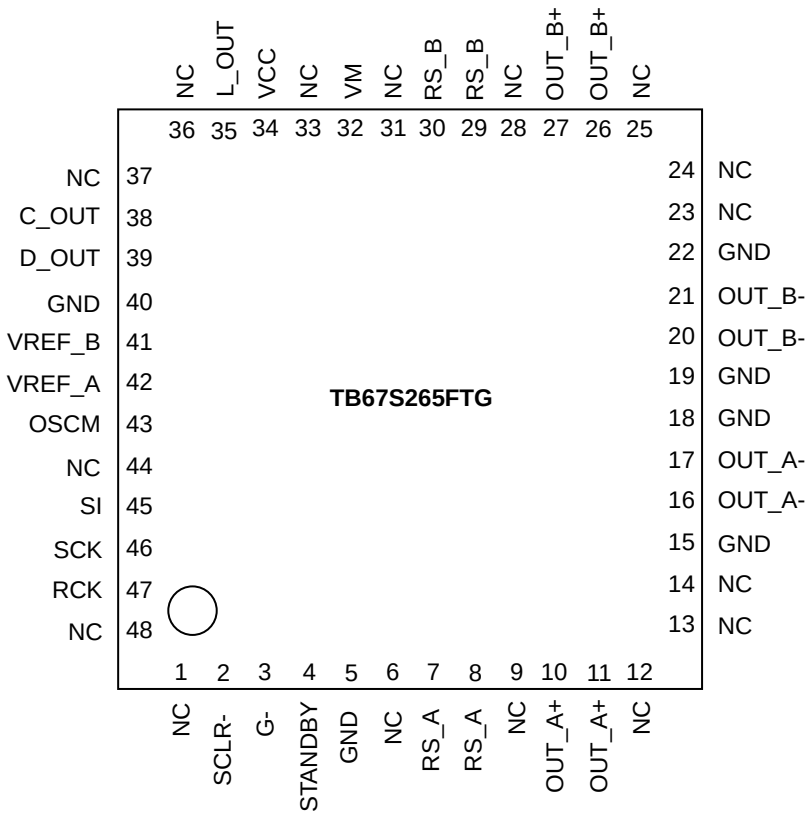
・Chopping frequency of a motor can be customized by external resistance and capacitor.

・Package type: P-WQFN48-0707-0.50-003

Note) Please be careful about thermal conditions during use.

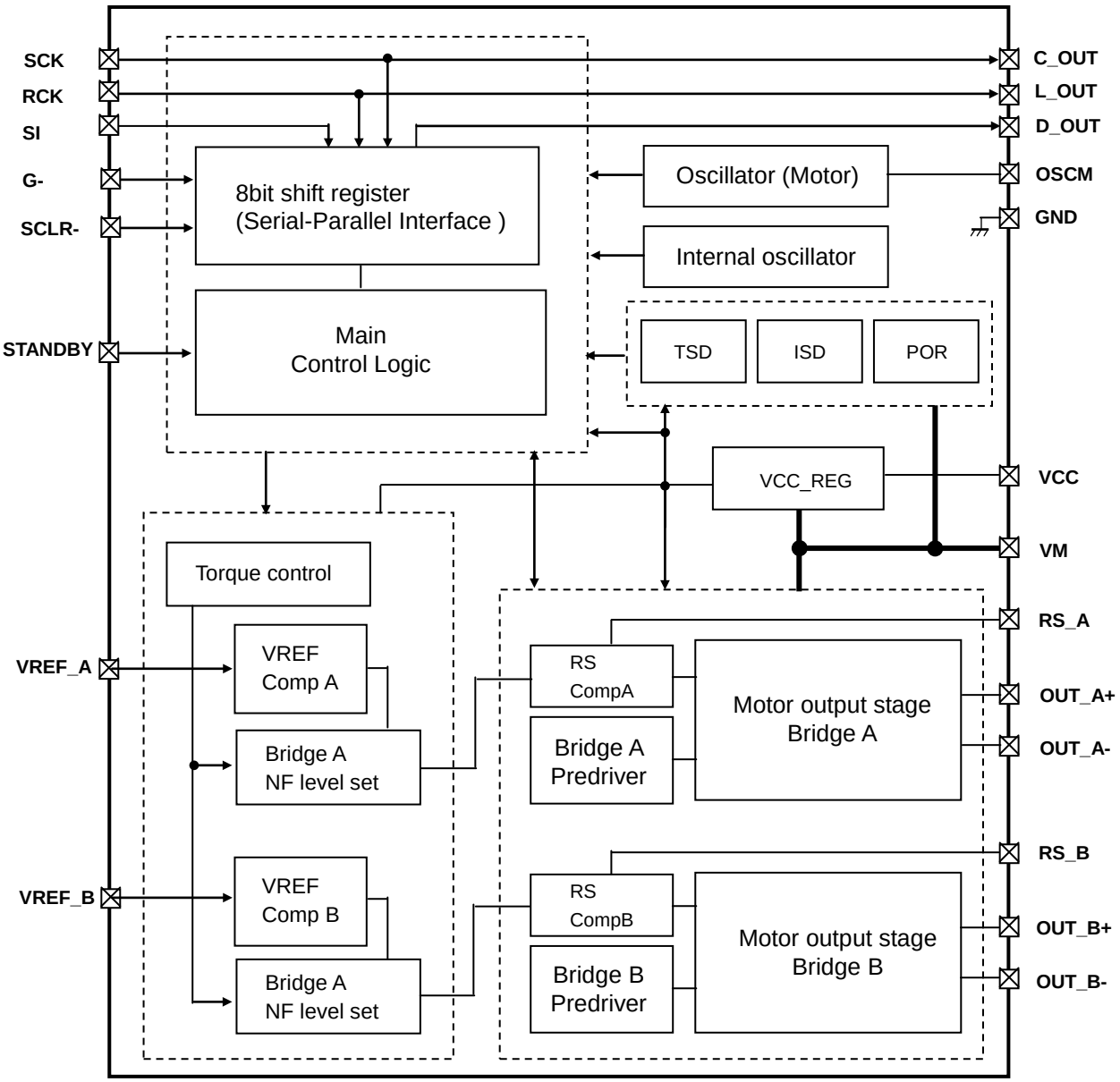
Pin assignment

(Top View)



Please mount the four corner pins of the QFN package and the exposed pad to the GND area of the PCB.

Block diagram



Functional blocks/circuits/constants in the block diagram may be omitted or simplified for explanatory purposes.

Application Notes

All the grounding wires of the TB67S265 must run on the solder mask on the PCB, and be externally connected at a single point. Also, the grounding method should be considered for efficient heat dissipation.

Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged. Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VM, RS, OUT, GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.
The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current.

Pin explanations
TB67S265FTG (QFN48)

Pin No.1 to 28

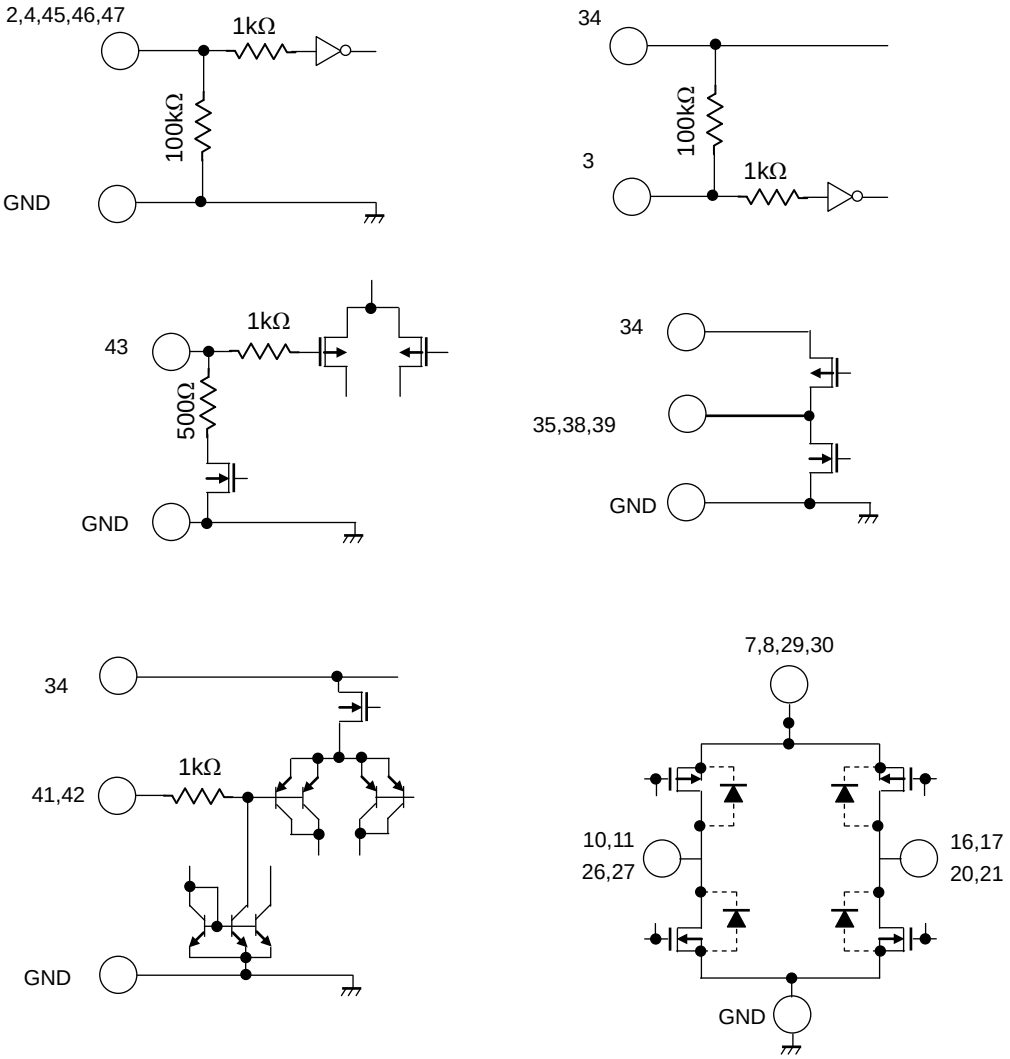
Pin No.	Pin Name	Function
1	NC	Non-connection pin
2	SCLR-	Serial register clear pin (low active)
3	G-	Serial data enable pin (low active)
4	STANDBY	Standby pin
5	GND	Ground pin
6	NC	Non-connection pin
7	RS_A(Note)	Motor Ach current sense pin
8	RS_A(Note)	Motor Ach current sense pin
9	NC	Non-connection pin
10	OUT_A+(Note)	Motor Ach (+) pin
11	OUT_A+(Note)	Motor Ach (+) pin
12	NC	Non-connection pin
13	NC	Non-connection pin
14	NC	Non-connection pin
15	GND	Ground pin
16	OUT_A-(Note)	Motor Ach (-) pin
17	OUT_A-(Note)	Motor Ach (-) pin
18	GND	Ground pin
19	GND	Ground pin
20	OUT_B-(Note)	Motor Bch (-) pin
21	OUT_B-(Note)	Motor Bch (-) pin
22	GND	Ground pin
23	NC	Non-connection pin
24	NC	Non-connection pin
25	NC	Non-connection pin
26	OUT_B+(Note)	Motor Bch (+) pin
27	OUT_B+(Note)	Motor Bch (+) pin
28	NC	Non-connection pin

Pin No.29 to 48

Pin No.	Pin Name	Function
29	RS_B(Note)	Motor Bch current sense pin
30	RS_B(Note)	Motor Bch current sense pin
31	NC	Non-connection pin
32	VM	Motor power supply pin
33	NC	Non-connection pin
34	VCC	Internal VCC regulator monitor pin
35	L_OUT	Serial 'Latch' output pin (logic output pin)
36	NC	Non-connection pin
37	NC	Non-connection pin
38	C_OUT	Serial 'Clock' output pin (logic output pin)
39	D_OUT	Shift register data output pin (logic output pin)
40	GND	Ground pin
41	VREF_B	Motor Bch output current set pin
42	VREF_A	Motor Ach output current set pin
43	OSCM	Oscillating circuit frequency for PWM chopping set pin
44	NC	Non-connection pin
45	SI	Serial 'Data' input pin
46	SCK	Serial 'Clock' input pin
47	RCK	Serial 'Latch' input pin
48	NC	Non-connection pin

Please do not run patterns under NC pins.
Note) Please connect the pins with the same pin name.

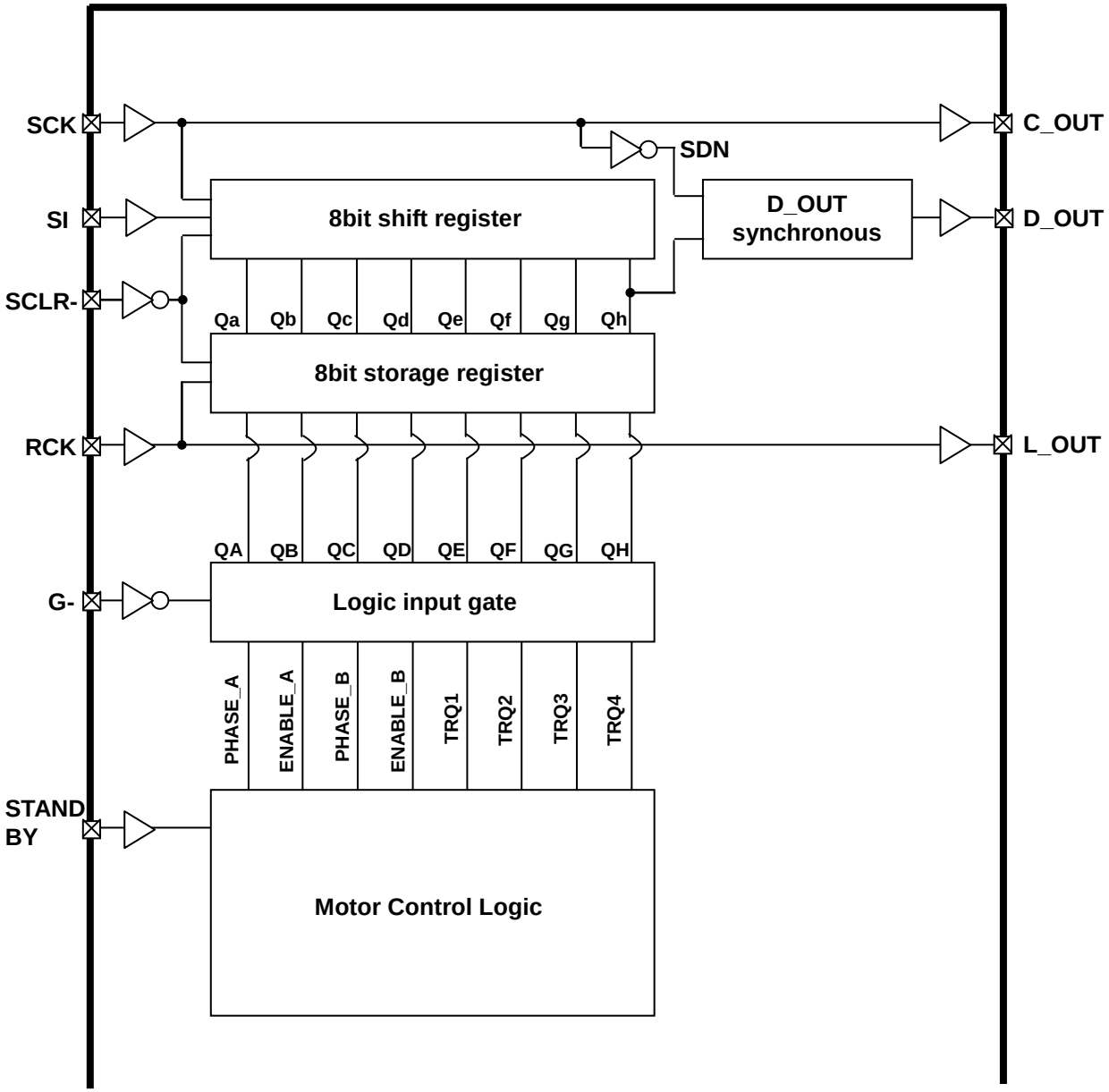
INPUT/OUTPUT equivalent circuit (TB67S265)



Pin No.	Pin Name	Pin No.	Pin Name
2	SCLR-	29	RS_B
3	G-	30	RS_B
4	STANDBY	32	VM
7	RS_A	34	VCC
8	RS_A	35	L_OUT
10	OUT_A+	38	C_OUT
11	OUT_A+	39	D_OUT
16	OUT_A-	41	VREF_B
17	OUT_A-	42	VREF_A
20	OUT_B-	43	OSCM
21	OUT_B-	45	SI
26	OUT_B+	46	SCK
27	OUT_B+	47	RCK

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

INPUT interface (8bit shift register + 8bit storage register)



Initial status of logic input signal

Input signal	Initial status
SCK	Low
SI	Low
SCLR-	Low
RCK	Low
G-	High
STANDBY	Low

If the logic signal is not asserted, the initial status of the logic pins will be as shown above.
SCLR-: Low=shift register and storage register is at the initial status.
G-: High=PHASE_A,ENABLE_A,PHASE_B,ENABLE_B,TRQ1,TRQ2,TRQ3,TRQ4=Disable
STANDBY=Low: Standby mode

Truth table

Input					Function
SI	SCK	SCLR-	RCK	G-	
X	X	X	X	H	PHASE_A,PHASE_B,ENABLE_A,ENABLE_B,TRQ1,TRQ2,TRQ3,TRQ4=Disable
X	X	X	X	L	PHASE_A,PHASE_B,ENABLE_A,ENABLE_B,TRQ1,TRQ2,TRQ3,TRQ4=Enable
X	X	L	X	X	Shift register and storage register is initialized
L	↑	H	X	X	The first data of the shift register is L, and the other register will be stored with the data before.
H	↑	H	X	X	The first data of the shift register is H, and the other register will be stored with the data before.
X	↓	H	X	X	The shift register data will maintain its status. The data after the shift register(Qh) will be output from D_OUT pin.
X	X	H	↑	X	Shift register data will be stored to the storage register.
X	X	H	↓	X	The storage register data will maintain its status.

X**:** Don't care

Note) To send the logic output data correctly to the next IC, please make sure to end the SCK data transfer with a Low signal.

Function explanation (Stepping motor mode)

The motor current is defined as plus when the current flows from OUT_X+ to OUT_X-, and defined minus when the current flows from OUT_X- to OUT_X+.

Signal	H	L	Notes
ENABLE_X	OUTPUT: ON	OUTPUT: OFF	When ENABLE_X is set to L, no matter what the PHASE status are, the corresponding output stage will be set OFF(Hi-z).
PHASE_X	OUT_X+**:** H OUT_X-**:** L	OUT_X+**:** L OUT_X-**:** H	When set to H, the current will flow from OUT_X+ to OUT_X- at charge status.
STANDBY	Motor operational	Standby mode	When STANDBY is set to L, the internal OSC circuit as well as output stage is set OFF; therefore the motor will not operate.

<Full step>

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT (A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+100%	H	H	+100%
L	H	-100%	H	H	+100%
L	H	-100%	L	H	-100%
H	H	+100%	L	H	-100%

<Half step>

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT (A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+100%	H	H	+100%
x	L	0%	H	H	+100%
L	H	-100%	H	H	+100%
L	H	-100%	x	L	0%
L	H	-100%	L	H	-100%
x	L	0%	L	H	-100%
H	H	+100%	L	H	-100%
H	H	+100%	x	L	0%

X : Don't care

Torque (TRQ) function: Current Ratio

TRQ1	TRQ2	TRQ3	TRQ4	Current Ratio
L	L	L	L	0%
L	L	L	H	5%
L	L	H	L	10%
L	L	H	H	15%
L	H	L	L	25%
L	H	L	H	29%
L	H	H	L	38%
L	H	H	H	43%
H	L	L	L	52%
H	L	L	H	60%
H	L	H	L	67%
H	L	H	H	74%
H	H	L	L	80%
H	H	L	H	86%
H	H	H	L	94%
H	H	H	H	100%

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	Remarks
Motor power supply		VM	50	V	-
Motor output voltage		VOUT	50	V	-
Motor output current (per channel)		IOUT	2.0	A	(Note 1)
Internal VCC voltage		VCC	6.0	V	When externally supplied
Logic input voltage		VIH	6.0	V	
Logic output current		IOH	-7.0	mA	
		IOL	7.0	mA	
VREF input voltage		VREF	5.0	V	
Power dissipation	WQFN48	PD	1.3	W	(Note 2)
Operating temperature		TOPR	-20 to 85	°C	
Storage temperature		TSTG	-55 to 150	°C	
Junction temperature		Tj (max)	150	°C	

Note 1: Usually the maximum current value should be controlled below 70%(IOUT≦1.4A) or less of the absolute maximum ratings for a standard based on thermal rating. The maximum output current may be further limited due to thermal considerations, depending on ambient temperature and board conditions.

Note 2: Device alone. (Ta =25°C)
If the ambient temperature is above 25°C, the power dissipation must be de-rated by 10.4mW/°C.

Ta: Ambient temperature

TOPR : Ambient temperature while the device is active

Tj: Junction temperature while the device is active. The maximum junction temperature is limited by the thermal shutdown(TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj(max), will not exceed 120°C.

Caution) Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. The device does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied.
All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

Operation ranges (Ta=0 to 85°C)

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Motor power supply	VM	10	24	47	V	
Motor output current	IOUT	-	1.4	2.0	A	(Note 1)
Logic input voltage	VIN(H)	3.0	-	5.5	V	Logic H level
	VIN(L)	0	-	2.0	V	Logic L level
Chopping frequency set range	fchop(range)	40	100	150	kHz	
VREF input voltage	VREF	GND	3.0	3.6	V	

Note 1: Maximum current for actual usage may be limited by the operating circumstances such as operating conditions (exciting mode, operating time, etc), ambient temperature, and heat conditions (board condition and so on).

Electrical Specifications 1(DC) (Ta = 25°C, VM = 24 V, unless specified otherwise)

Characteristics		Symbol	Test conditions	Min	Typ.	Max	Unit
Logic input voltage	HIGH	VIN(H)	Logic input (Note 1)	3.0	-	5.5	V
	LOW	VIN(L)	Logic input (Note 1)	0	-	2.0	V
Logic input hysteresis		VIN(HYS)	Logic input (Note 1)	300	-	500	mV
Logic input current	HIGH	IIN(H)	VIN(H)=3.3V	-	33	50	μA
	LOW	IIN(L)	VIN(L)=0V	-	-	1	μA
Logic output pin voltage	HIGH	VOH	IOH=-3mA, VCC based	-0.41	-0.34	-0.27	V
	LOW	VOL	IOL=3mA, GND based	0.20	0.25	0.30	V
Power consumption		IM1	Output pins=open Standby mode	-	2	3.5	mA
		IM2	Output pins=open Standby release ENABLE=Low	-	3.5	5.5	mA
		IM3	Output pins=open Full step resolution	-	5.5	7	mA
Output leakage current	HIGH	IOH	VRS=VM=50V,VOUT=0V	-	-	1	μA
	LOW	IOL	VRS=VM=VOUT=50V	1	-	-	μA
Motor current channel differential		ΔIOUT1	Current differential between channels	-5	0	5	%
Motor current setting accuracy		ΔIOUT2	IOUT=1.0A (Note 2)	-5	0	5	%
RS pin current		IRS	VRS=VM=24V	0	-	10	μA
Output MOSFET On resistance (High+Low side)		Ron(S)_PN	Tj=25°C, IOUT=2.4A, Forward direction (High-side+Low-side)	-	0.8	0.9	Ω

Note1: VIN (H) is defined as the VIN voltage that causes the outputs (OUTA,OUTB) to change when a pin under test is gradually raised from 0 V. V IN (L) is defined as the V IN voltage that causes the outputs (OUTA, OUTB) to change when the pin is then gradually lowered from 5V. The difference between V IN (H) and V IN (L) is defined as the V IN (HYS).

Note2:When using the internal VCC regulator and for VREF input voltage with a resistance divider; taking VCC accuracy and VREF ratio in to consideration, the motor current setting accuracy specification will be±8%.

Note: When the logic signal is applied to the device whilst the VM power supply is not asserted; the device is designed not to function, but for safe usage, please apply the logic signal after the VM power supply is asserted and the VM voltage reaches the proper operating range.

Electrical Specifications 2(DC) (Ta=25°C, VM=24 V, unless specified otherwise)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
VREF input voltage	VREF	VM=24V,VCC=5V	GND	3.0	3.6	V
VREF input current	IREF	VREF=3.0V	-	0	1	μA
VCC pin voltage	VCC	ICC=5.0mA	4.75	5.0	5.25	V
VCC pin current	ICC	VCC=5.0V	-	2.5	5	mA
VREF ratio	VREF(gain)	VREF=2.0V	1/5.2	1/5.0	1/4.8	-
Thermal shutdown threshold(Note 1)	T_jTSD	-	140	150	170	°C
VM POR threshold	VMR	-	7.0	8.0	9.0	V
Over-current detection threshold (Note 2)	ISD	-	2.1	3.0	4.0	A

(Note 1) About Thermal shutdown (TSD)
When the junction temperature of the device reaches the TSD threshold, the TSD circuit is triggered; the internal reset circuit then turns off the output transistors. Noise rejection blanking time is built-in to avoid misdetection. Once the TSD circuit is triggered; the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. The TSD circuit is a backup function to detect a thermal error, therefore is not recommended to be used aggressively.

(Note 2) About Over-current detection (ISD)
When the output current reaches the threshold, the ISD circuit is triggered; the internal reset circuit then turns off the output transistors. In order to avoid malfunction due to the switching, IC have a dead time. Once the ISD circuit is triggered, the detect latch signal can be cleared by reasserting the VM power source, or setting the device to standby mode. For fail-safe, please insert a fuse to avoid secondary trouble.

Back-EMF

While the motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that the device or other components will be damaged or fail due to the motor back-EMF.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

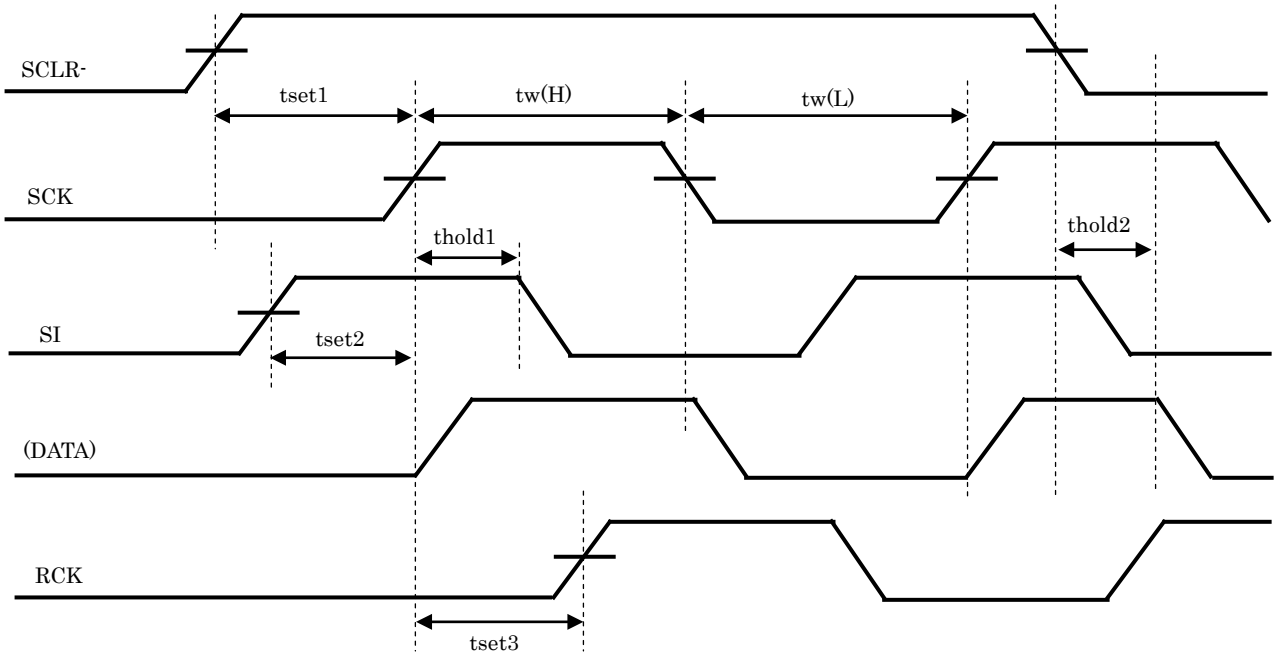
IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

AC Electrical Specification (Ta = 25°C, VM = 24 V, 6.8 mH/5.7 Ω)

Characteristics	Symbol	Test conditions	Min	Typ.	Max	Unit
Minimum pulse width (SCK,RCK,SI input signal)	tw(H)	fOSCM=1600kHz	250	-	-	ns
	tw(L)	fOSCM=1600kHz	250	-	-	ns
Minimum setup time	tset1	SCLR- → SCK	50	-	-	ns
	tset2	SI → SCK	50	-	-	ns
	tset3	SCK → RCK	50	-	-	ns
Minimum clock signal cycle (SCK,RCK)	tcyc	fOSCM=1600kHz	500	-	-	ns
Minimum hold time	thold1	SCK → SI	50	-	-	ns
	thold2	SCLR- → Data	50	-	-	ns
Output transistor switching specific	tr	Motor output	70	120	170	ns
	tf	Motor output	100	150	200	ns
Analog noise blanking time	AtBLK	VM=24V,IOUT=1.0A Analog tBLK	250	400	550	ns
Oscillator reference frequency	fOSCM	COSC=270pF,ROSC=3.6kΩ	1360	1600	1840	kHz
Chopping frequency	fchop	Output ACTIVE (IOUT=1.0 A), fOSCM= 1600 kHz	-	100	-	kHz

AC timing chart

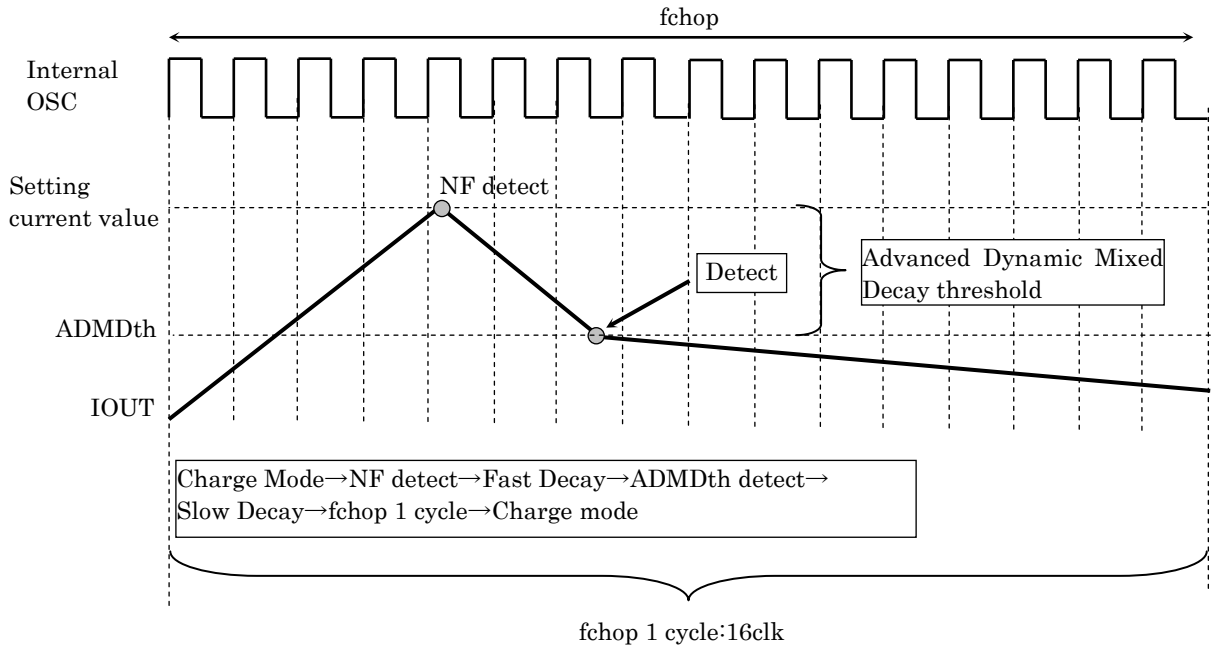


Timing charts may be simplified for explanatory purpose.

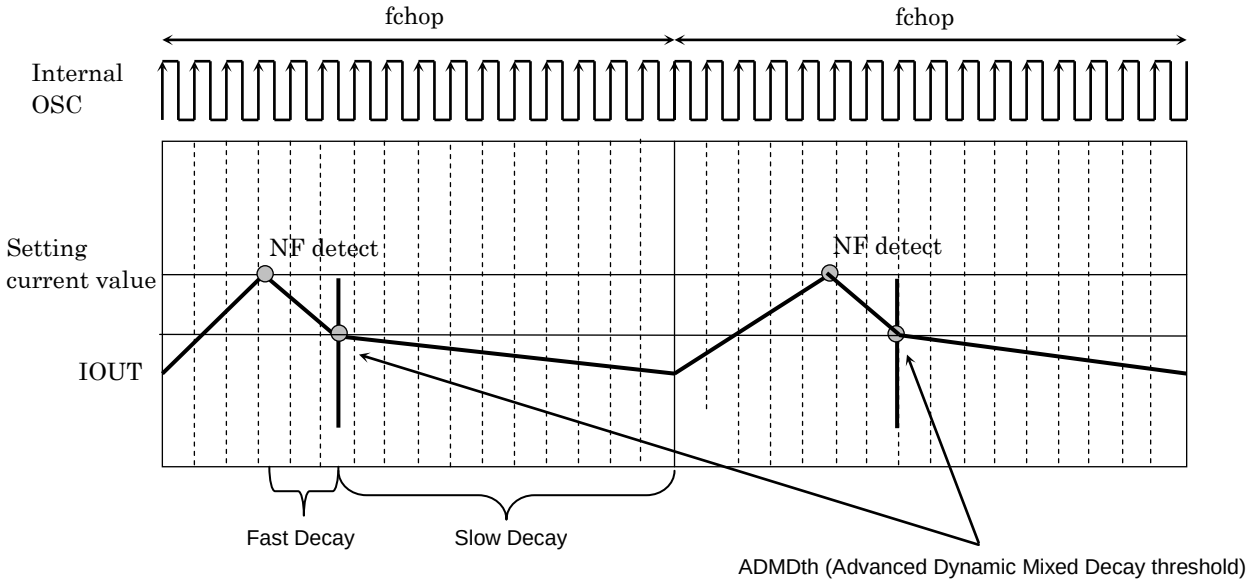
Decay function

ADMD(Advanced Dynamic Mixed Decay) constant current control

The Advanced Dynamic Mixed Decay threshold, which determines the current ripple level during current feedback control, is a unique value.



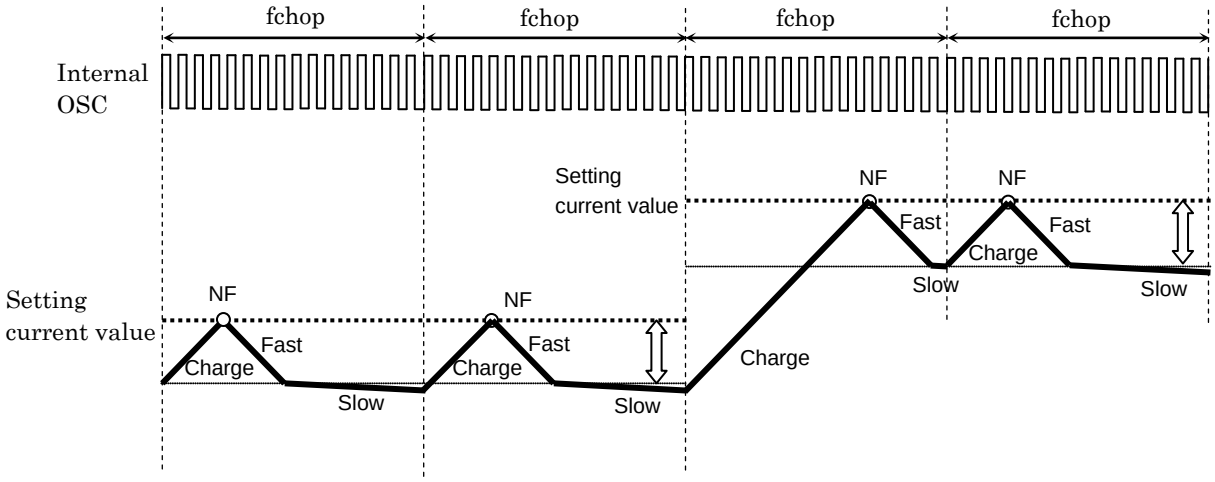
Auto Decay Mode current waveform



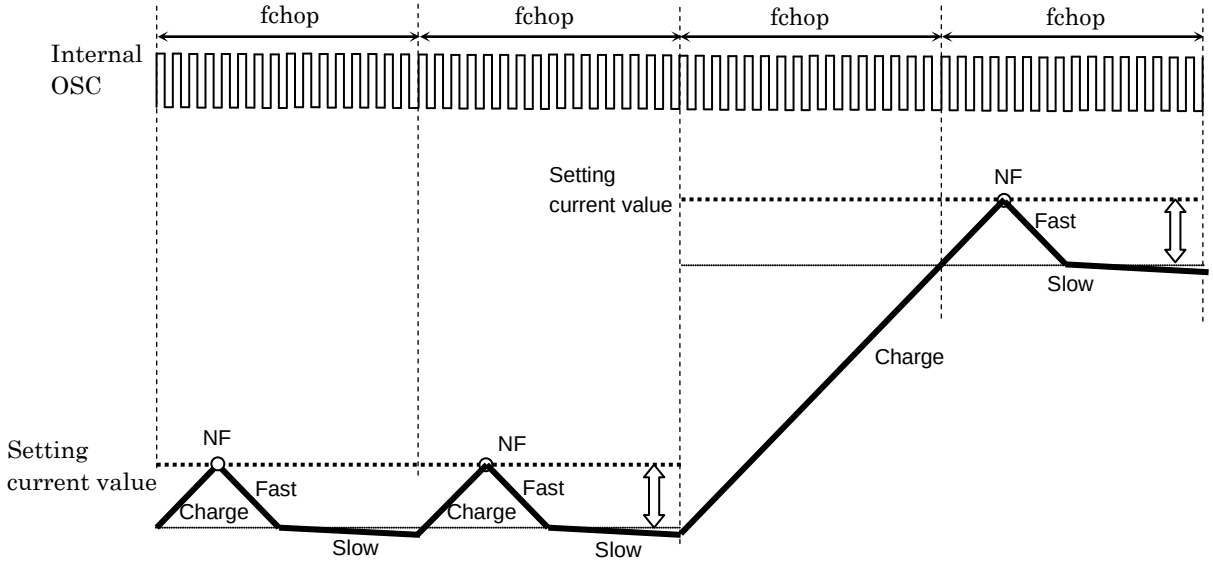
Timing charts may be simplified for explanatory purpose.

ADMD current waveform

・When the next current step is higher :

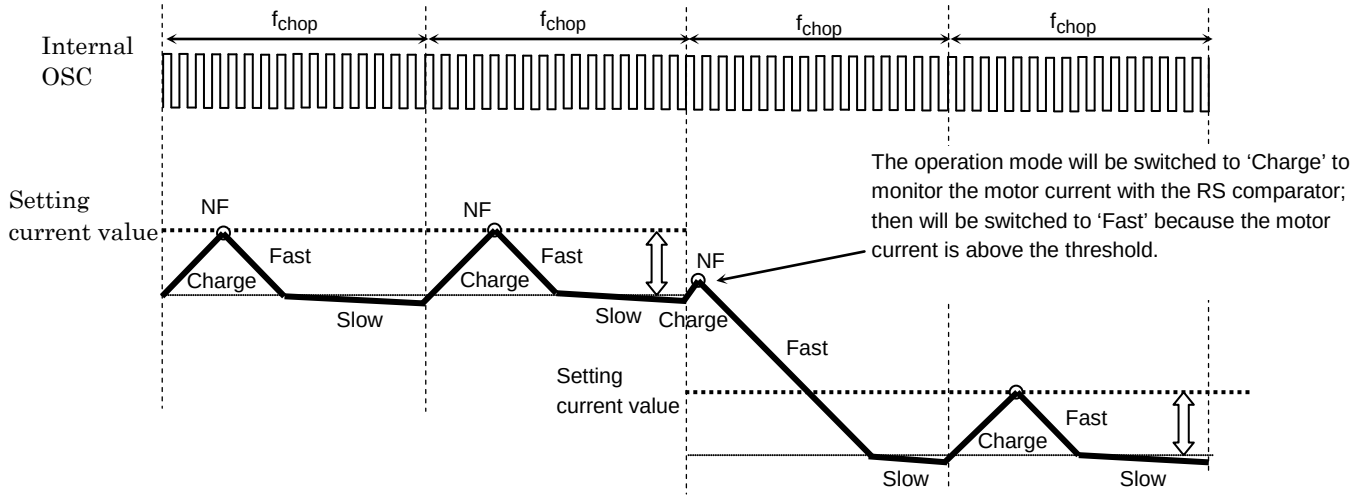


・When Charge period is more than 1 fchop cycle :

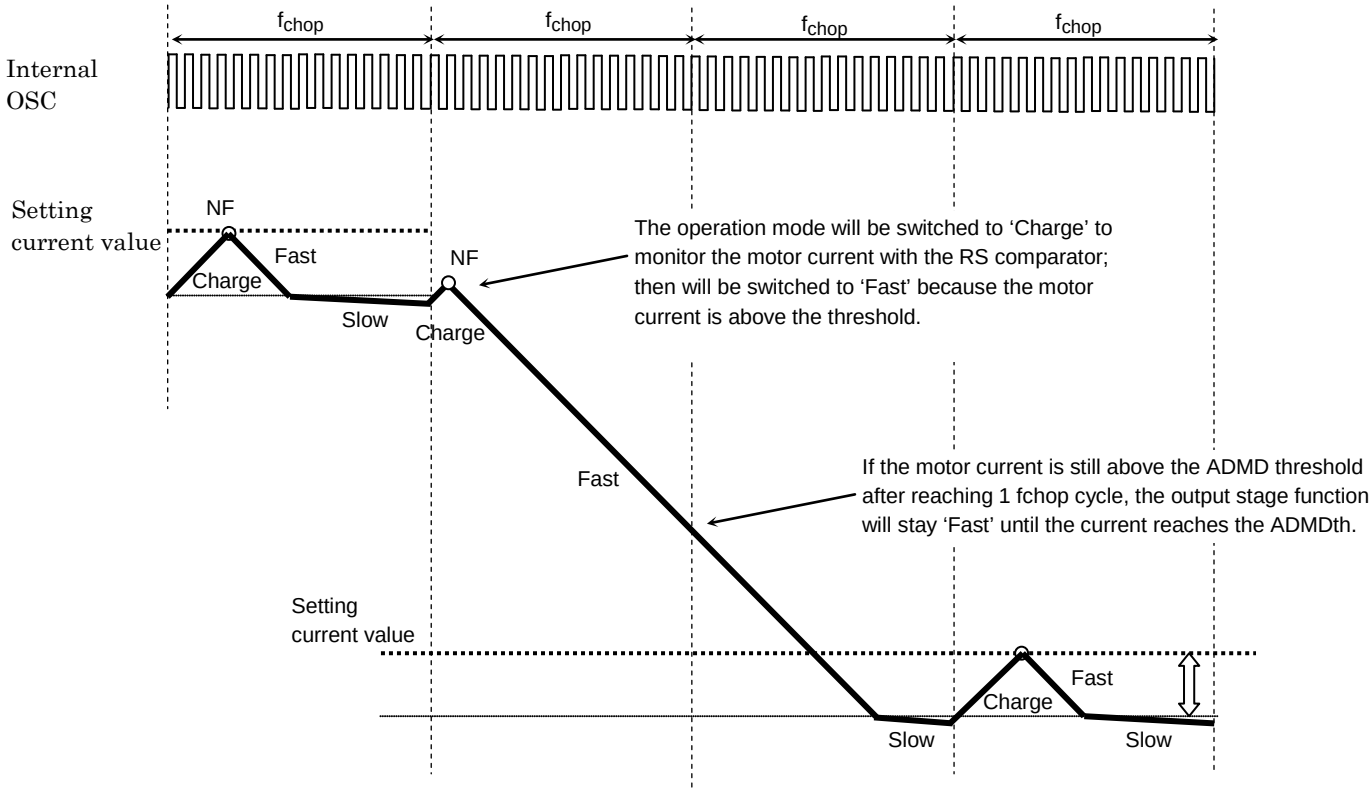


When the Charge period is longer than fchop cycle, the Charge period will be extended until the motor current reaches the NF threshold. Once the current reaches the next current step, then the sequence will go on to ADMD control.

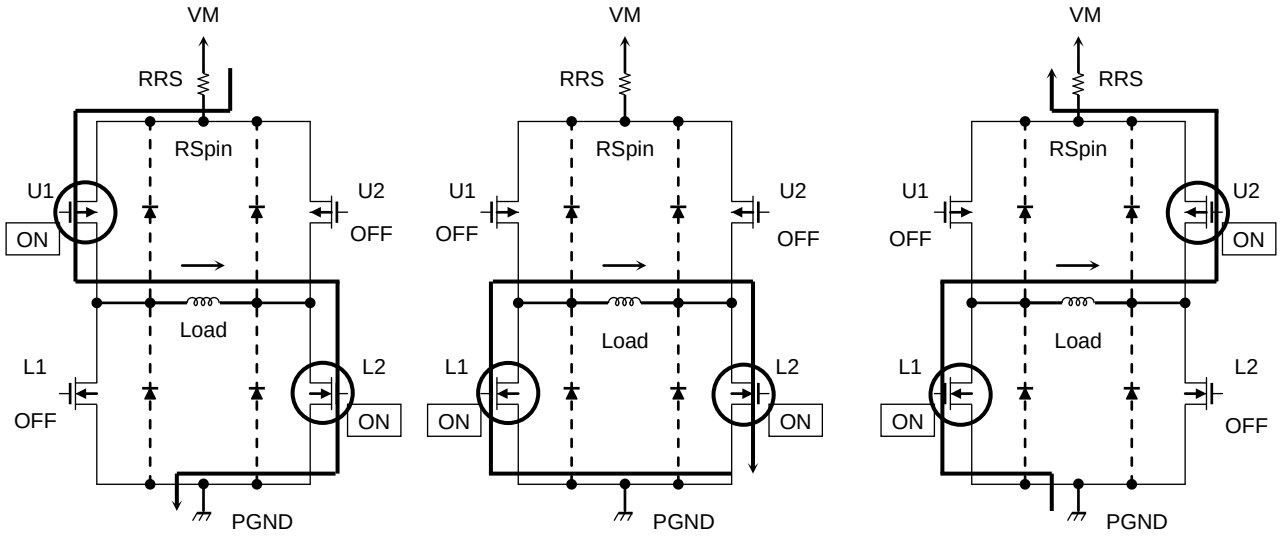
・When the next current step is lower :



・When the Fast continues past 1 fchop cycle (the motor current not reaching the ADMD threshold during 1 fchop cycle)



Output transistor function mode



Charge mode
A current flows into the motor coil.

Slow mode
A current circulates around the motor coil and this device.

Fast mode
The energy of the motor coil is fed back to the power

Output transistor function

MODE	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: This table shows an example of when the current flows as indicated by the arrows in the figures shown above.
If the current flows in the opposite direction, refer to the following table.

MODE	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

This IC controls the motor current to be constant by 3 modes listed above.

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Calculation of the Predefined Output Current

For PWM constant-current control, this IC uses a clock generated by the OSCM oscillator.
The peak output current (Peak current) can be set via the current-sensing resistor (RS) and the reference voltage (Vref), as follows:

$$IOUT(max) = Vref(gain) \times \frac{Vref(V)}{R_{RS}(\Omega)}$$

Vref(gain) : the Vref decay rate is 1/ 5.0 (typ.)

For example : In the case of a 100% setup
when Vref = 3.0 V, Torque=100%,RS=0.51Ω, the motor constant current (Peak current) will be calculated as:

IOUT = 3.0V / 5.0 / 0.51Ω= 1.18 A

Calculation of the OSCM oscillation frequency (chopper reference frequency)

An approximation of the OSCM oscillation frequency (fOSCM) and chopper frequency (fchop) can be calculated by the following expressions.

fOSCM=1/[0.56x{Cx(R1+500)}]
……C,R1: External components for OSCM (C=270pF , R1=5.1kΩ => fOSCM= 1.12MHz(Typ.))

fchop = fOSCM / 16
……fOSCM=1.12MHz => fchop =About 70kHz

If chopping frequency is raised, Rippl of current will become small and wave-like reproducibility will improve. However, the gate loss inside IC goes up and generation of heat becomes large.

By lowering chopping frequency, reduction in generation of heat is expectable. However, Rippl of current may become large. It is a standard about about 70 kHz. A setup in the range of 50 to 100 kHz is recommended.

Power consumption of the IC

Power of the IC is consumed by the transistor of the output block and that of the logic block mainly.

Power consumption of the motor output block
Power of the output block (P(out)) is consumed by MOSFET of upper and lower H-Bridge.

P(out) =Number of H-Bridge × IOUT (A) × VDS (V) = 2 (ch) × IOUT (A) × IOUT (A) × Ron (Ω)…….(1)

When the current waveform of the motor output corresponds to the ideal waveform, average power of output block can be provided as follows;

When Ron = 0.6Ω, IOUT (peak: Max) = 1.0 A, VM = 24 V
P(out) = 2 (ch) × 1.0 (A) × 1.0 (A) × 0.6 (Ω)…….....(2)
= 1.2(W)

Power consumption of logic and IM systems.
Power consumptions of logic and IM systems are calculated by separating the states (operating and stopping).

I (IM3) = 5.5 mA (typ.) : Operating
I (IM2) = 3.5 mA (typ.) : Stopping

Output system is connected to VM (24V). (Output system: Current consumed by the circuit connected to VM + Current consumed by switching output steps)

Power consumption is calculated as follows;

P (IM) = 24 (V) × 0.0055 (A)…….(3)
= 0.132 (W)

Power consumption
Total power consumption P(total) is calculated from the values of formula (2) and (3).

P(total) = P(out) + P (IM) = 1.2+ 0.132 = 1.332(W)

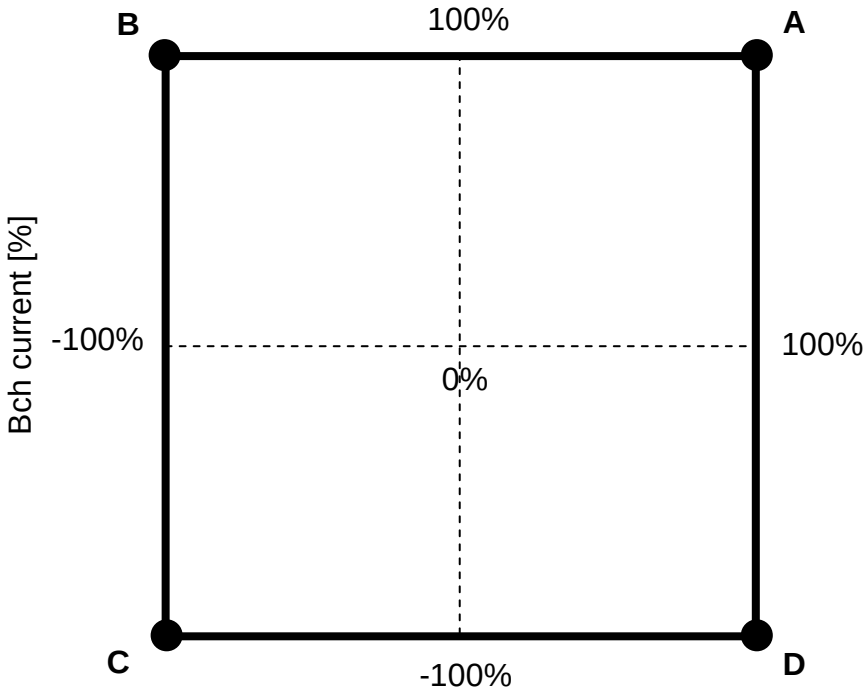
Standby mode is released. The power consumption in non-operation mode of the motor (waiting mode) is calculated as follows;

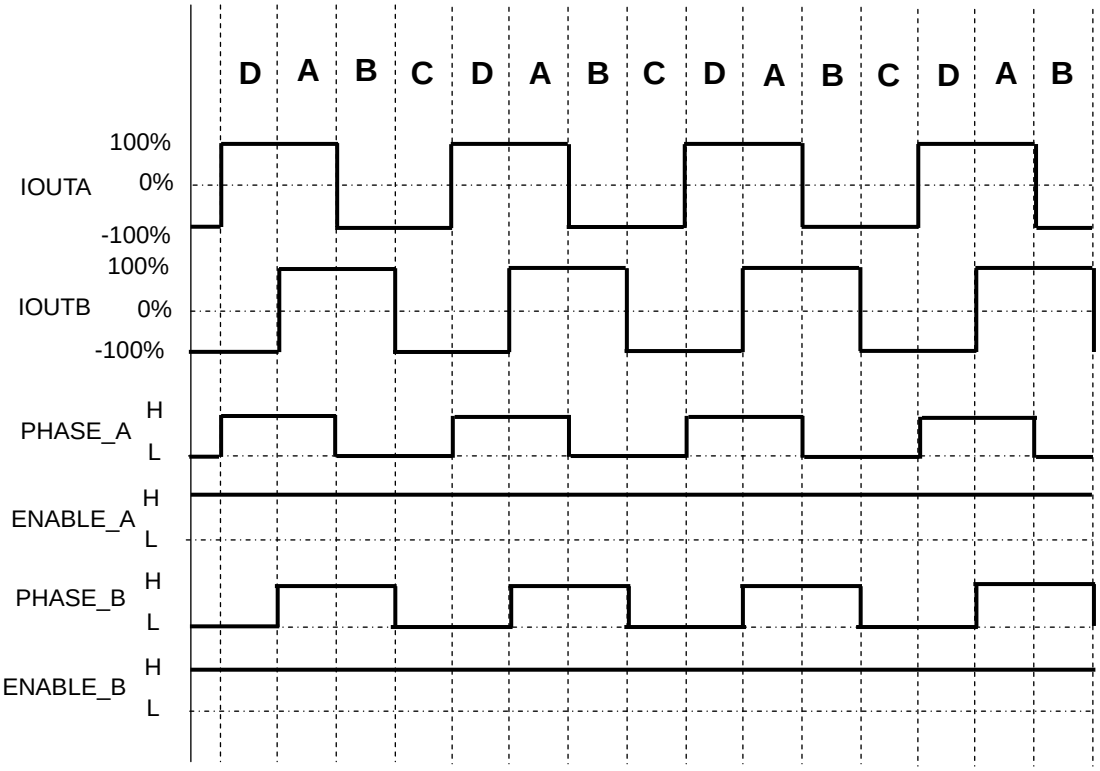
P(standby) = 24 (V) × 0.0035 (A) = 0.084 (W)

Refer to the above equations, evaluate the heat design of the board by the actual board enough, and configure the appropriate margin.

Step resolution sequence

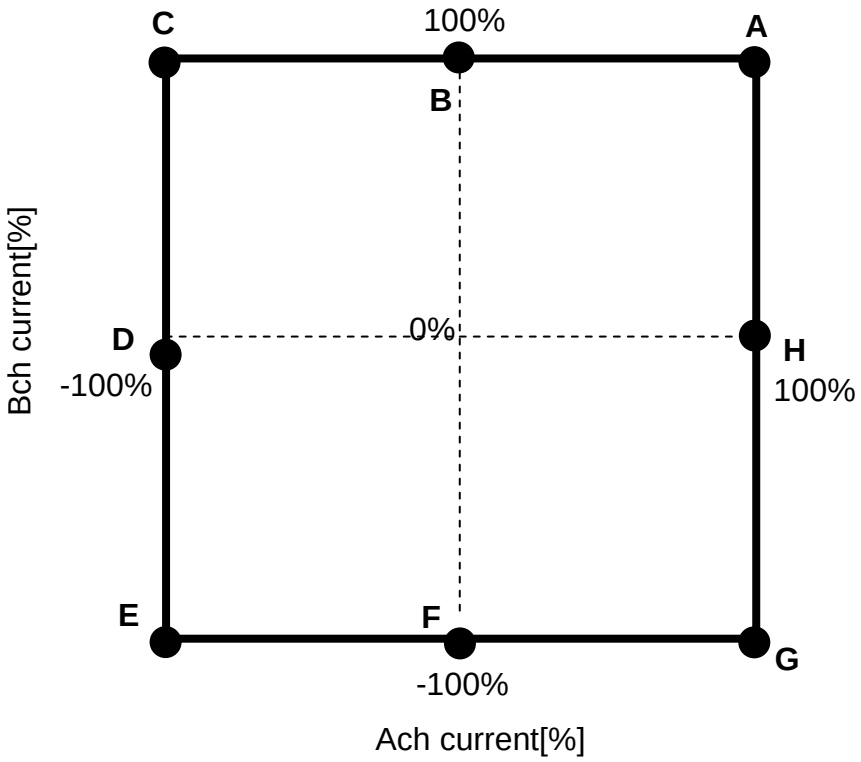
Full step resolution sequence

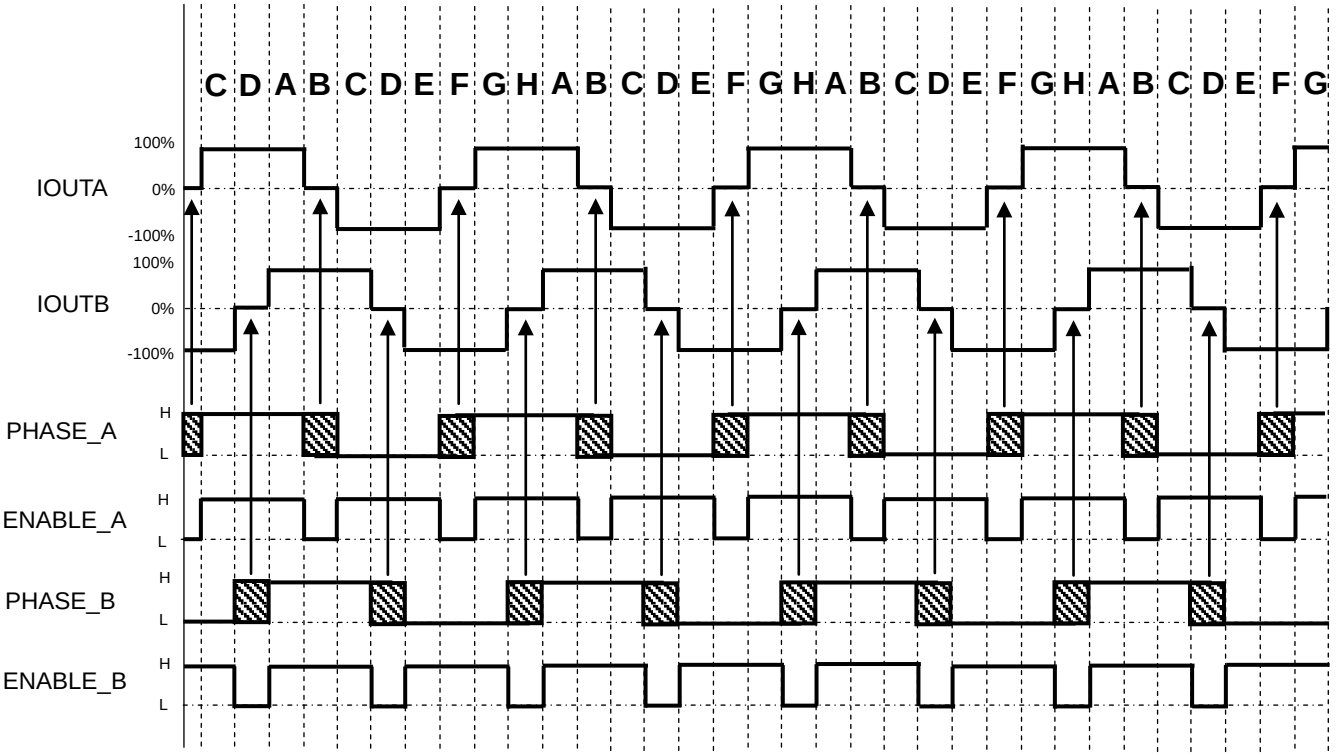




Timing charts may be simplified for explanatory purpose.

Half step(a) resolution sequence

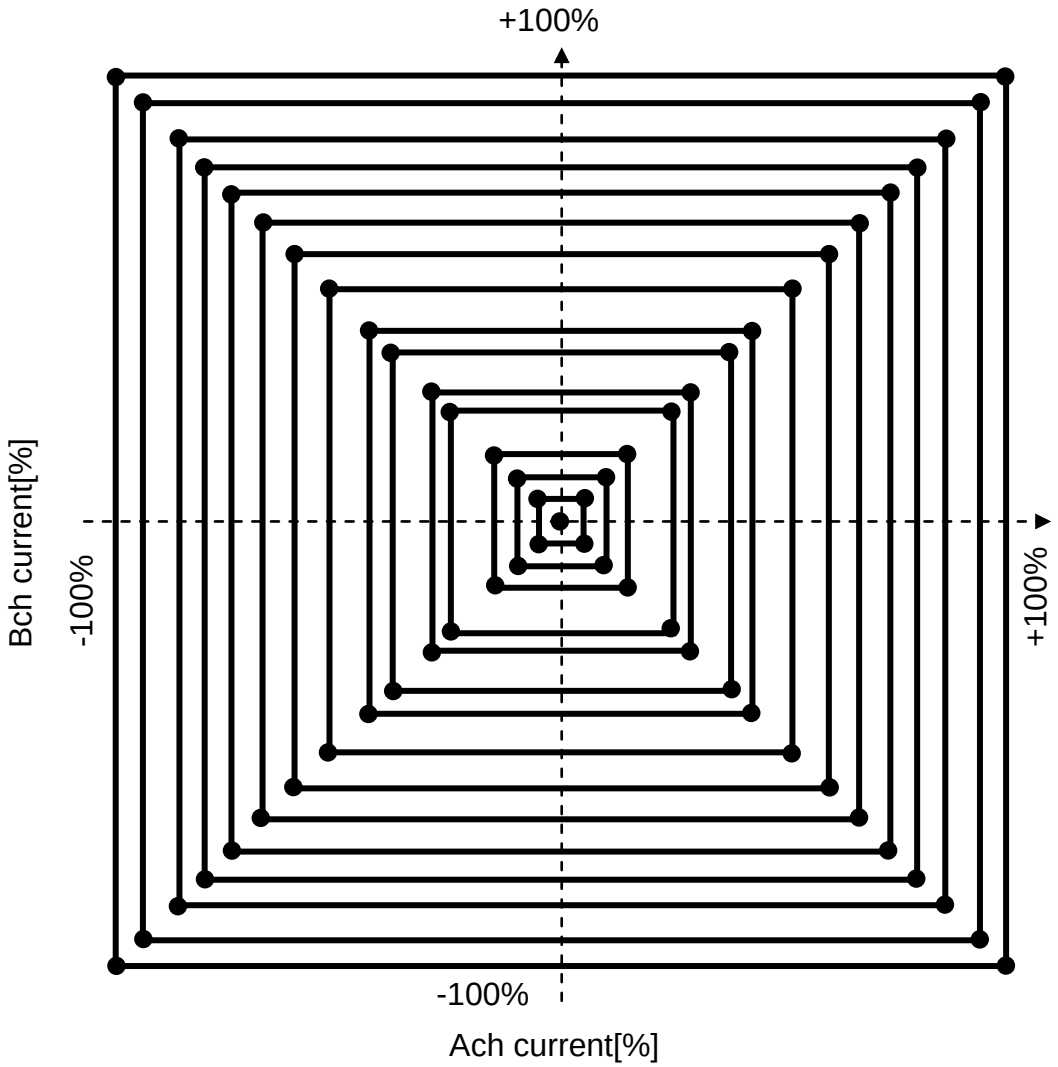




Timing charts may be simplified for explanatory purpose.

Step resolution sequence

Full step resolution sequence (TRQ1/TRQ2,TRQ3,TRQ4 settings)



Example) <Full step resolution> (TRQ1,TRQ2,TRQ3,TRQ4=H,H,H,H=100%)

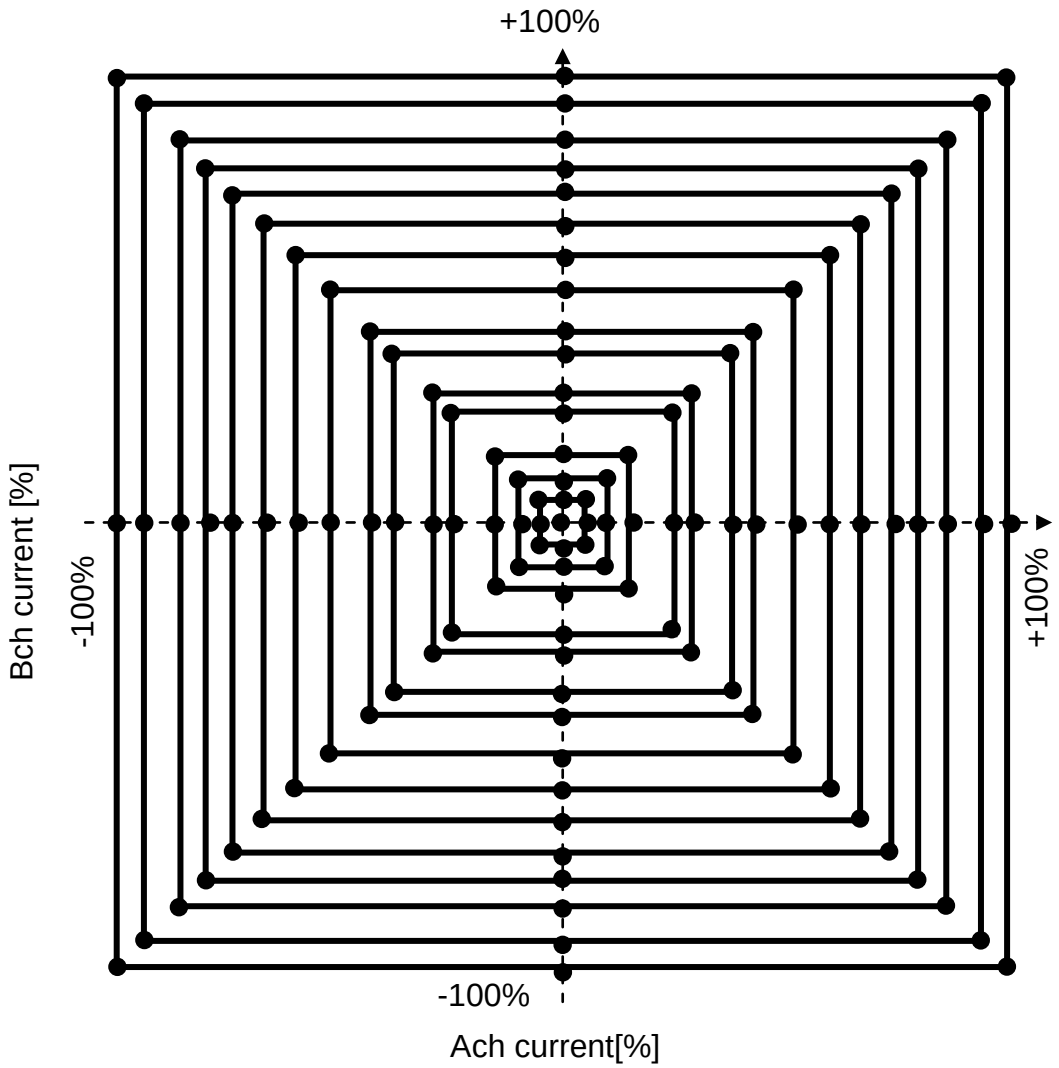
Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT(A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+100%	H	H	+100%
L	H	-100%	H	H	+100%
L	H	-100%	L	H	-100%
H	H	+100%	L	H	-100%

Example) <Full step resolution> (TRQ1,TRQ2,TRQ3,TRQ4=H,L,L,H=60%)

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT(A)	PHASE_B	ENABLE_B	IOUT(B)
H	H	+60%	H	H	+60%
L	H	-60%	H	H	+60%
L	H	-60%	L	H	-60%
H	H	+60%	L	H	-60%

Step resolution sequence

Half step resolution sequence (TRQ1,TRQ2,TRQ3,TRQ4 settings)



Example) <Half step(a) resolution> (TRQ1,TRQ2,TRQ3,TRQ4=H,H,H,H=100%)

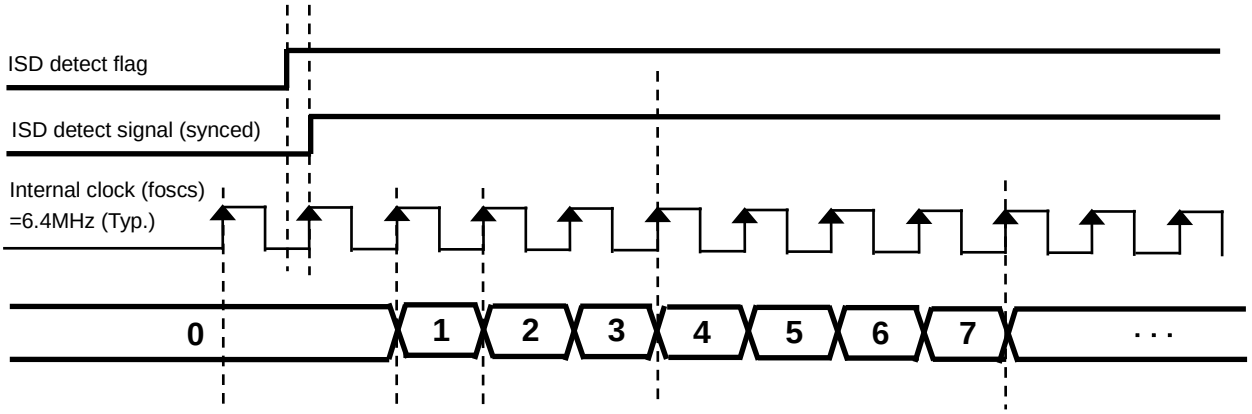
Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT (A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+100%	H	H	+100%
x	L	0%	H	H	+100%
L	H	-100%	H	H	+100%
L	H	-100%	x	L	0%
L	H	-100%	L	H	-100%
x	L	0%	L	H	-100%
H	H	+100%	L	H	-100%
H	H	+100%	x	L	0%

Example) <Half step(a) resolution> (TRQ1,TRQ2,TRQ3,TRQ4=L,H,L,L=25%)

Ach			Bch		
INPUT		OUTPUT	INPUT		OUTPUT
PHASE_A	ENABLE_A	IOUT (A)	PHASE_B	ENABLE_B	IOUT (B)
H	H	+25%	H	H	+25%
x	L	0%	H	H	+25%
L	H	-25%	H	H	+25%
L	H	-25%	x	L	0%
L	H	-25%	L	H	-25%
x	L	0%	L	H	-25%
H	H	+25%	L	H	-25%
H	H	+25%	x	L	0%

Blanking time for over current detection (ISD)

About ISD blanking time



Timing charts may be simplified for explanatory purpose.

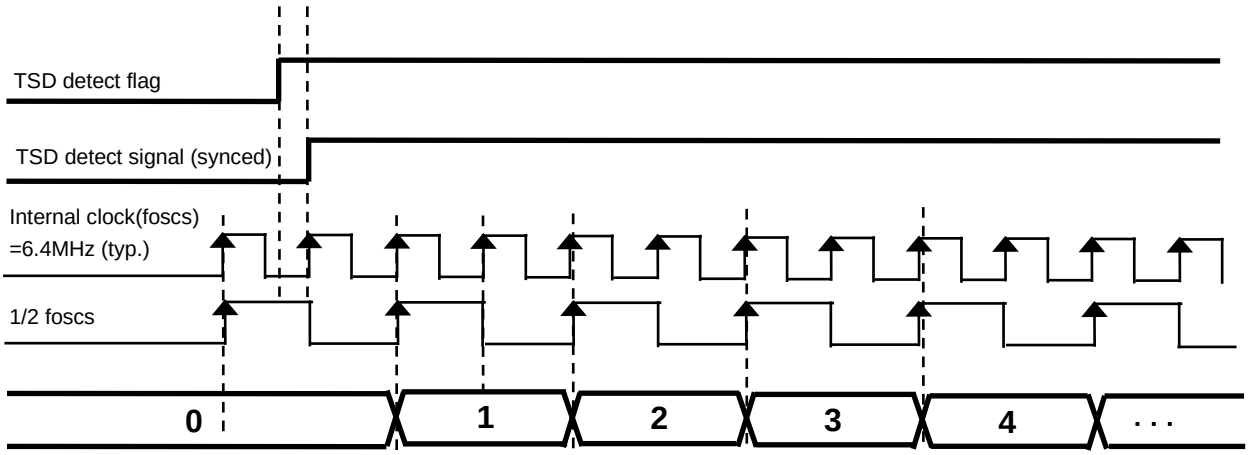
To avoid miss detecting, the over current detection circuit has a blanking time to reject any spike current which may or may not appear when switching operation. This blanking time is counted by the internal OSC(6.4MHz (Typ.)).

*foscs=6.4MHz(Typ.) internal clock
1/foscs × 7 to 8clk worth(1.09μs to 1.25μs)

Please note that this blanking time is an example when the current flows ideally, therefore the ISD circuit may not function correctly in some cases. Therefore please insert protective fuse for safe use. Fuse constants may change due to usage conditions; so please select which operates correctly.

Blanking time for thermal shutdown detection (TSD)

About TSD blanking time

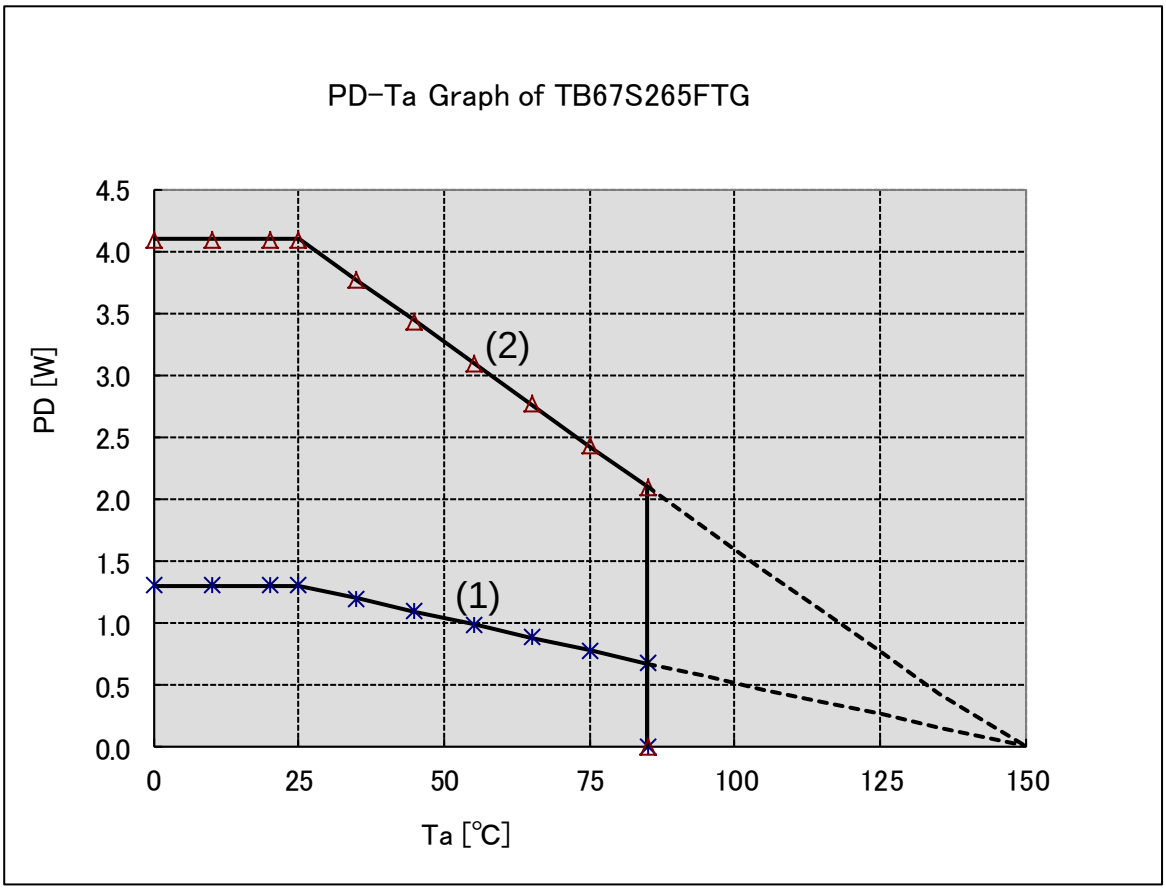


Timing charts may be simplified for explanatory purpose.

To avoid miss detecting, the thermal shutdown detection circuit has a blanking time to reject any spike current which may or may not appear when switching operation. This blanking time is counted by the internal OSC(6.4MHz (Typ.).

*foscs=6.4MHz(Typ.) internal clock
1/(foscs/2) × 7 to 8clk=1/foscs × 14 to 16clk worth(2.5μs to 2.8μs)

(For reference) PD-Ta graph



(1) … Rth(j-a) Device alone (96°C/W)

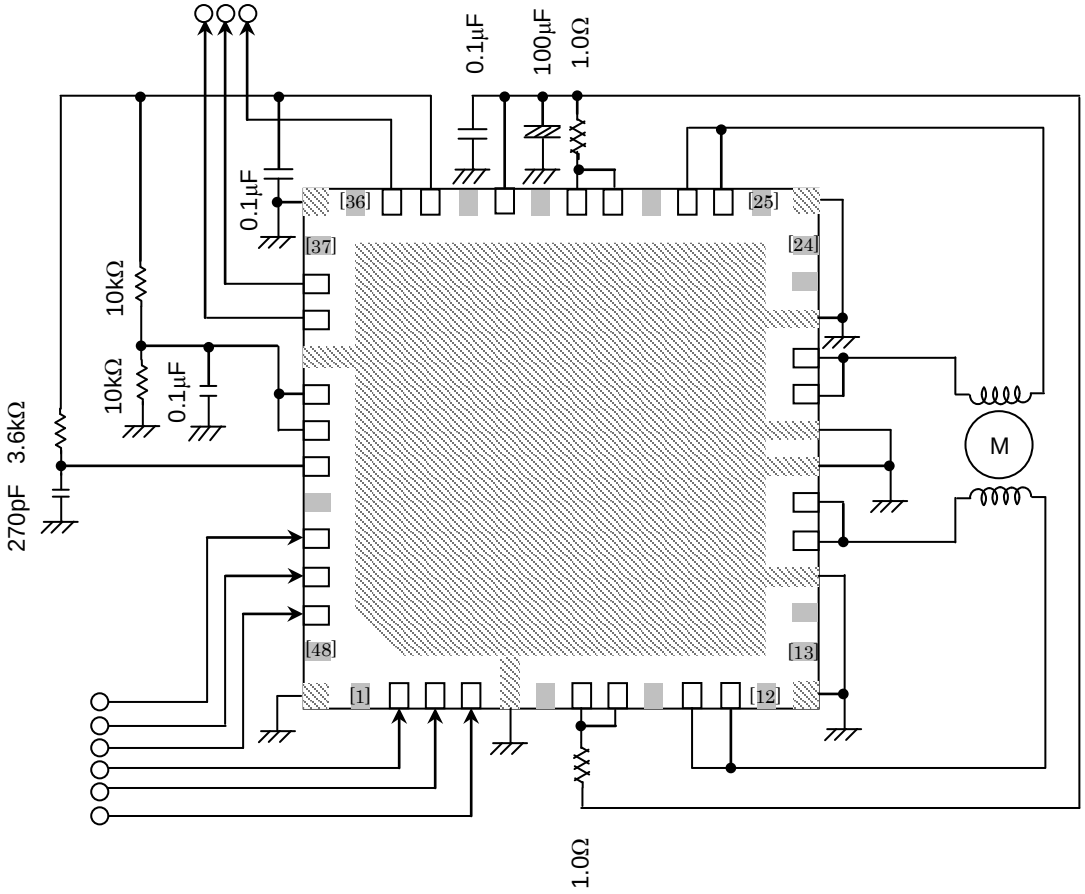
-> If the ambient temperature is above 25°C, please de-rate by 10.4mW/°C

(2) … When mounted to a 4 layer glass epoxy board (power dissipation example of Rth(j-a)=25°C/W (when mounted); dependent of board and mount condition.)

-> If the ambient temperature is above 25°C, please de-rate by 33.3mW/°C

TB67S265FTG Application circuit example

(Each constant of external components are for reference.)



Note) The shaded area above shows the GND pin and area, also the area shown in gray is non-connection pins.

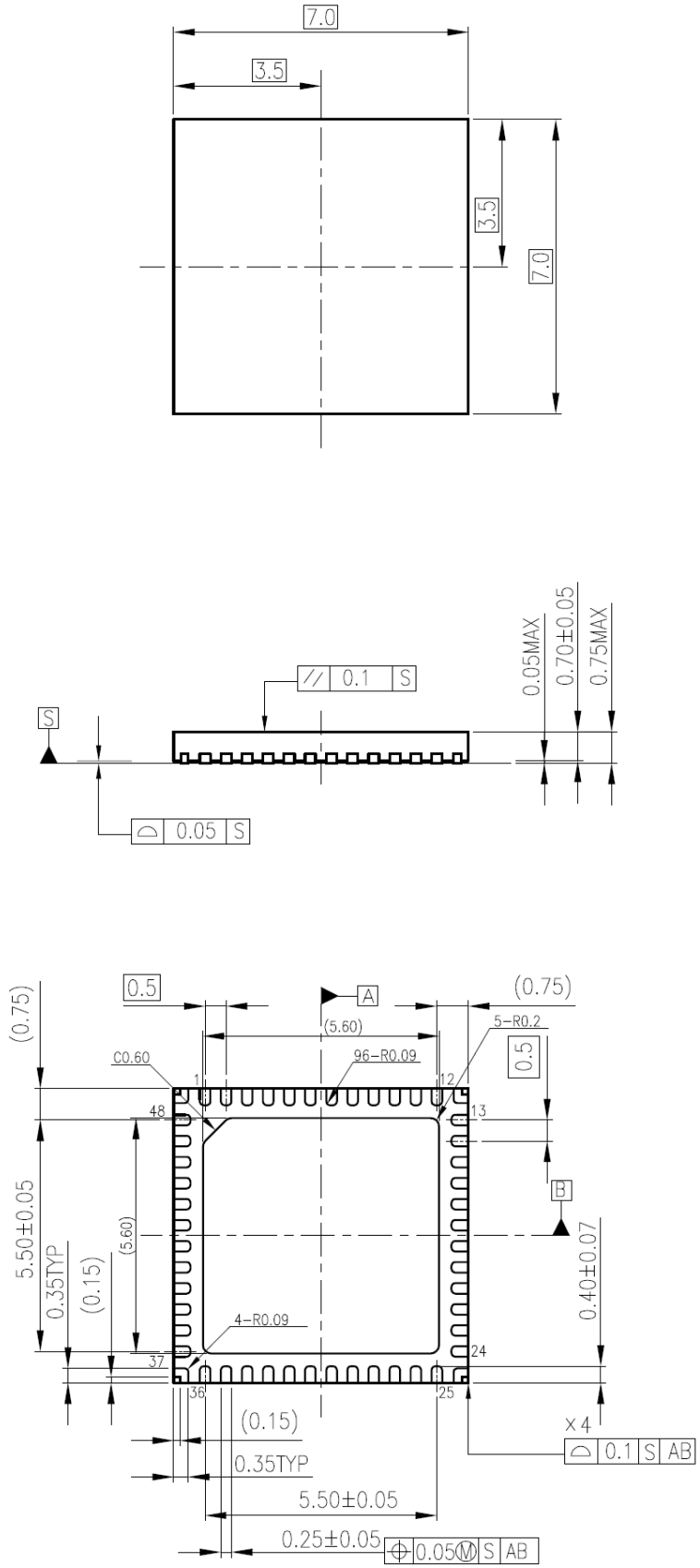
Please consider adding capacitors if necessary. Also, make sure that the GND pattern is connected at a single point if possible. There are two pins each for OUT_A-,OUT_A+,OUT_B-,OUT_B+, therefore make sure to connect the both pins when using the device.

Please mount the four corner pins of the QFN package and the exposed pad to the GND area of the PCB.

The application circuit above is an example; therefore, mass-production design is not guaranteed.

Package Dimensions

P-WQFN48-0707-0.50-003 **Unit: mm**



Weight: 0.10 g (Typ.)

Notes on Contents

Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Timing Charts

Timing charts may be simplified for explanatory purposes.

Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass-production design stage.
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Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

(2)
Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of overcurrent and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.
In addition, do not use any device inserted in the wrong orientation or incorrectly to which current is applied even just once.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as from input or negative feedback capacitor, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure may cause smoke or ignition. (The overcurrent may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

Overcurrent detection Circuit

Overcurrent detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the overcurrent detection circuits operate against the overcurrent, clear the overcurrent status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the overcurrent detection circuit to operate improperly or IC breakdown may occur before operation. In addition, depending on the method of use and usage conditions, if overcurrent continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over-temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, exceeding absolute maximum ratings may cause the thermal shutdown circuit to operate improperly or IC breakdown to occur before operation.

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, design the device so that heat is appropriately radiated, in order not to exceed the specified junction temperature (Tj) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, when designing the device, take into consideration the effect of IC heat radiation with peripheral components.

Back-EMF

When a motor rotates in the reverse direction, stops or slows abruptly, current flows back to the motor's power supply owing to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond the absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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