TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB62771FTG

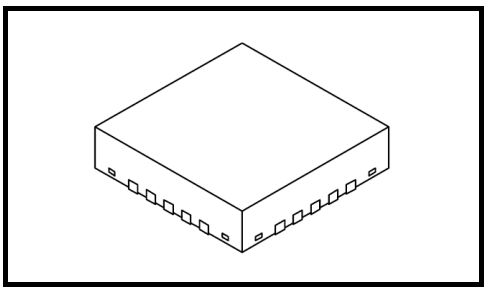
Step-up DC/DC controller built in 4-channel sink driver for white LED

1. General description

TB62771FTG is a large-current LED driver IC incorporating DC/DC controller for high-power LED systems.

This IC can drive high-intensity and large-current LED connected to 4 constant current sinks.

This IC is for driving backlight of white LEDs for large LCD.

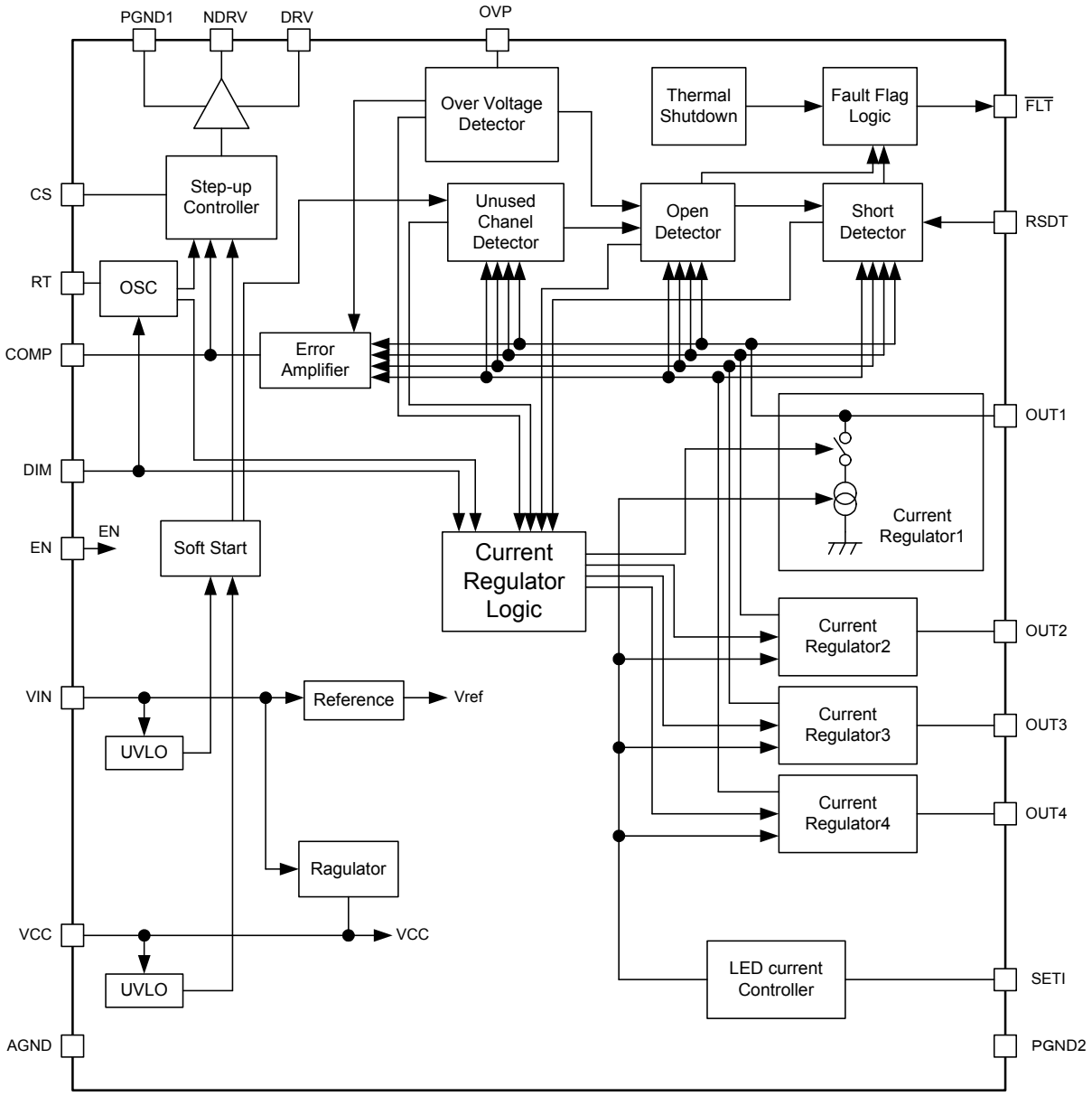


Weight : 0.03 g (TYP.)

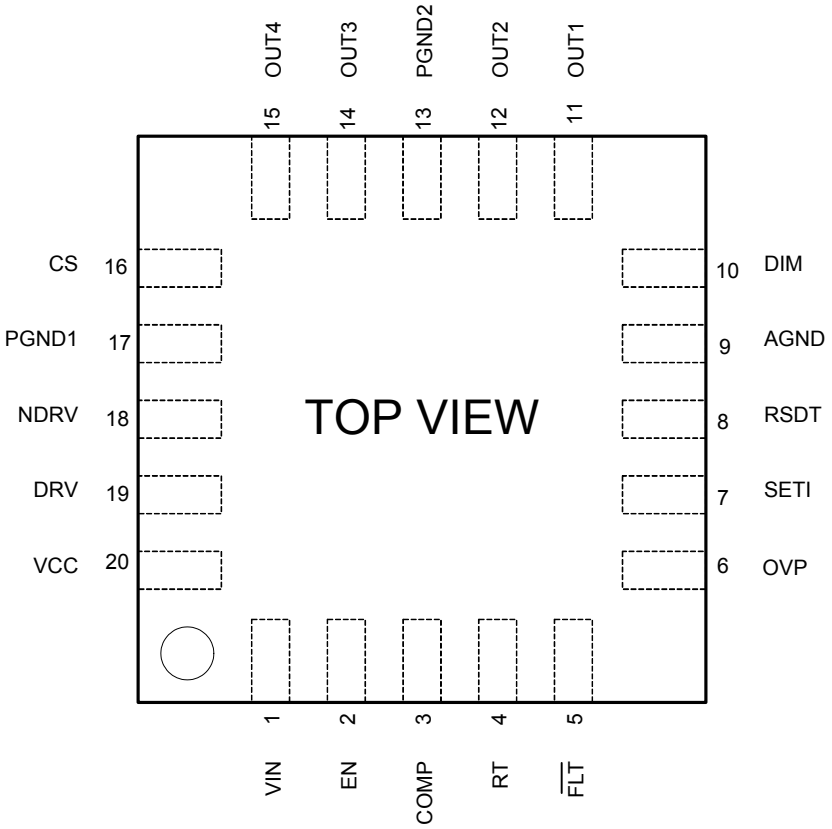
2. Features

- Input voltage range : 4.75 V to 40 V
- Built in current mode DC/DC controller
- Switching frequency:
  Set by the resistance connected to RT terminal (200 kHz to 2.0 MHz), Synchronization with external clock
- 4ch constant current driver:
  Sink current 20 mA to 150 mA
  Current accuracy +/- 2% (ILED = 100 mA, between channels)
  Control voltage for minimum OUT terminal 0.5 V (ILED = 150 mA)
- Dimming control: Input PWM range 100 Hz to 30 kHz
  Minimum pulse width of input PWM 330 ns
- Detection circuit:
  VIN under voltage lockout (UVLO(VIN))
  VCC under voltage lockout (UVLO(VCC))
  LED open detection
  LED short detection (Set by the resistance connected to RSDT terminal)
  Built in thermal shutdown circuit
  Overvoltage detection (set by external resistance)
- Soft start function
- Output delay function
- Shutdown consumption current 40 μA (max)
- IC package:P-WQFN20-0404-0.50-002

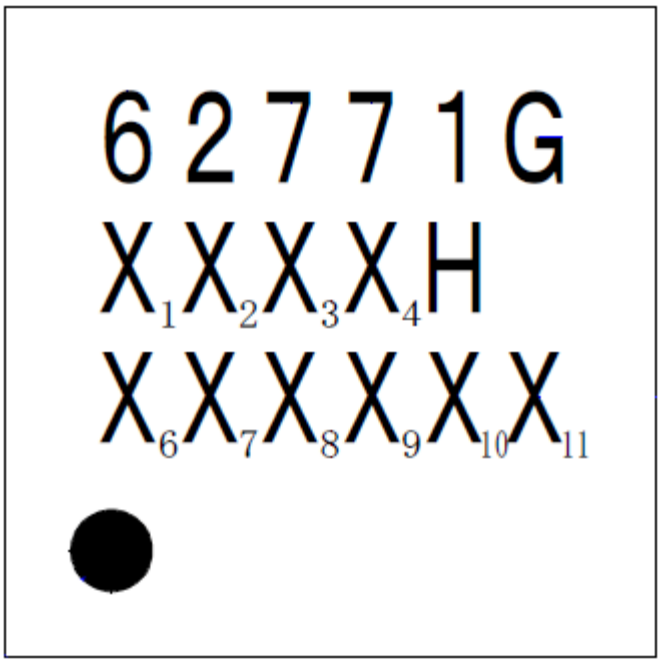
3. Block Diagram



4. Pin Assignment (Top view)



5. Marking (Top view)



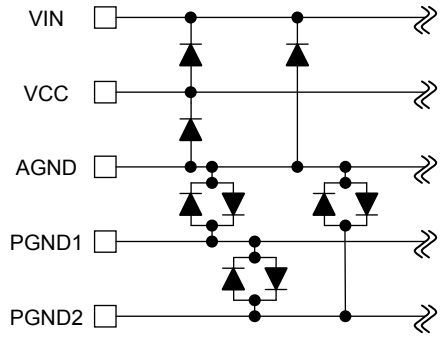
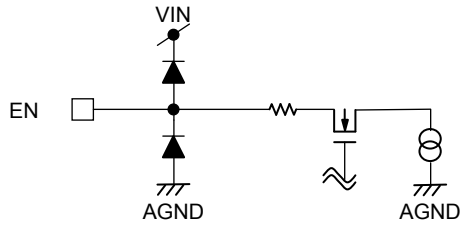
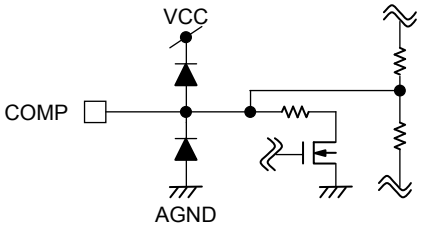
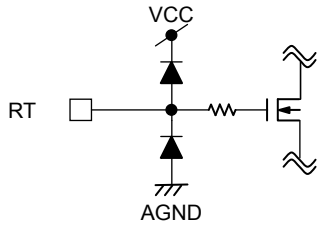
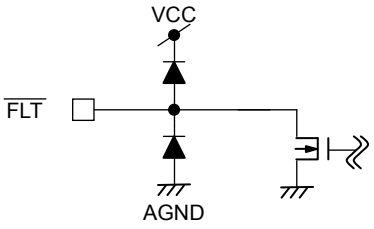
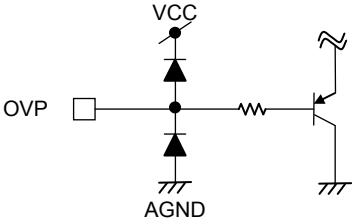
X_1 ,X_2 : Yearly code (last 2 digits of the year of manufacture)
X_3 ,X_4 : Weekly code
X_6 toX_{11} : Lot trace code

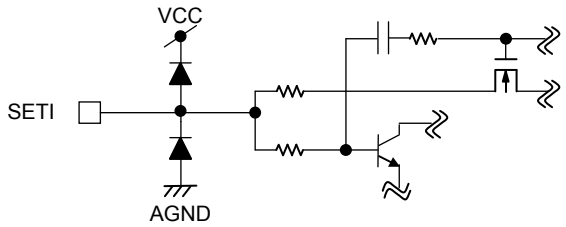
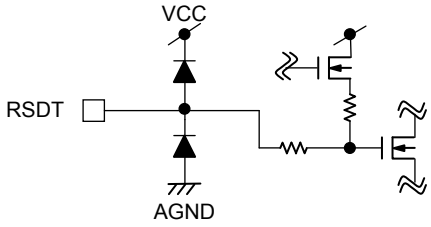
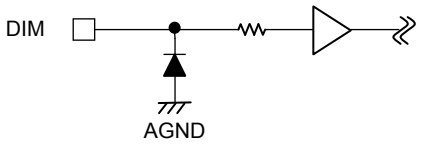
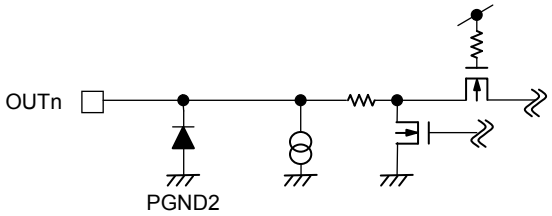
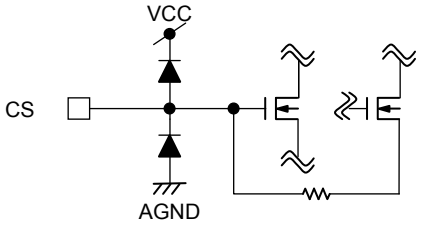
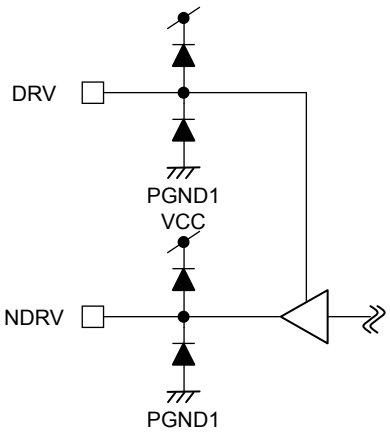
6. Pin function

No	Name	I/O (Note)	Function
1	VIN	P	Power supply input.
2	EN	I	Input chip enable signal, EN=High: operation mode or standby mode, EN=Low: shutdown mode.
3	COMP	O	Terminal for controlling compensation point of AMP that controls output voltage. Connect RC between COMP and AGND.
4	RT	I	Internal oscillator setting terminal. Connect RT resistor to AGND.
5	$\overline{\text{FLT}}$	O	Error signal output by fault protection control (Nch open drain) , This terminal is set Low in detecting LED Open, LED Short, and thermal shutdown. Connect a pull-up resistor of 10kΩ from FLT to VCC.
6	OVP	I	Overvoltage threshold adjust input. Connect a divided resistance from the switching convertor output to OVP and AGND. The OVP comparator reference is set 1.23V internally.
7	SETI	O	LED current adjust input. Connect a resistor (RSETI) to AGND.
8	RSDT	I	LED short detection adjusting input. Connect a divided resistance from VCC to AGND. Connect RSDT directly to VCC to disable LED short detection.
9	AGND	P	Ground for logic signal. Connect to PGND1, PGND2.
10	DIM	I	Digital PWM dimming input. DIM = High: Operation mode DIM = Low: Standby mode. Connect DIM to VCC if dimming control is not used (continuous constant current operation). *The minimum pulse width which can be inputted is 330 ns. When a pulse of the width less than 330ns is input, it may not operate normally.
11	OUT1	O	Constant current sink terminals to drive LED for channel 1. This terminal is open drain output that sinks up to 150mA.
12	OUT2	O	Constant current sink terminals to drive LED for channel 2. This terminal is open drain output that sinks up to 150mA.
13	PGND2	P	Power Ground. Connect PGND2 to AGND and PGND1.
14	OUT3	O	Constant current sink terminals to drive LED for channel 3. This terminal is open drain output that sinks up to 150mA.
15	OUT4	O	Constant current sink terminals to drive LED for channel 4. This terminal is open drain output that sinks up to 150mA.
16	CS	I	Current sense input It monitors the current of external power MOSFET source.
17	PGND1	P	Power Ground. Connect PGND1 to AGND and PGND2.
18	NDRV	O	Switching n-MOSFET gate driver output.
19	DRV	I	Power Supply input for the control circuits of switching MOSFET gate. Connect Resistance between DRV and 5V regulator output VCC. And connect DRV and PGND with minimum of 0.1μF Bypass capacitor.
20	VCC	O	5V Regulator Output. Connect minimum of 1.0μF capacitor between VCC and AGND as close to the device as possible.

Note. : I: Input terminal
O: Output terminal
P: Power supply terminal

7. Equivalent circuits of terminals

Pin No.	Pin name	Equivalent circuit
1	VIN	
9	AGND	
13	PGND2	
17	PGND1	
20	VCC	
2	EN	
3	COMP	
4	RT	
5	$\overline{\text{FLT}}$	
6	OVP	

No.	Pin name	Equivalent circuit
7	SETI	
8	RSDT	
10	DIM	
11 12 14 15	OUT1 OUT2 OUT3 OUT4	
16	CS	
18	NDRV	
19	DRV	

8. Absolute Maximum Ratings (Ta = 25°C Unless otherwise specified)

Characteristics	Symbol	condition	Rating	Unit
Power supply voltage	V_{IN}	-	−0.3 to +45	V
Input voltage1	V_{IN1}	EN	−0.3 to V_{IN} +0.3	V
Input voltage2	V_{IN2}	DRV, $\overline{FLT}$, DIM, RSDT, OVP	−0.3 to +6	V
Input voltage3	V_{IN3}	CS, RT, COMP, SETI	−0.3 to V_{CC} +0.3	V
Input voltage4	V_{IN4}	NDRV	−0.3 to V_{DRV} +0.3	V
Output voltage	V_{out}	OUT1, OUT2, OUT3, OUT4	−0.3 to +45	V
Power dissipation	P_D	Exposed Pad mounting (Note1,2)	3.2	W
Saturated heat resistance	$R_{th\ (j-a)}$	Exposed Pad mounting (Note1,2)	39	°C/W
Operation temperature range	Topr	-	−40 to +85	°C
Storage temperature range	Tstg	-	−65 to +150	°C
Maximum junction temperature	Tj	-	150	°C

Note1: PCB condition is 74mm×74mm×1.6 mm, 4layer, FR-4

Note2: When ambient temperature is 25°C or more, reciprocal of saturated heat resistance (1/Rth(j-a)) should be reduced every 1°C rise.

9. Electrical Characteristics

(Unless otherwise specified, V_{IN} = V_{EN} = 12V, R_{SETI} = 15kΩ, C_{VCC} = 1μF, V_{CC} = V_{DRV}, NDRV = COMP = OUT = Open, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = V_{CS} =V_{PGND1} = V_{PGND2} = V_{AGND} = 0V, Ta = -40 to 85°C, Typical values are at Ta = 25°C condition)

VIN input

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Power supply voltage	V_{IN}	-	4.75	-	40	V
Operating consumption current	$I_{IN(ON)}$	RT = 7.35 x 10^9/fsw	-	4.5	5.5	mA
Shutdown consumption current	$I_{IN(OFF)}$	V_{EN} = 0V	-	15	40	μA
VIN under lock out voltage	UVLO_VIN	V_{IN} rising	3.975	4.3	4.625	V
VIN under lock out voltage hysteresis	$UVLO\_VIN_{HYS}$	-	-	170	-	mV

Electrical Characteristics

(Unless otherwise specified, V_{IN} = V_{EN} = 12V, R_{SETI} = 15kΩ, C_{VCC} = 1μF, V_{CC} = V_{DRV}, NDRV = COMP = OUT = Open, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = V_{CS} =V_{PGND1} = V_{PGND2} = V_{AGND} = 0V, Ta = -40 to 85°C, Typical values are at Ta = 25°C condition)

VCC REGULATOR

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
VCC output voltage	V_{CC}	6.5V < VIN < 10V, 1mA < ILOAD < 50mA 10V < VIN < 40V, 1mA < ILOAD < 10mA	4.75	5.0	5.25	V
VCC drop voltage	VCC_{DROP}	VIN - VCC, VIN = 4.75V, ILOAD = 50mA	-	200	500	mV
VCC current limit	ICC_{LIMIT}	VCC connects to AGND	-	100	-	mA
VCC under lock out voltage	UVLO_VCC	VCC rising	-	4	-	V
VCC under lock out voltage hysteresis	$UVLO\_VCC_{HYS}$	-	-	100	-	mV

RT OSCILLATOR

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Switching frequency	f_{SW}	-	200	-	2000	kHz
Maximum duty cycle	Dmax	f_{SW} = 200kHz to 600kHz	90	94	98	%
		f_{SW} = 600kHz to 2000kHz	86	90	94	
Frequency accuracy (Note3)	-	f_{SW} = 200kHz to 2000kHz	-7	-	7	%
Synchronized signal threshold voltage	-	-	4	-	-	V
Minimum synchronized frequency	-	-	$1.1f_{SW}$	-	-	Hz

Note3: Relative accuracy to typical characteristic.

PWM COMPARATOR

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
PWM comparator Leading-edge blanking time (Note4)	-	-	-	60	-	ns
PWM-NDRV propagation delay (Note4)	-	-	-	90	-	ns

SLOPE COMPENSATION

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Peak slope compensation current	-	Peak slope for CS input	45	50	55	μA·fsw

Note4: This specification is design guarantee, not production tested.

Electrical Characteristics

(Unless otherwise specified, V_{IN} = V_{EN} = 12V, R_{SETI} = 15kΩ, C_{VCC} = 1μF, V_{CC} = V_{DRV}, NDRV = COMP = OUT = Open, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = V_{CS} =V_{PGND1} = V_{PGND2} = V_{AGND} = 0V, Ta = -40 to 85°C, Typical values are at Ta = 25°C condition)

CURRENT LIMIT COMPARATOR

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Current limit threshold	-	-	384	-	438	mV
CS limit comparator to NDRV propagation delay (Note4)	-	10mV over drive Leading-edge blanking time is not included.	-	10	-	ns

ERROR AMPLIFIER

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
OUT regulation voltage	-	20mA < ILED < 150mA	-	0.5	-	V
Trans conductance	gM	-	650	-	1450	μS
No load gain (Note4)	-	Gain = $\Delta V_{COMP} / \Delta VCS$ 0.05V < VCS < 0.15V.	-	75	-	dB
COMP sink current	-	VOUT=5V, V_{COMP} =2.5V	160	375	800	μA
COMP source current	-	VOUT=5V, V_{COMP}=2.5V	160	375	800	μA

MOSFET DRIVER

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
NDRV on resistance (Note4)	R_{ONNDRV}	ISINK = 100mA (nMOS)	-	0.9	-	Ω
		ISOURCE = 100mA (pMOS)	-	1.1	-	
Peak sink current (Note4)	-	VNDRV = 5V	-	2.0	-	A
Peak source current (Note4)	-	VNDRV = 0V	-	2.0	-	A
Rise time	-	CLOAD = 1nF	-	6	-	ns
Fall time	-	CLOAD = 1nF	-	6	-	ns

LED CURRENT

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
OUT current sink range	-	VOUT = VREF (0.5V)	20	-	150	mA
Channel to channel matching	-	IOUT = 100mA	-	-	±2	%
	-	IOUT = 100mA, all channels on	-	-	±1.5	%
Output current accuracy	-	IOUT = 100mA, Ta =-40 to 85°C	-	-	±3	mA
	-	IOUT = 50 to 150mA, Ta =-40 to 85°C	-	-	±3	mA
Output leakage current	$I_{OFFOUTn}$	VDIM = 0V, VOUT = 40V	-	-	1	μA

Note4: This specification is design guarantee, not production tested.

Electrical Characteristics

(Unless otherwise specified, V_{IN} = V_{EN} = 12V, R_{SETI} = 15kΩ, C_{VCC} = 1μF, V_{CC} = V_{DRV}, NDRV = COMP = OUT = Open, V_{RSDT} = V_{DIM} = V_{CC}, V_{OVP} = V_{CS} =V_{PGND1} = V_{PGND2} = V_{AGND} = 0V, Ta = -40 to 85°C, Typical values are at Ta = 25°C condition)

LOGIC INPUTS/OUTPUTS

Parameter	Symbol	Test Condition	Min	Typ.	Max	Unit
EN reference voltage	V_{EN}	VEN rising	1.150	1.275	1.400	V
EN hysteresis voltage	V_{HYSEN}	-	-	50	-	mV
EN input current	I_{INEN}	VEN = 40V	-	-	±250	nA
DIM input high voltage	V_{IHDIM}	-	2.1	-	5.5	V
DIM input low voltage	V_{ILDIM}	-	-	-	0.8	V
DIM hysteresis voltage	V_{HYSDIM}	-	-	250	-	mV
DIM input current	I_{INDIM}	-	-	-	±2	μA
DIM↑ to LED turn-on delay	-	DIM rising edge to IOUT↑(10% rise)	-	100	-	ns
DIM ↓to LED turn-off delay	-	DIM falling edge to IOUT↓(10% fall)	-	100	-	ns
IOUT rise and fall times	-	-	-	200	-	ns
/FLT output low voltage	V_{OLFLT}	VIN = 4.75V, ISINK = 5mA	-	-	0.4	V
/FLT output leakage current	I_{OFFFLT}	VFLT = 5.5V	-	-	1.0	μA
LED short detection threshold	V_{RSDT}	VRSDT=1V	3.0	3.5	4.0	V
Short detection comparator delay	-	-	-	6.5	-	μs
RSDT leakage current	I_{RSDT}	-	-	-	±600	nA
OVP detecting threshold	V_{OVP}	Output rising	1.19	1.228	1.266	V
OVP hysteresis voltage	V_{OVPHYS}	-	-	70	-	mV
OVP leakage current	I_{OVP}	VOVP = 1.25V	-	-	±600	nA

10. Operation mode

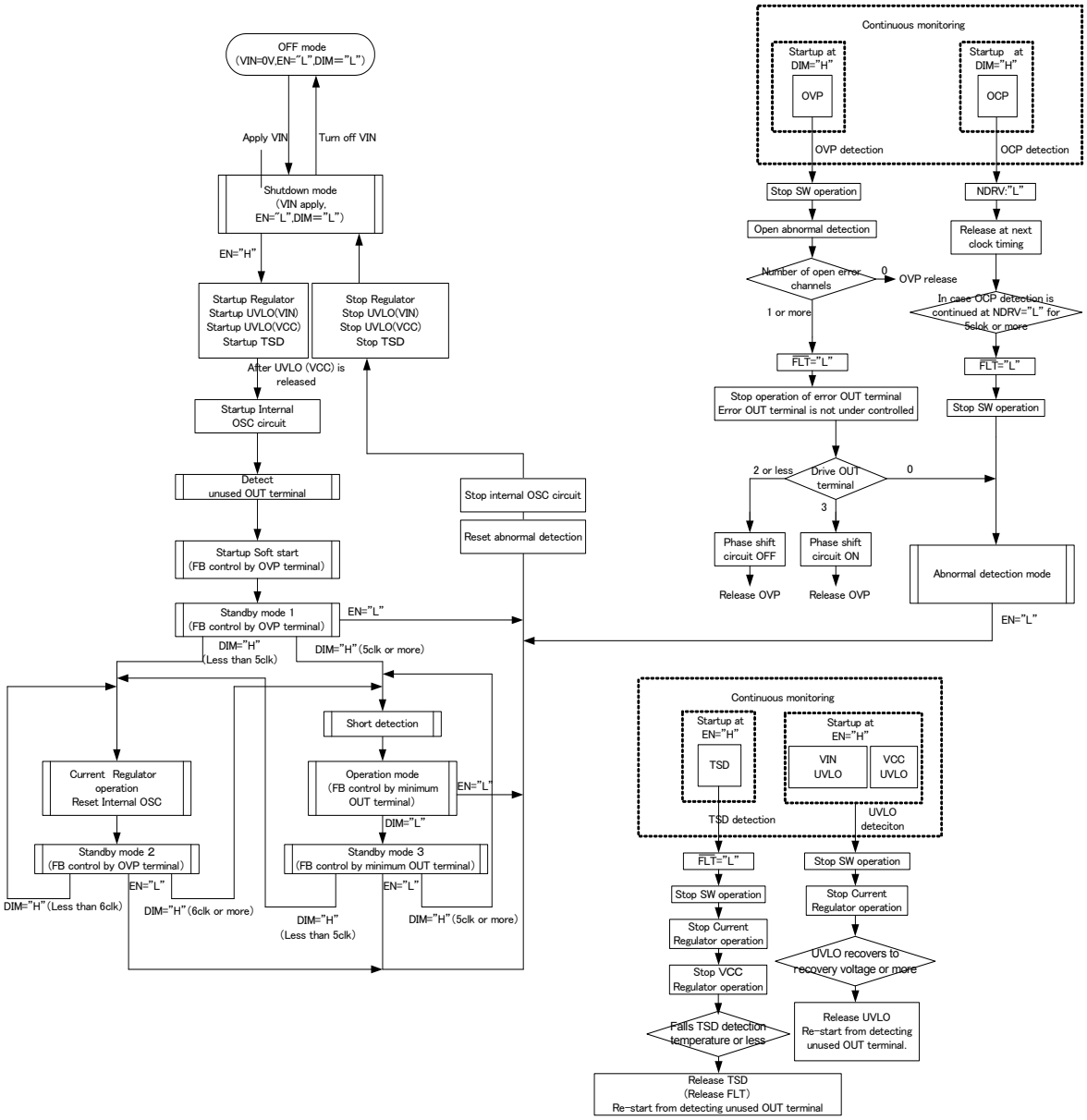
10.1 Mode change

Modes are selectable by 2 input signals.

EN input
- ・High : Stand-by Mode1, Stand-by Mode2, Operation Mode
  (Depend on DIM input condition. See the next page.)
- ・Low : Shutdown Mode

DIM input
- ・High : Operation Mode
- ・Low : Stand-by Mode1, Stand-by Mode2
  (See the next page.)

State of the IC is transferred to the operation mode by inputting high to EN terminal. DC/DC controller and constant current regulators are controlled by inputting signal from DIM terminal.
This IC has variable abnormal detecting circuits and controls the operation depending on the abnormal state.



10.1.1 Shutdown mode (EN="L")

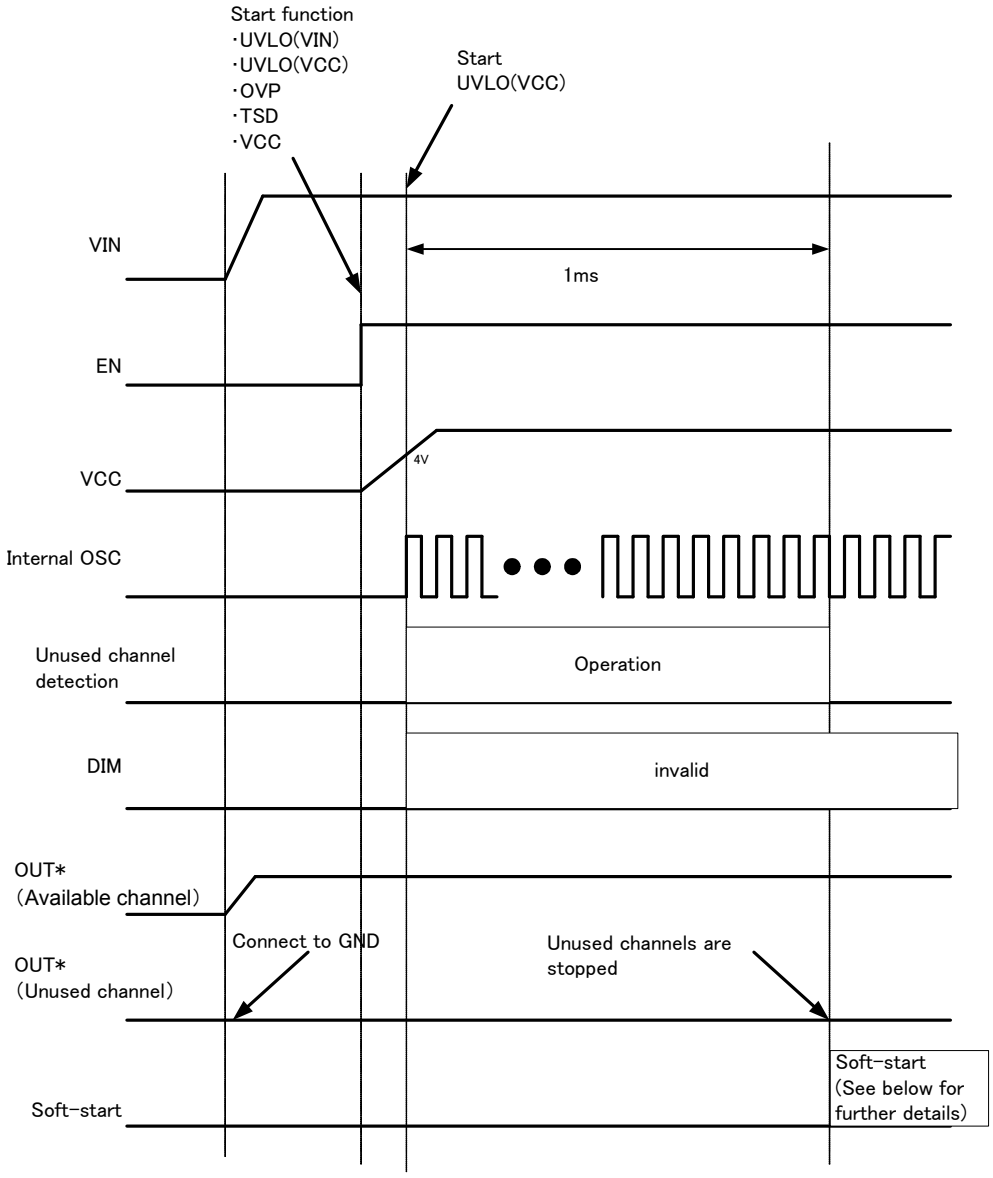
Power is supplied. IC operation halts.

10.1.2 Shutdown mode → Stand-by mode1 (EN="L" → "H")

Unused OUT terminals are detected when the operation moves from shutdown mode to standby mode. When unused channel is detected, it is eliminated from object of control and its constant current operation is turned off.
When unused channels are two or more, phase shift function is stopped. (Phase shift function is described later)
Then, voltage boosting starts and the operation moves to the soft start. As for voltage boosting, object of feedback control is OVP terminal whose voltage is 95% of the detection voltage.
Soft-start period is maximum 100ms. It doesn't depend on internal OSC frequency for DC-DC switching.

After soft start is finished, it shifts to Stand-by mode1 completely.

The conditions in which a soft start completes are the following three cases.
1) VLED (DC/DC convertor output) reaches OVP×95% level.
2) Constant current regulators are generated by inputting high to DIM. And the voltage of minimum OUT terminal reaches 0.5V.
3) 100ms (Typ.) passes.



10.1.3 Stand-by mode1 (EN="H", DIM="L")

The operation of the IC is shifted to Stand-by mode1 by inputting high to EN after power is supplied to VIN.
After soft start, VLED (DC/DC convertor output) is controlled to set the voltage of the OVP terminal to "OVP detection voltage×95%"

10.1.4 Stand-by mode2 (EN="H", DIM="L")

When pulse width of PWM input to DIM terminal is small (5 clocks or less), the operation of the IC is shifted to Stand-by mode2 while voltage of DIM is low.
Although constant current block is turned off by inputting low to DIM, DC/DC convertor is operated, and VLED is controlled to set the voltage of the OVP terminal to "OVP detection voltage×95%".

10.1.5 Stand-by mode3 (EN="H", DIM="L")

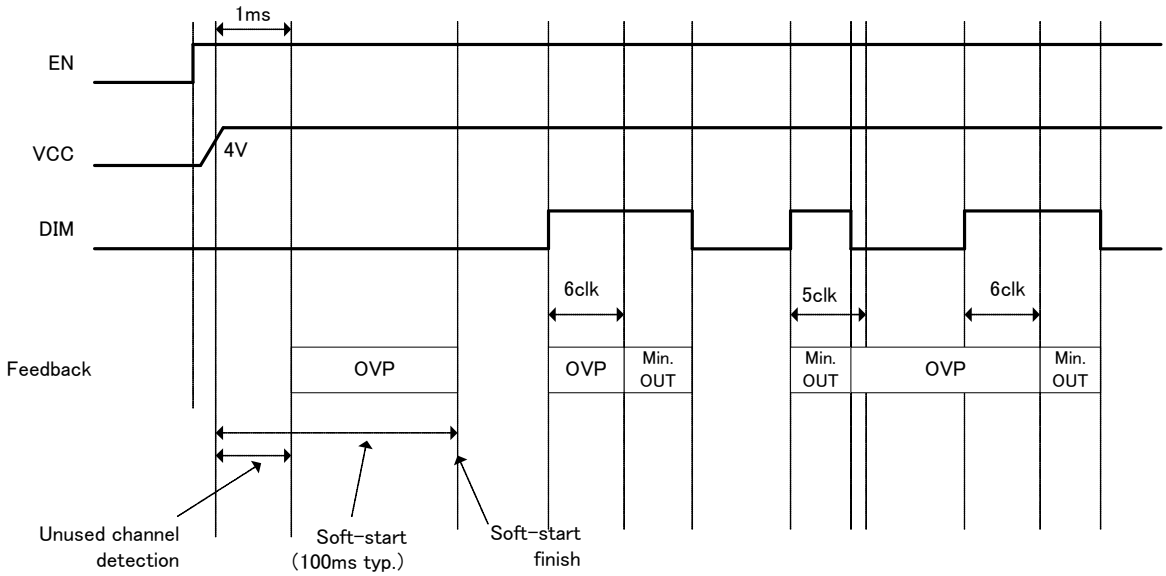
When pulse width of PWM input to DIM is 5 clocks or more, the operation of the IC is shifted to Stand-by mode3 while voltage of DIM is low.
DC/DC convertor is turned off.

10.1.6 Operation mode (EN="H", DIM="H")

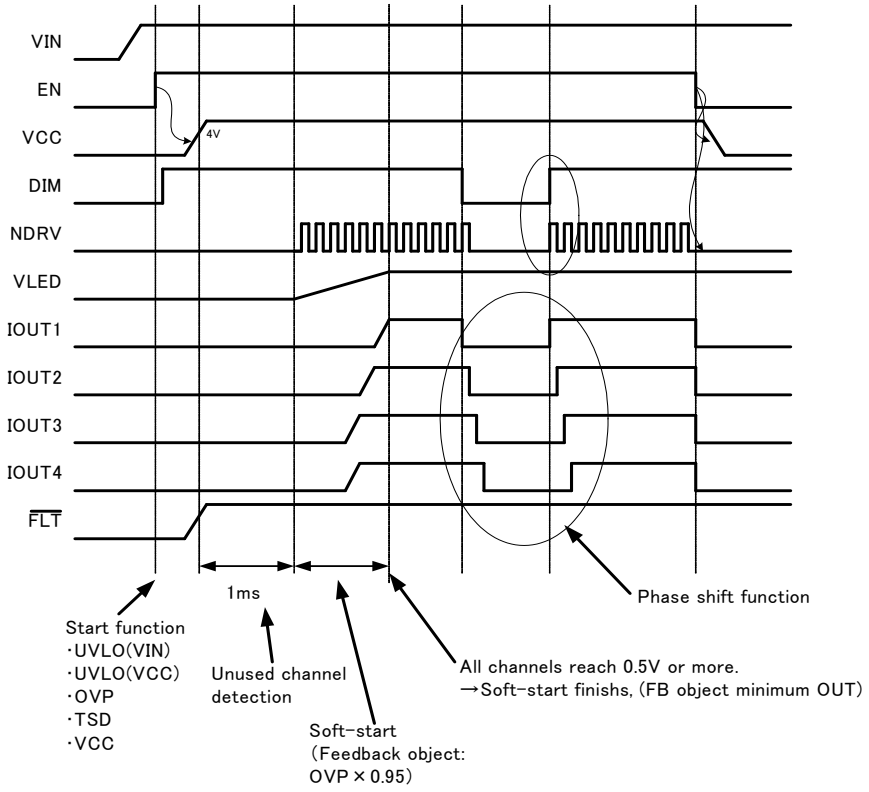
Both the DC/DC convertor and the constant current block are in operation mode.
The DC/DC convertor controls the boosted voltage to set the minimum OUT voltage to 0.5V (TYP.).

10.1.7 Mode transition

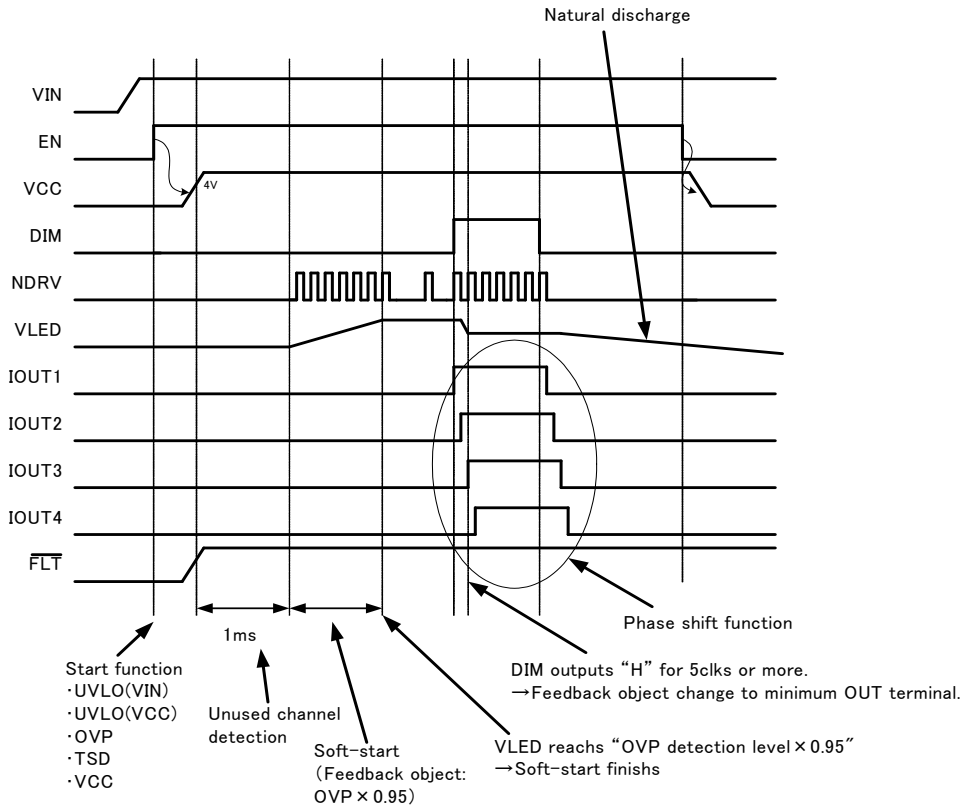
1) Example1 (Startup ~ PWM operation)



2) Example2 (DIM signal is inputted before soft-start)



3) Example3 (DIM signal is inputted after soft-start)



11. Explanation of Operation

11.1 Unused channel detection

When high signal is input to EN, unused channel detection is operated before soft start.
This function detects that the OUT terminals (OUT1 to 4) are connected to PGND at the same voltage.
Connect the OUT terminals of unused channel to PGND.
The constant current blocks of unused channel are turned off and removed from the object of LED open detection and LED short detection.

11.2 Dimming control

When high signal is input to DIM, constant current block operates and LED current is generated.
Constant current block operates ON/OFF synchronizing with DIM input.
Feedback control of DC/DC convertor in dimming has 2 modes and they depend on DIM pulse width.
Phase shift function (Delay between constant current channels) is incorporated to prevent simultaneous ON of constant current from rush current.

11.2.1 Minimum OUT control mode

When pulse width of DIM is 5clks or more of oscillation frequency, the object of feedback control of DC/DC convertor is the OUT terminal to which the lowest voltage is applied among OUT1, OUT2, OUT3, and OUT4. Voltage booster controls this minimum OUT voltage to be 0.5V (TYP.).
In OVP control mode, the operation shifts to minimum OUT terminal control mode when ON time of DIM corresponds to 6clks of the oscillation frequency or more.

11.2.2 OVP control mode

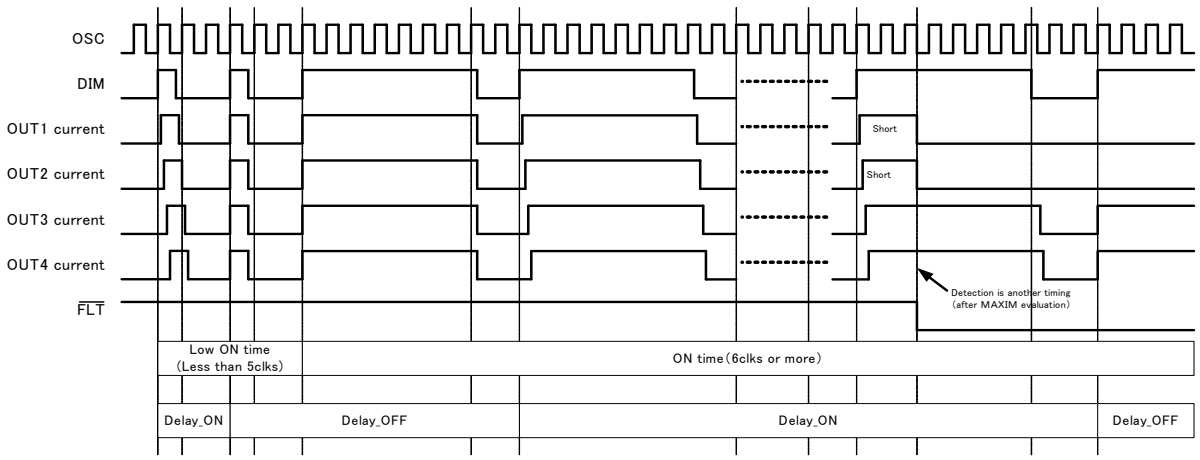
When ON time of DIM is less than 5clks of oscillation frequency, the object of feedback control for voltage booster is OVP detection voltage×95%. When the operation starts from OVP control mode, OVP control mode continues until ON time of DIM corresponds to 6clks of the oscillation frequency or more.
The minimum pulse width which can be inputted to DIM is 330ns. When a pulse of the width less than 330ns is input, it may not operate normally. Refer to Page1 (2.Features) and Page4 (6.Pin function).

11.2.3 Phase shift function (Delay between constant current channels)

OUT1 to OUT4 have the delay time of 100ns (typ.) at the ON timing of constant current circuit between each operation channel. So, sudden current increase caused by turning on OUT1 to 4 at the same time is avoided.
However, this delay time is omitted under the conditions below and constant current circuits between all operating channels are turned on at the same time. Delay circuit is tuned on just after the initial startup.
When ON time of DIM signal is less than 5clks at the initial operation, delay circuit is turned off at the next signal.

Conditions

1) ON time of DIM signal is less than 5clks. (When delay time is added again, the time is 6clks or more.)
2) Two or more of the OUT terminal controls are turned off among unused channel, open channel and short channel.



11.3 Oscillator

11.3.1 Frequency setting by external resistance (RT)

Oscillation frequency of boost switching is set by RT resistance connected between RT terminal and AGND.
Oscillation frequency is provided by the formula below.

$$RT = 7.350 \times 10^{9}/fsw$$

11.3.1 Oscillation by external signal input

Oscillation frequency synchronized with the external signal is set by inputting external signal to RT terminal.
External signal should be input by AC coupling, and the capacitance for AC coupling is provided by the formula below.

$$CSYNC \leqq \frac{9.862}{RT} - 0.144 \times 10^{-3} \quad (\mu F)$$

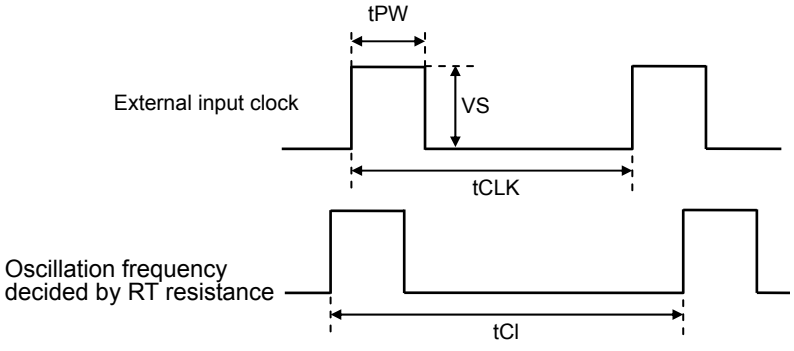
And input signal should fill next formula.

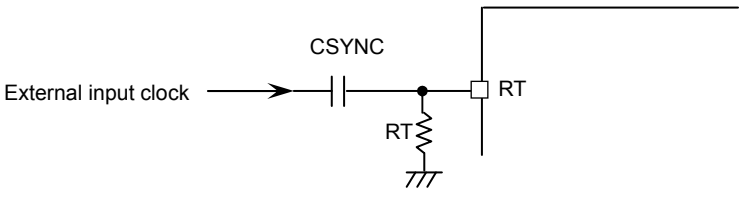
“

$$\frac{tPW}{tCLK} \times VS < 0.5$$

$$\left[0.8 - \frac{tPW}{tCLK} \times VS\right] + VS > 3.4$$

$$tPW < \frac{tCLK}{tCl} \times (tCl - 1.05 \times tCLK)$$





11.4 Constant current setting

Constant current (ILED) can be set by RISET resistance connected between ISET terminal and GND.
ILED is provided by the formula below.

ILED (mA) = 1.23(V) ÷RSETI (kΩ) ×1500

12. Error detection function

12.1 LED open detection and OVP detection

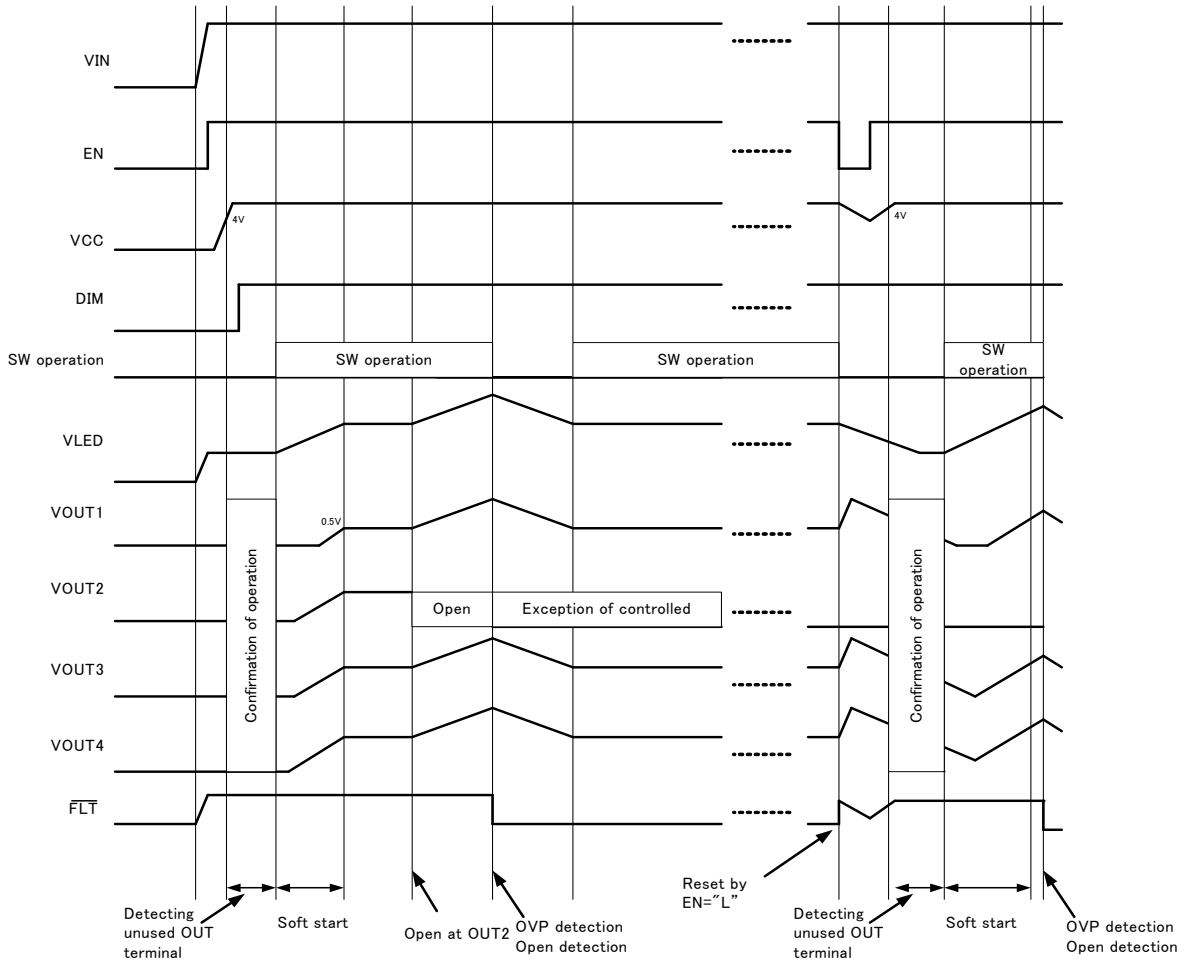
In the case that VLED rises and overvoltage is detected while object of feedback control is the minimum of OUT terminal, voltage boosting stops and the open state of OUT terminal is detected.

Voltage of OUT terminal that is open does not rise though VLED rises. Open state is detected by monitoring the voltage of this OUT terminal. Detecting voltage is 0.2V (typ.) or less.

When open state is detected, operation of only object OUT terminal is turned off. They are eliminated from feedback control target and low level is output to $\overline{FLT}$. Low level of $\overline{FLT}$ is resumed to high by applying voltage to the EN or to the power supply.

When voltage of OVP terminal falls 70 mV (typ.) lower than the detecting voltage after overvoltage is detected, SW operation is resumed.

In the case that operation is resumed without abnormity of open, $\overline{FLT}$ signal does not output.



12.2 LED short detection

When high voltage is input to DIM, short detection starts in the IC after 6μs passes. In controlling mode of OVP×95%, short detection does not operate though high voltage is input to DIM.

Voltage of OUT terminal that detects short is defined in the formula below.

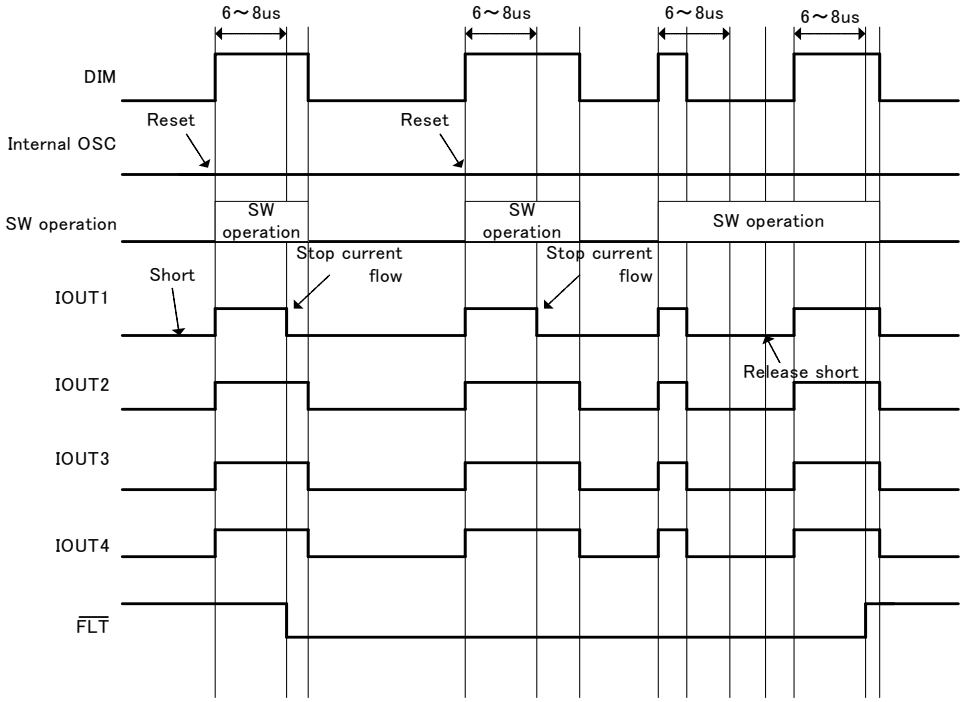
Short detection level = 3.5 × VRSDT

VRSDT corresponds to voltage of RSDT terminal. Apply the voltage set by divided resistance between VCC and AGND of external IC.

Short detection operates while DIM outputs high. When short state is detected for 2 μs or longer, operation of target OUT terminal is turned off and they are eliminated from feedback control target. Then low level is output to $\overline{FLT}$.

However, short state is released during operation, operation of target OUT terminal is resumed and they become object of feedback control. Then outputting low to $\overline{FLT}$ is released. To confirm the release of short state, detected OUT terminal operates with constant current drive for 6 to 8μs after DIM input.

Sequence of detection of short-circuit (Operation of channel delay function is omitted)



12.3 TSD (Thermal shut down circuit)

It monitors the temperature of internal IC. When TSD operates, operations of all circuits are turned off. When TSD detecting temperature falls to recovery temperature or lower, regulator of 5 V operates, unused OUT terminal is detected, and soft-start function starts up.

12.4 OCP (Over current protection)

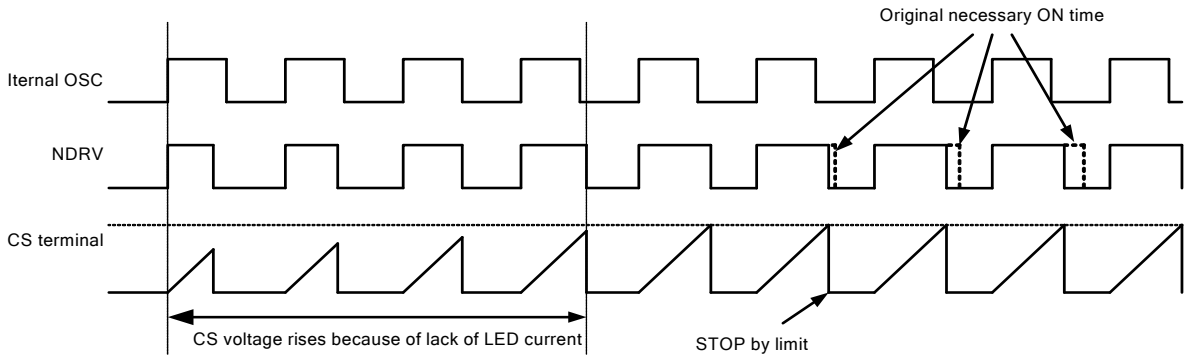
Current flowing through external MOS is monitored by monitoring the voltage of CS terminal connected to the source terminal of the external MOS. CS terminal is connected to the external MOS through the resistance for the slope compensation.

Detecting mask of 10 ns (typ.) is incorporated to avoid error detection by noise. This noise is generated when “H” is output from NDRV at the high edge of DIM.

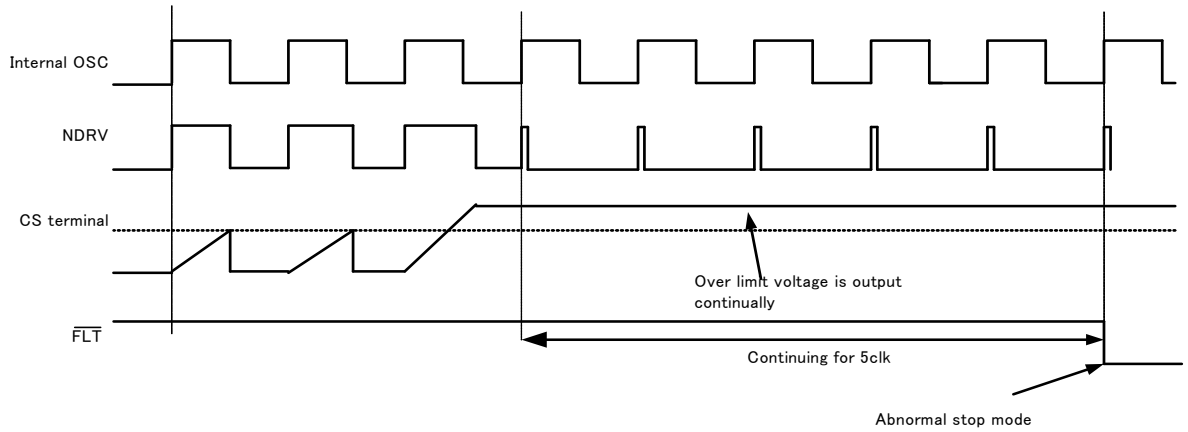
When the voltage of CS terminal exceeds the limit during normal operation, low level is output to NDRV terminal immediately and the external MOS is turned off. However, error signal is not output in special. The normal operation is resumed from the next cycle.

In the case that the voltage that is over specification is detected in CS terminal for 5clks or more though external MOS is turned off, all operations except regulator are turned off. And the abnormal operation is stopped by outputting low level to $\overline{FLT}$. To release this error protection, apply voltage to EN or to power supply.

1) Limit of voltage DC/DC operation by CS limit function



2) Stop abnormal operation by CS limit over



12.5 UVLO1 (VIN under voltage lockout)

Voltage of VIN is monitored. It is monitored just after ”H” is input to EN. When VIN falls to specified voltage or lower, all operations except that of the regulator are turned off.

Regulator operates by operable voltage. When VIN recovers to the recovery voltage or higher, the operation is resumed. At this time, unused OUT terminal is detected at first.

12.6 UVLO2 (VCC under voltage lockout)

The voltage of regulator is monitored. It starts just after “H” is input to EN. When voltage of regulator output falls to specified voltage or lower, all outputs except regulator are turned off. Regulator operates by operable voltage.

When output voltage of regulator rises to recovery voltage or higher, the operation is resumed. At this time, unused OUT terminal is detected at first.

12.7 Detecting functions

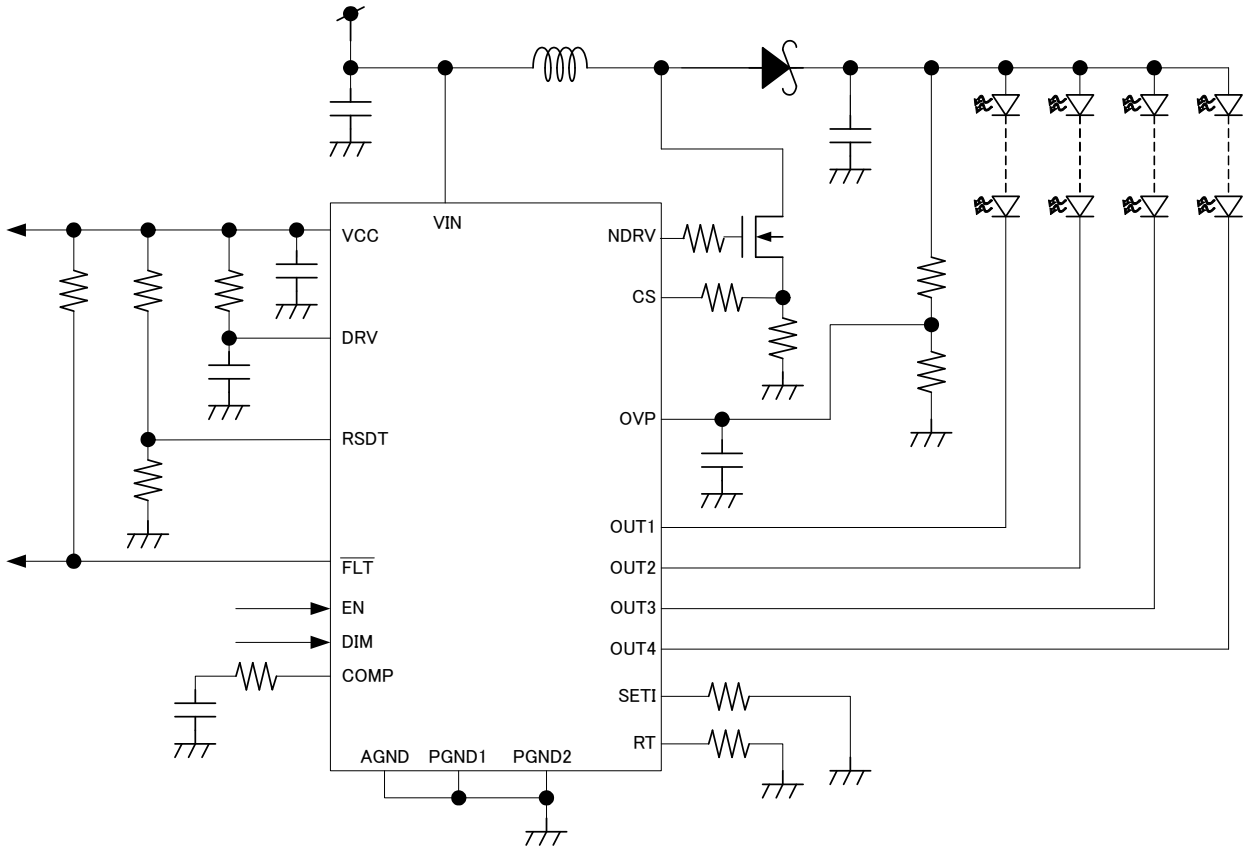
12.7.1 Table of detections

Detection	Function	Conditions for starting detection	$\overline{FLT}$
TSD	All functions are turned off when the temperature of the IC exceeds detection temperature. When the temperature falls release voltage from the detecting temperature, the operation is resumed. The starting sequence of this case is the same as the sequence just after EN input.	After EN signal is input ”H”.	---
UVLO1 (VIN)	All functions (except regulator.) are turned off when VIN falls below detecting voltage. When the voltage rises to the detecting voltage or more, the operation is resumed. The starting sequence of this case is the same as the sequence just after EN input.	After EN signal is input ”H”.	---
UVLO2 (VCC)	All functions (except regulator.) are turned off when VCC falls below detecting voltage. Shutdown signal (=EN: ”L”) is output internally. When the voltage rises to the detecting value or more, the operation is resumed. The starting sequence of this case is the same as the sequence of EN input.	After EN signal is input ”H”.	---
OVP	SW operation stops when the voltage of OVP rises to the detecting voltage or more. SW operation restarts when the voltage falls below the detecting voltage.	After EN signal is input ”H”.	---
OCP	In the case that the voltage of CS terminal rises to the detecting voltage or more, output of NDRV terminal is fixed low until the next cycle starts. In the case that the operation continues 5 cycles or more (including the state of fixing low for NDRV terminal), all functions (except regulator) are turned off by outputting low for FLT.	After DIM signal is input ”H”.	Less than 5 cycles:--- 5 cycles or more: L(Latch)
LED open	Operations of OUT terminals, which are detecting voltage or less just after OVP detection, are turned off. They are eliminated from object of controlling the minimum OUT terminal voltage. When all operations of OUT terminal are turned off because of abnormal state, all functions (except regulator) are turned off.	Just after OVP detection	$\overline{FLT}$ =L (Latch)
LED short	Detection starts 6μs (typ.) after DIM is input high and operations of OUT terminals, which are detecting voltage or more, are turned off. They are eliminated from object of controlling the minimum OUT terminal voltage. When all operations of OUT terminal are turned off because of abnormal state, all functions (except regulator) are turned off.	From Six to eight μs after DIM is input “H”.	$\overline{FLT}$ =L When short detection is released and other abnormal conditions are not detected, operation is resumed.

12.7.2 State of each block in detection

Detection		Conditions	Detection operation			Method of re-startup
			VCC	DC/DC control	Constant current	
TSD		T > 165℃(TYP.)	Stop	Stop	Stop	TSD recovery voltage or less.
UVLO1(VIN)		VIN < 4.13V(TYP.) @VIN falling	Continue	Stop	Stop	VIN≥4.3V(TYP.) @VIN rising
UVLO2(VCC)		VCC < 3.9V(TYP.) @VCC falling	Continue	Stop	Stop	VCC≥4.0V(TYP.) @VCC rising
OVP		VOVP > 1.228V(TYP.) @ VOVP rising	Continue	Stop	Continue	When the voltage is OVP recovery voltage or less, operation is resumed.
OCP		CS> 0.433V(TYP.)	Continue	NDRV : L fixed	Continue	Recovering from the next cycle.
		CS> 0.433V (TYP.): for 5 cycles or more.	Continue	Stop	Stop	Recovering by re-applying voltage of EN or power supply.
LED Open	Some channel (not all)	VOUT* < 0.2V(TYP.)	Continue	Active	Only error terminal: Stop (Not controlled)	Recovering by re-applying voltage of EN or power supply.
	All channel		Continue	Stop	Stop	Recovering by re-applying voltage of EN or power supply.
LED Short	Some channel (not all)	VOUT*> 3.5(TYP.)×VRSDT	Continue	Active	Only error terminal: Stop (Not controlled)	When short error is released, it is resumed by inputting voltage of DIM at the next cycle
	All channel		Continue	Stop	Stop	

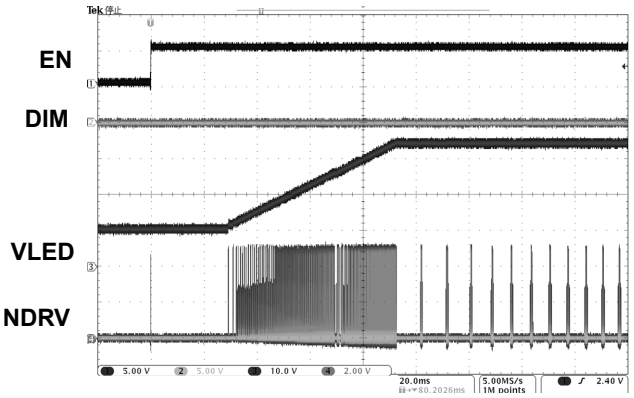
13. Application Circuit



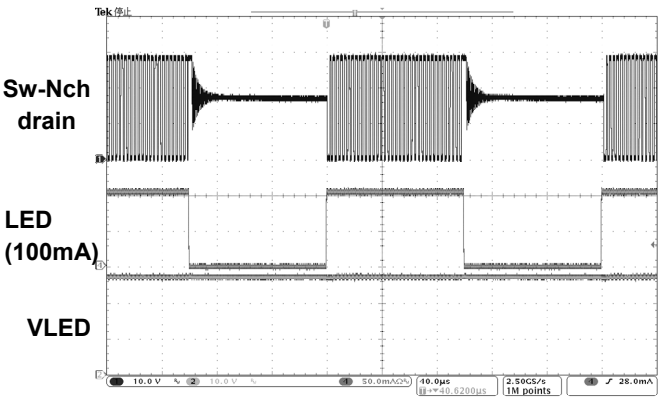
14. Characteristics (Reference data)

14.1 Characteristics Waveform (Reference data)

・Startup waveform (DIM=L)

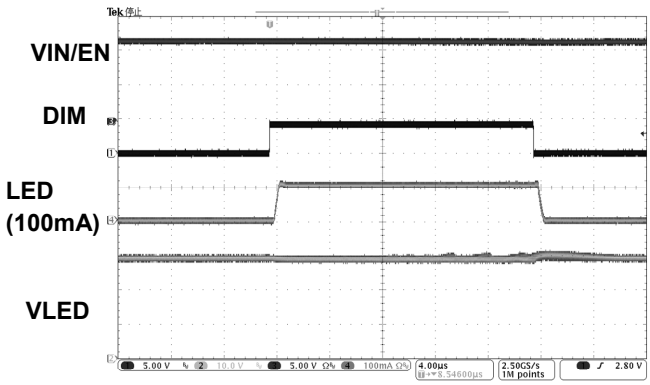


・Switching waveform (5kHz/50%Duty)

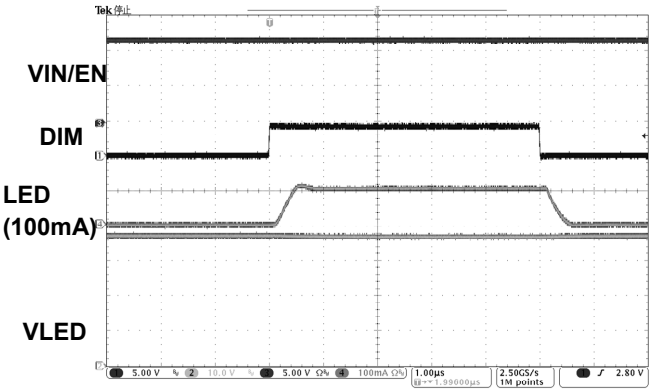


・Current (ILED) response

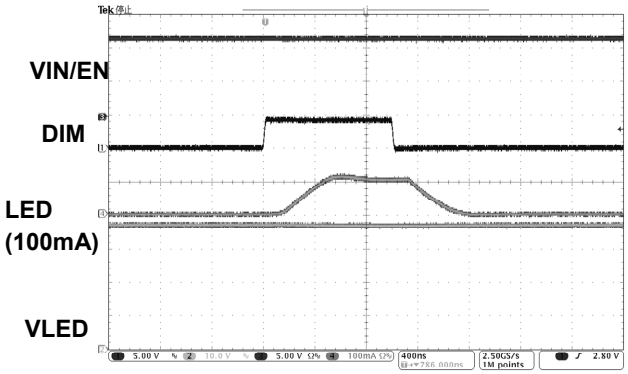
(DIM=20μs Pulse width)



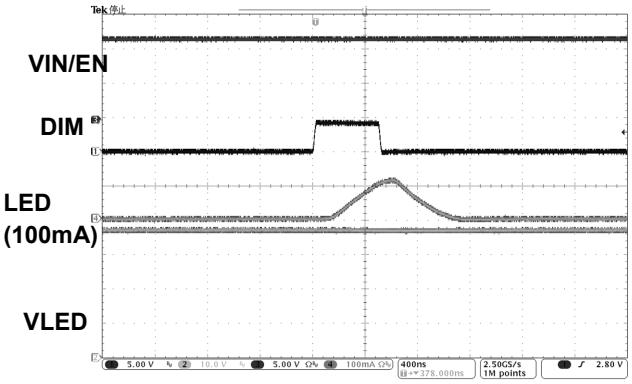
(DIM=5μs Pulse width)



(DIM=1μs Pulse width)

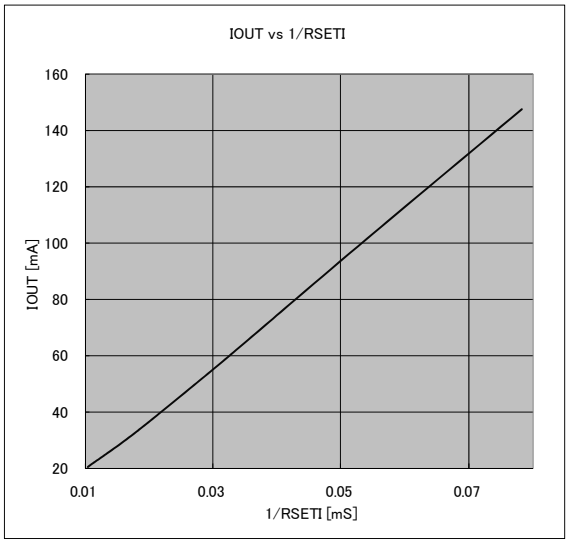


(DIM=0.5μs Pulse width)

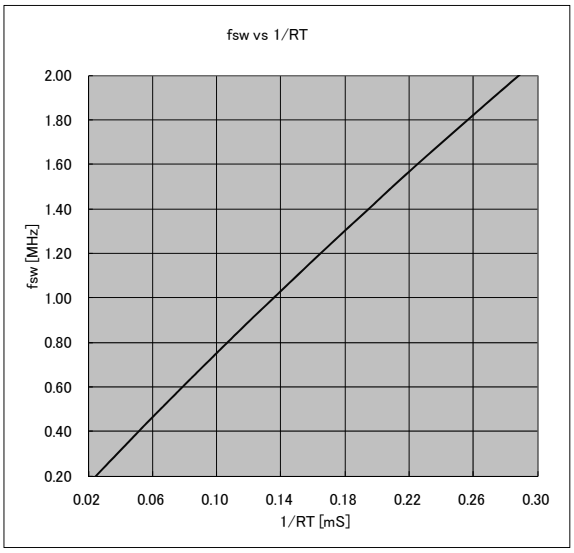


14.2 Characteristics Graph

・LED current (IOUT)

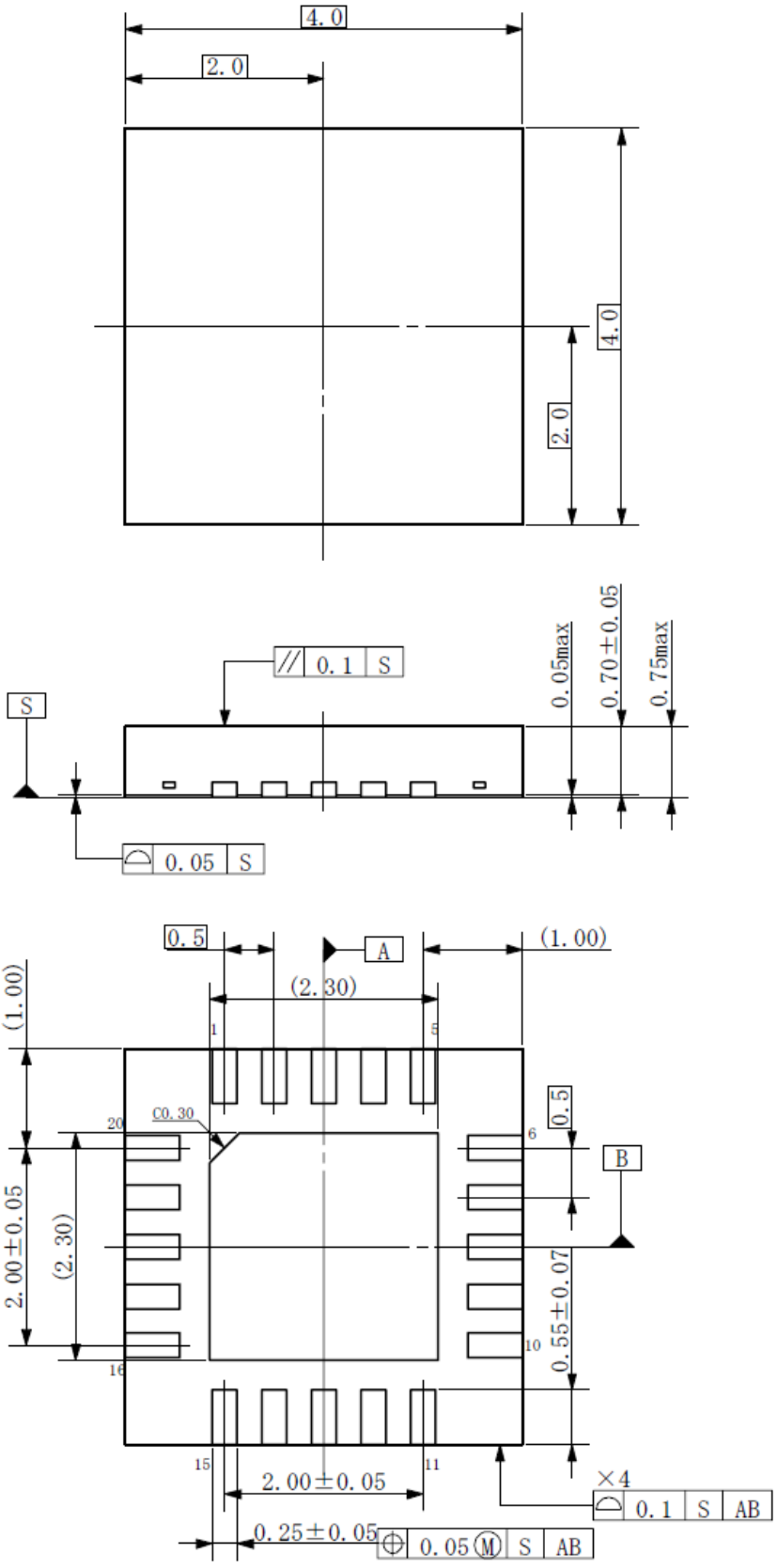


・Switching frequency (fsw)



Package Dimensions

P-WQFN20-0404-0.50-002 unit: mm



Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

[1] The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

[2] Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

[3] If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

[4] Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

[5] Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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