TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7W240FU

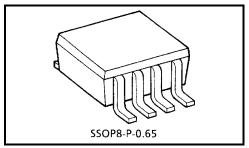
Inverted, 3-State Outputs

The TC7W240FU is a high speed C²MOS Dual Bus Buffers fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the C^2MOS low power dissipation.

It is an inverting 3-state buffer having two active-low output enables.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.02 g (typ.)

Features

- High speed: $t_{pd} = 10 \text{ ns}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 2 \mu A (max)$ at $Ta = 25^{\circ}C$
- High noise immunity: VNIH = VNIL = 28% VCC (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6 \text{ mA} (\text{min})$
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: VCC (opr) = 2 to 6 V

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7	V
DC input voltage	V _{IN}	-0.5 to V_{CC} + 0.5	V
DC output voltage	V _{OUT}	-0.5 to V_{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	I _{OK}	±20	mA
DC output current	IOUT	±35	mA
DC V _{CC} /ground current	ICC	±37.5	mA
Power dissipation	PD	300	mW
Storage temperature range	T _{stg}	-65 to 150	°C
Lead temperature (10 s)	ΤL	260	°C

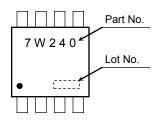
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

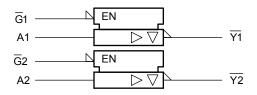
Start of commercial production 1993-04

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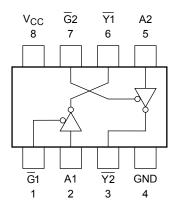
Marking



Logic Diagram



Pin Configuration (top view)



Truth Table

Inp	Output		
G	А	Ŧ	
L	L	Н	
L	Н	L	
Н	Х	Z	

X: Don't care Z: High impedance

Operating Ranges

Characteristics	Symbol	Rating	Unit	
Supply voltage	V _{CC}	2 to 6	V	
Input voltage	V _{IN}	0 to V _{CC}	V	
Output voltage	V _{OUT}	0 to V _{CC}	V	
Operating temperature range	T _{opr}	-40 to 85	°C	
		0 to 1000 (V _{CC} = 2.0 V)	ns	
Input rise and fall time	t _r , t _f	0 to 500 (V _{CC} = 4.5 V)		
		0 to 400 (V _{CC} = 6.0 V)		

Electrical Characteristics

DC Electrical Characteristics

Characteristics		Symbol Test Condition			Ta = 25°C		Ta = -40 to 85°C		Unit		
		Cymbol	1001	Test Condition		Min	Тур.	Max	Min	Max	Offic
Input voltage	High level	VIH	_		2.0	1.5		—	1.5		V
					4.5	3.15	_	_	3.15	—	
					6.0	4.2	_		4.2	_	
			_		2.0			0.5		0.5	
	Low level	VIL			4.5			1.35		1.35	
					6.0			1.8		1.8	
	High level	Vон	$V_{IN} = V_{IL}$	I _{OH} = -20 μA	2.0	1.9	2.0		1.9		
Output voltage					4.5	4.4	4.5		4.4		V
					6.0	5.9	6.0		5.9		
				I _{OH} = -6 mA	4.5	4.18	4.31	_	4.13	—	
				I _{OH} = -7.8 mA	6.0	5.68	5.80	_	5.63	—	
	Low level	V _{OL}	VIN = VIH or VIL	I _{OL} = 20 μA	2.0		0	0.1		0.1	
					4.5		0	0.1		0.1	
					6.0		0	0.1		0.1	
				I _{OL} = 6 mA	4.5		0.17	0.26		0.33	
				I _{OL} = 7.8 mA	6.0		0.18	0.26		0.33	
3-state output off-state current		I _{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } GND$		6.0			±0.5		±5.0	μA
Input leakage current		I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0		_	±0.1		±1.0	μA
Quiescent supply current		ICC	$V_{IN} = V_{CC}$ or GND		6.0			2.0		20.0	μA

Output capacitance

Power dissipation

capacitance

Unit

ns

ns

ns

ns

ns

ns

pF

pF

pF

_

Ta = -40 Ta = 25°C to 85°C Symbol Characteristics **Test Condition** C_{L(pF)} V_{CC} (V) Min Тур. Max Min Max 2.0 25 60 75 ____ ____ t_{TLH} 4.5 7 12 15 Output transition time 50 ____ ____ t_{THL} 6.0 6 10 13 ____ ____ 2.0 36 90 115 50 4.5 12 18 23 ____ ____ 6.0 10 15 20 ____ ____ t_{pLH} Propagation delay time tpHL 2.0 51 130 165 ____ ____ 150 4.5 17 26 33 _ ____ 6.0 _ 14 22 28 2.0 48 125 155 50 4.5 16 25 31 ____ ____ 6.0 14 21 26 t_{pZL} Output enable time $R_L = 1 \ k\Omega$ t_{pZH} 2.0 63 165 205 ____ ____ 150 4.5 21 33 41 6.0 18 28 35 2.0 32 125 155 ____ ____ t_{pLZ} Output disable time $R_L = 1 \ k\Omega$ 50 4.5 15 25 31 t_{pHZ} 6.0 14 21 26 ____ ____ Input capacitance C_{IN} 5 10 10

AC Electrical Characteristics (input $t_r = t_f = 6$ ns)

Note: C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

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31

Average operating current can be obtained by the equation: $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per gate)

(Note)

COUT

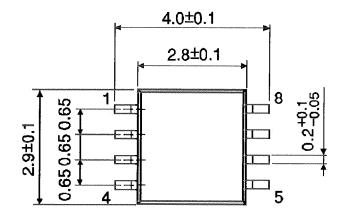
CPD

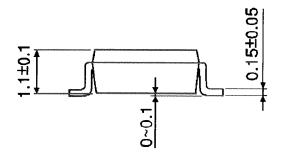
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Package Dimensions

SSOP8-P-0.65

Unit : mm





Weight: 0.02 g (typ.)

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