

TLP118

PDP (Plasma Display Panel)
 FA (Factory Automation)
 Interfaces of measuring and control instruments
 Operate at high ambient temperatures up to 125°C

The Toshiba TLP118 consists of an infrared emitting diodes and integrated high-gain, high-speed photodetectors.
 The TLP118 is housed in the SO6 package. The output stage is an open collector type.
 The photodetector has an internal Faraday shield that provides a guaranteed common-mode transient immunity of ± 15 kV/ μ s.

- Inverter logic type (Open collector output)
- Package: SO6 pin
- Guaranteed performance over: -40 to 125°C
- Power supply voltage: 4.5 to 5.5 V
- Input threshold current: $I_{FH} = 5.0$ mA (max)
- Propagation delay time t_{pHL}/t_{pLH} : 60 ns (max)
- Common-mode transient immunity: ± 15 kV/ μ s (min)
- Isolation voltage: 3750 Vrms (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved: EN 60747-5-5, EN 62368-1 (Note 1)
- CQC-approved: GB4943.1, GB8898 Thailand Factory



仅适用于海拔 2000m 以下地区安全使用

Note 1 : When VDE approved type is needed, please designate the **Option(V4)**.

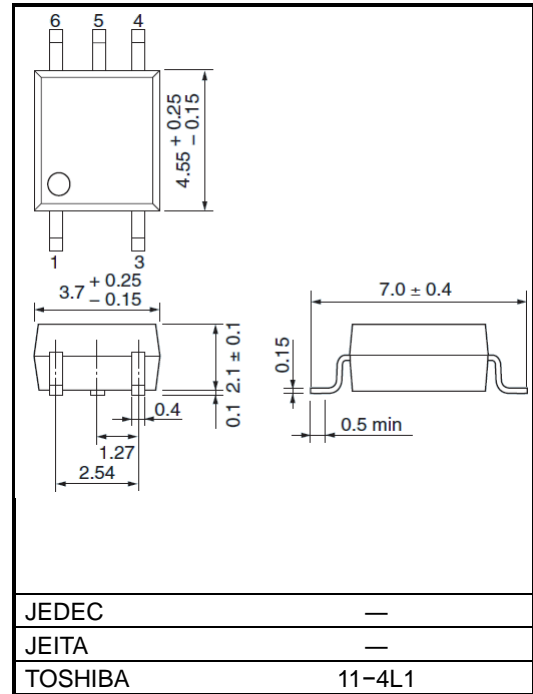
Truth Table

Input	LED	Output
H	ON	L
L	OFF	H

Construction Mechanical Ratings

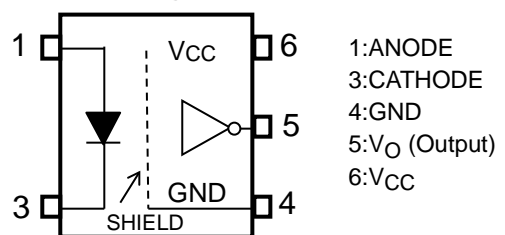
Creepage distance	5.0 mm (min)
Clearance distance	5.0 mm (min)
Insulation thickness	0.4 mm (min)

Unit: mm

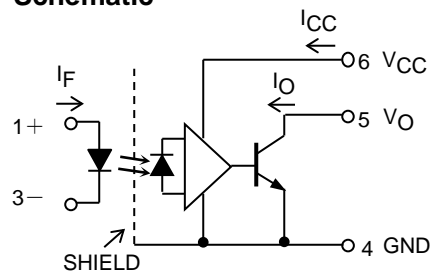


Weight: 0.08 g (typ.)

Pin Configuration (Top View)



Schematic



Start of commercial production
 2009-10

Absolute Maximum Ratings (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	I_F	25	mA
	Forward Current Derating (Ta ≥ 110°C)	$\Delta I_F / ^\circ\text{C}$	-0.67	mA/°C
	Pulse Forward Current (Note 1)	I_{FP}	50	mA
	Pulse Forward Current Derating (Ta ≥ 110°C)	$\Delta I_{FP} / ^\circ\text{C}$	-1.34	mA/°C
	Input Power Dissipation	PD	40	mW
	Input power Dissipation Derating (Ta > 85°C)	$\Delta PD / ^\circ\text{C}$	-1.0	mW/°C
	Reverse Voltage	V_R	5	V
DETECTOR	Output Current 1 (Ta ≤ 125°C)	I_O	25	mA
	Output Voltage	V_O	6	V
	Supply Voltage	V_{CC}	6	V
	Output Power Dissipation	P_O	80	mW
	Output Power Dissipation Derating (Ta ≥ 110°C)	$\Delta P_O / ^\circ\text{C}$	-2.0	mW/°C
Operating Temperature Range		T_{opr}	-40 to 125	°C
Storage Temperature Range		T_{stg}	-55 to 125	°C
Lead Soldering Temperature (10 s)		T_{sol}	260	°C
Isolation Voltage (AC, 60 s, R.H. ≤ 60 %) (Note 2)		BV_S	3750	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width ≤ 1 ms, duty = 50 %.

Note 2: This device is regarded as a two terminal device: pins 1 and 3 are shorted together, as are pins 4, 5 and 6.

Recommended Operating Conditions

CHARACTERISTIC	SYMBOL	MIN	TYP.	MAX	UNIT
Input Current , High Level	I_{FH}	7.5	—	15	mA
Input Voltage , Low Level	V_{FL}	0	—	0.8	V
Supply Voltage*	V_{CC}	4.5	—	5.5	V
Operating Temperature	T_{opr}	-40	—	125	°C

* This item denotes operating range, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics

(Unless otherwise specified, Ta=-40 to 125°C, VCC=4.5 to 5.5 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT
Input Forward Voltage	V _F	—	I _F = 10 mA, Ta = 25 °C	1.45	1.61	1.85	V
Temperature Coefficient of Forward Voltage	ΔV _F /ΔTa	—	I _F = 10 mA	—	-1.6	—	mV/°C
Input Reverse Current	I _R	—	V _R = 5 V, Ta = 25 °C	—	—	10	μA
Capacitance between Input terminals	C _T	—	V = 0 V, f = 1 MHz, Ta = 25 °C	—	60	—	pF
Logic High Output Current	I _{OH}	1	V _F = 0.8 V, V _O = 5.5 V	—	—	250	μA
			Ta = 25 °C	—	0.5	10	
Logic Low Output Voltage	V _{OL}	2	I _F = 10 mA, I _O = 13 mA (Sinking)	—	0.2	0.6	V
Logic Low Supply Current	I _{CCL}	3	I _F = 10 mA	—	1.5	5	mA
Logic High Supply Current	I _{CCH}	4	I _F = 0 mA	—	1.5	5	mA
"H Level Output to L Level Output" Input Current	I _{FHL}	—	I _O = 13 mA (Sinking), V _O < 0.6 V	—	1.0	5.0	mA

*All typical values are at Ta=25°C, VCC=5 V unless otherwise specified

Isolation Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	MIN	TYP.	MAX	UNIT
Capacitance input to output	C _S	V _S = 0 V, f = 1 MHz (Note 1)	—	0.8	—	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V (Note 1)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 60 s	3750	—	—	V _{rms}

Note 1: This device is regarded as a two terminal device: pins 1 and 3 are shorted together, as are pins 4, 5 and 6.

Switching Characteristics

(Unless otherwise specified, $T_a = -40$ to 125 °C, $V_{CC} = 4.5$ to 5.5 V)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	CONDITION	MIN	TYP.	MAX	UNIT	
Propagation delay time (H→L)	t_{pHL}	5	$I_F = 0 \rightarrow 7.5$ mA, $R_L = 350 \Omega$, $C_L = 15$ pF	—	30	60	ns	
Propagation delay time (L→H)	t_{pLH}		$I_F = 7.5 \rightarrow 0$ mA	(Note 1)	—	30	60	ns
Switching Time Dispersion between ON and OFF	$ t_{pHL} - t_{pLH} $		$I_F = 0 \leftrightarrow 7.5$ mA, $R_L = 350 \Omega$, $C_L = 15$ pF	(Note 1)	—	—	30	ns
Propagation Delay Skew (Note 2)	t_{psk}				-40	—	40	ns
Fall Time (90 – 10 %)	t_f		$I_F = 0 \rightarrow 7.5$ mA, $R_L = 350 \Omega$, $C_L = 15$ pF	(Note 1)	—	30	—	ns
Rise Time (10 – 90 %)	t_r		$I_F = 7.5 \rightarrow 0$ mA, $R_L = 350 \Omega$, $C_L = 15$ pF	(Note 1)	—	30	—	ns
Common Mode transient Immunity at High Level Output	CM_H	6	$V_{CM} = 1000$ V _{p-p} , $I_F = 0$ mA, $V_{CC} = 5$ V, $T_a = 25$ °C	15	—	—	kV/ μ s	
Common Mode transient Immunity at Low Level Output	CM_L		$V_{CM} = 1000$ V _{p-p} , $I_F = 10$ mA, $V_{CC} = 5$ V, $T_a = 25$ °C	-15	—	—	kV/ μ s	

*All typical values are at $T_a = 25$ °C

Note : A ceramic capacitor (0.1 μ F) should be connected from pin 6 (V_{CC}) to pin 4 (GND) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypass may impair the switching property.

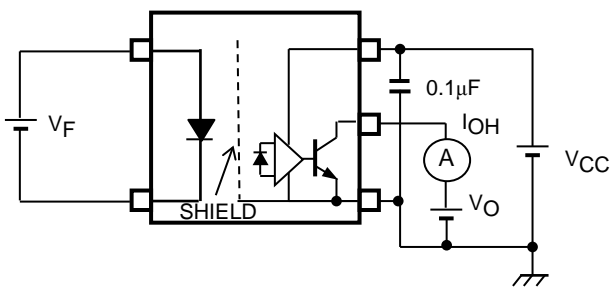
The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: $f = 5$ MHz, duty = 50 %, input current $t_r = t_f = 5$ ns,

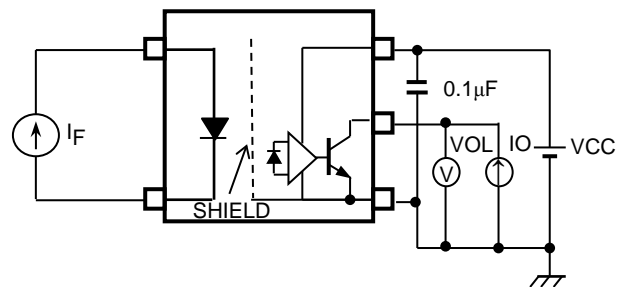
C_L is approximately 15pF which includes probe and Jig/stray wiring capacitance.

Note 2: Propagation delay skew is defined as the difference between the largest and smallest propagation delay times (i.e. t_{pHL} or t_{pLH}) of multiple samples. Evaluations of these samples are conducted under identical test conditions (supply voltage, input current, temperature, etc).

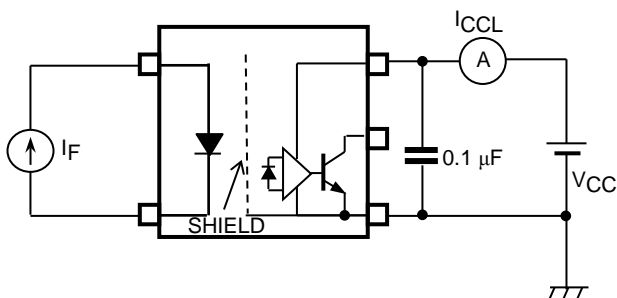
TEST CIRCUIT 1: I_{OH} Test Circuit



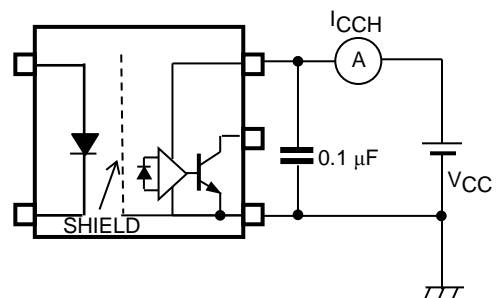
TEST CIRCUIT 2: V_{OL} Test Circuit



TEST CIRCUIT 3: I_{CCL} Test Circuit



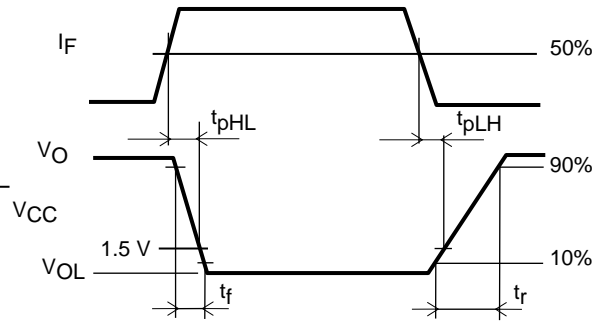
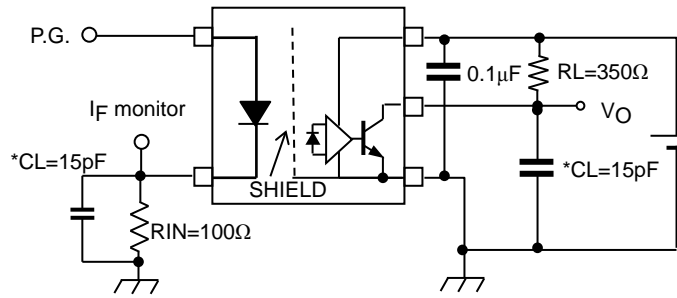
TEST CIRCUIT 4: I_{CCH} Test Circuit



TEST CIRCUIT 5: Switching Time Test Circuit

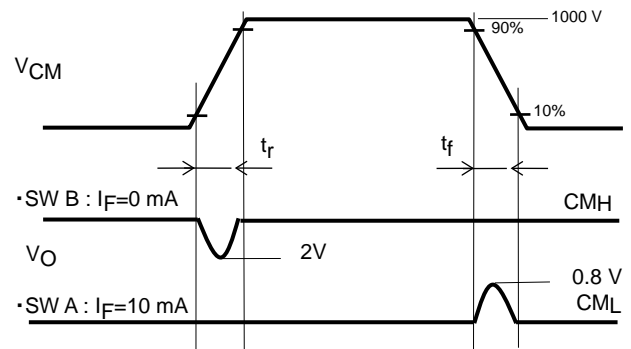
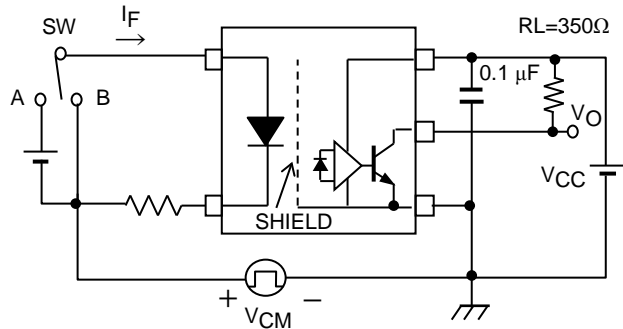
$I_F = 7.5\text{mA (P.G)}$

($f = 5\text{MHz}$, duty=50%, $t_r = t_f = \text{Less than } 5\text{ns}$)

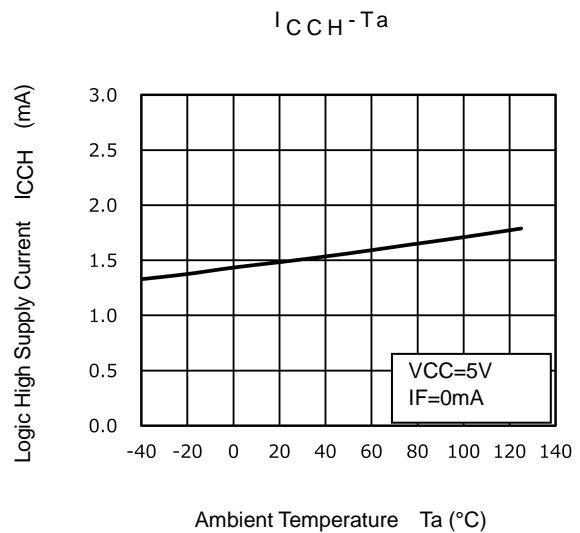
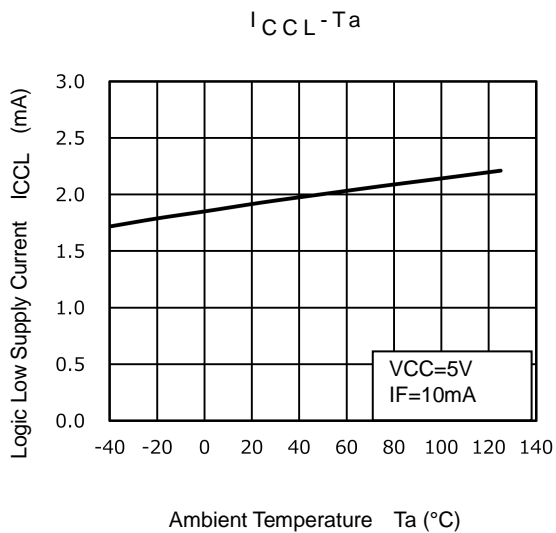
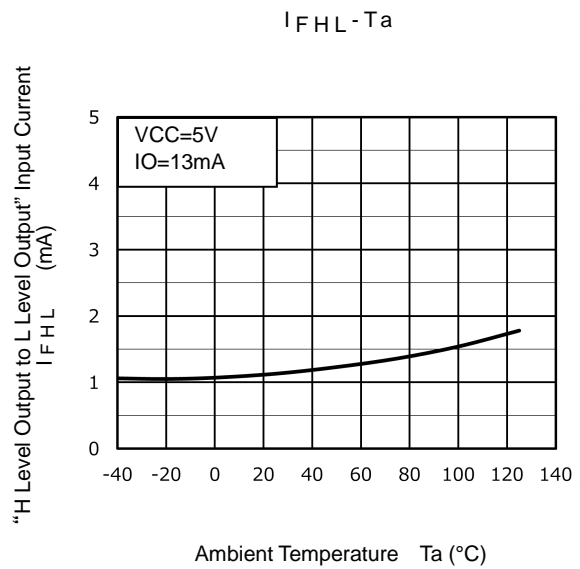
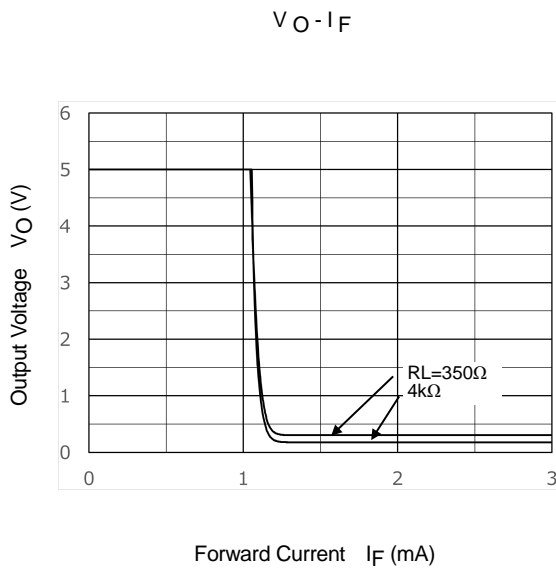
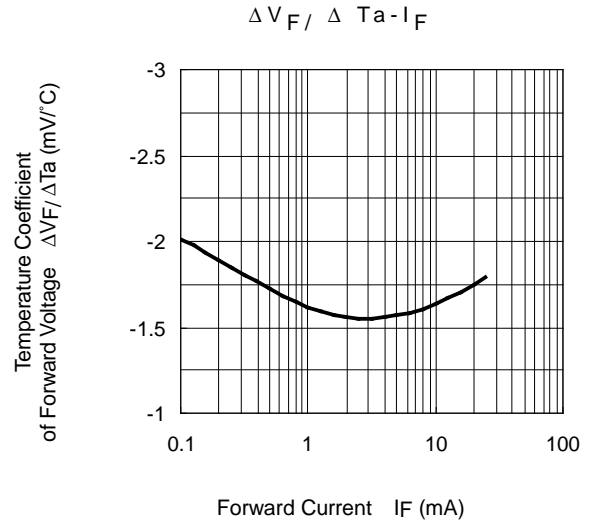
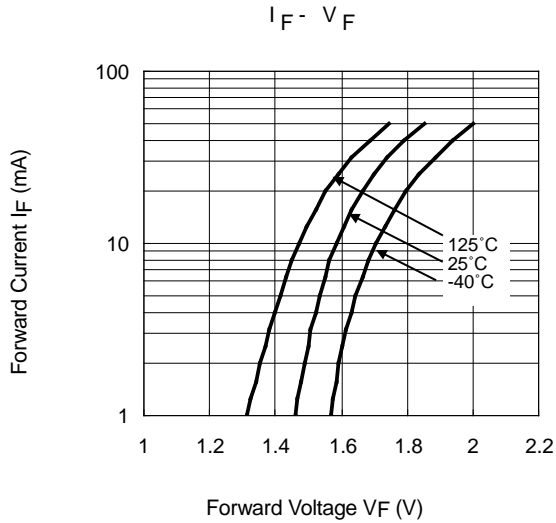


*CL: includes probe and stray capacitance.
P.G.: Pulse generator

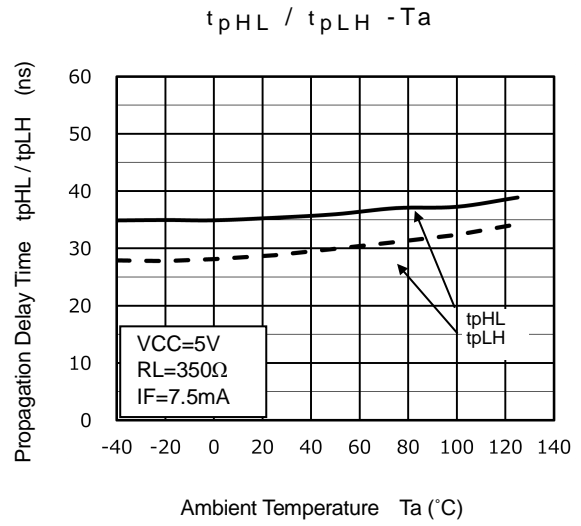
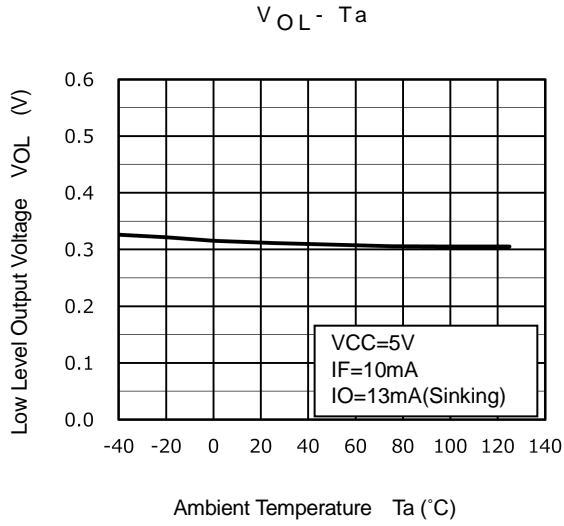
TEST CIRCUIT 6: Common-Mode Transient Immunity Test Circuit



$$CM_H = \frac{800(V)}{t_r(\mu s)} \quad CM_L = \frac{800(V)}{t_f(\mu s)}$$



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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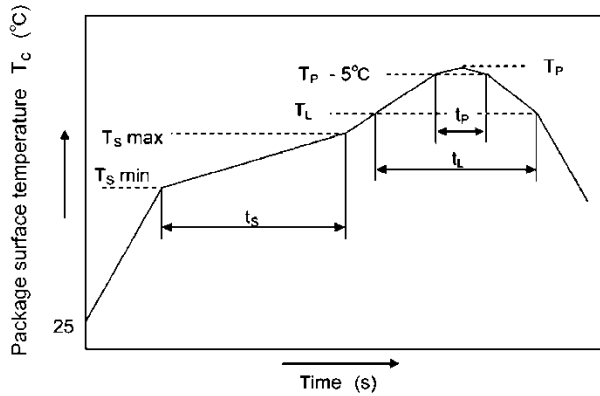
Soldering and Storage

(1) Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

1) When Using Soldering Reflow

An example of a temperature profile when lead(Pb)-free solder is used



	Symbol	Min	Max	Unit
Preheat temperature	T_s	150	200	°C
Preheat time	t_s	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	150	s
Peak temperature	T_P		260	°C
Time during which T_c is between ($T_P - 5$) and T_P	t_p		30	s
Ramp-down rate (T_P to T_L)			6	°C/s

- The soldering temperature profile is based on the package surface temperature (See the figure shown above.)
- Reflow soldering must be performed once or twice.
- The mounting should be completed with the interval from the first to the last mountings being 2 weeks.

2) When using soldering Flow

- Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
- Mounting condition of 260 °C within 10 seconds is recommended
- Flow soldering must be performed once.

3) When using soldering Iron

- Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
- Heating by soldering iron must be done only once per lead

(2) Precautions for General Storage

- 1) Do not store devices at any place where they will be exposed to moisture or direct sunlight.
- 2) When transportation or storage of devices, follow the cautions indicated on the carton box.
- 3) The storage area temperature should be kept within a temperature range of 5 °C to 35 °C, and relative humidity should be maintained at between 45% and 75%.
- 4) Do not store devices in the presence of harmful (especially corrosive) gases, or in dusty conditions.
- 5) Use storage areas where there is minimal temperature fluctuation. Because rapid temperature changes can cause condensation to occur on stored devices, resulting in lead oxidation or corrosion, as a result, the solderability of the leads will be degraded.
- 6) When repacking devices, use anti-static containers.
- 7) Do not apply any external force or load directly to devices while they are in storage.
- 8) If devices have been stored for more than two years, even though the above conditions have been followed, it is recommended that solderability of them should be tested before they are used.

Specification for Embossed–Tape Packing (TPL)(TPR) for SO6 Coupler

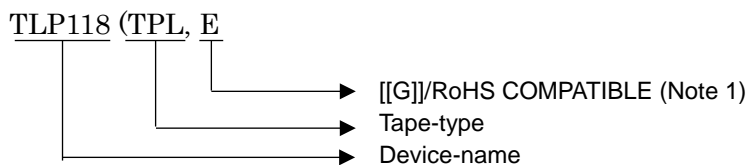
1. Applicable Package

Package	Product Type
SO6	Mini-flat coupler

2. Product Naming System

Type of package used for shipment is denoted by a symbol suffix after a product number. The method of classification is as below.

(Example)



Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility. RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

3. Tape Dimensions

3.1 Specification Classification Are as Shown in Table 1

Table 1 Tape Type Classification

Tape type	Classification	Quantity (pcs / reel)
TPL	L direction	3000
TPR	R direction	3000

3.2 Orientation of Device in Relation to Direction of Tape Movement

Device orientation in the recesses is as shown in Figure 1.

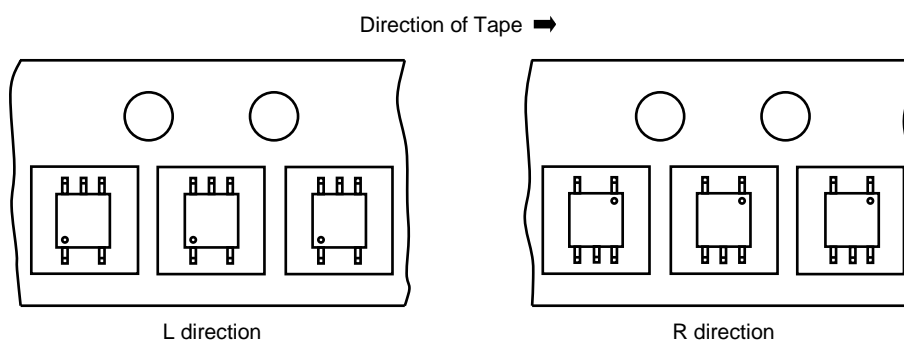


Figure 1 Device Orientation

3.3 Empty Device Recesses Are as Shown in Table 2.

Table 2 Empty Device Recesses

	Standard	Remarks
Occurrences of 2 or more successive empty device recesses	0 device	Within any given 40-mm section of tape, not including leader and trailer
Single empty device recesses	6 devices (max) per reel	Not including leader and trailer

3.4 Start and End of Tape

The start of the tape has 50 or more empty holes. The end of tape has 50 or more empty holes and two empty turns only for a cover tape.

3.5 Tape Specification

- (1) Tape material: Plastic (protection against electrostatics)
- (2) Dimensions: The tape dimensions are as shown in Figure 2 and Table 3.

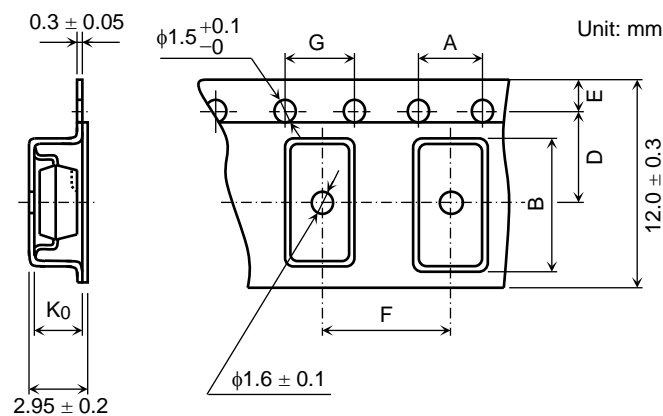


Figure 2 Tape Forms

Table 3 Tape Dimensions

Unit: mm
Unless otherwise specified: ±0.1

Symbol	Dimension	Remark
A	4.0	—
B	7.6	—
D	5.5	Center line of indented square hole and sprocket hole
E	1.75	Distance between tape edge and hole center
F	8.0	Cumulative error $\begin{matrix} +0.1 \\ -0.3 \end{matrix}$ (max) per 10 feed holes
G	4.0	Cumulative error $\begin{matrix} +0.1 \\ -0.3 \end{matrix}$ (max) per 10 feed holes
K0	2.6	Internal space

3.6 Reel

- (1) Material: Plastic
- (2) Dimensions: The reel dimensions are as shown in Figure 3 and Table 4.

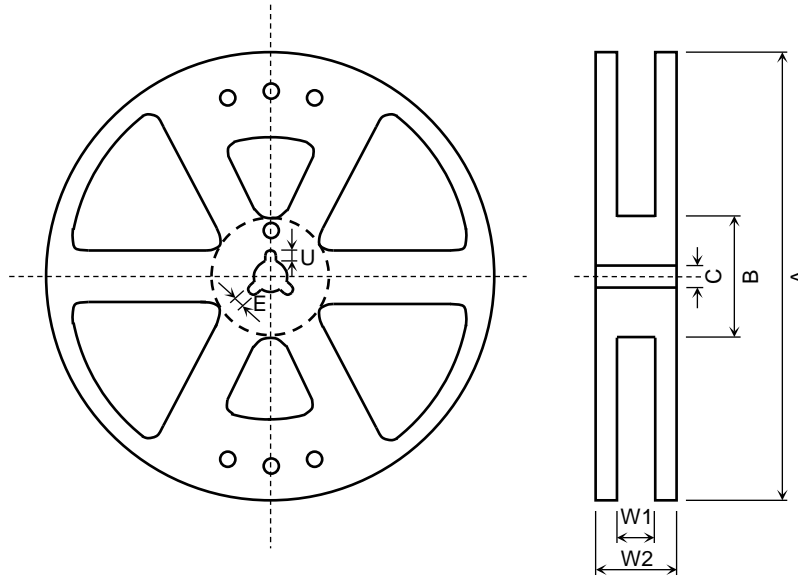


Figure 3 Reel Form

Table 4 Reel Dimensions

Unit: mm

Symbol	Dimension
A	$\Phi 330 \pm 2$
B	$\Phi 80 \pm 1$
C	$\Phi 13 \pm 0.5$
E	2.0 ± 0.5
U	4.0 ± 0.5
W1	13.5 ± 0.5
W2	17.5 ± 1.0

4. Packing

Packed in a shipping carton.

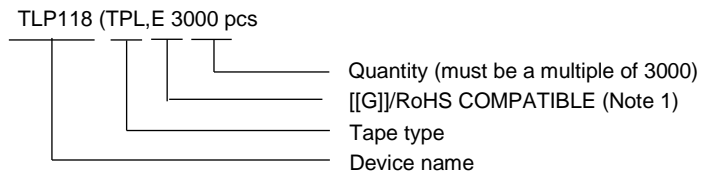
5. Label Indication

The carton bears a label indicating the product number, the symbol representing classification of standard, the quantity, the lot number and the Toshiba company name.

6. Ordering Method

When placing an order, please specify the product number, the tape type and the quantity as shown in the following example.

(Example)



Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility. RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

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