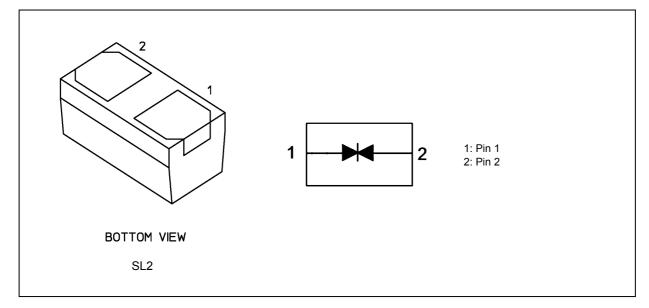
ESD Protection Diodes Silicon Epitaxial Planar

# DF2B7M2SL

#### 1. Applications

- ESD Protection
- Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

#### 2. Packaging and Internal Circuit



#### 3. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^{\circ}$ C)

Characteristics	Symbol	Note	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V <sub>ESD</sub>	(Note 1)	±12	kV
Electrostatic discharge voltage(IEC61000-4-2)(Air)			±15	kV
Peak pulse power	P <sub>PK</sub>		40	W
Peak pulse current	I <sub>PP</sub>	(Note 2)	2	А
Junction temperature	Tj		150	°C
Storage temperature	T <sub>stg</sub>		-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

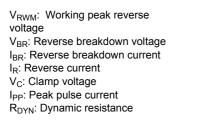
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: According to IEC61000-4-2.

Note 2: According to IEC61000-4-5.

Start of commercial production 2014-10 2015-04-02 Rev.4.0

### 4. Electrical Characteristics (Unless otherwise specified, $T_a = 25^{\circ}C$ )



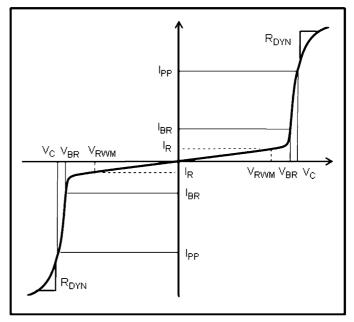


Fig. 4.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V <sub>RWM</sub>		—	_		5	V
Reverse breakdown voltage	V <sub>BR</sub>		I <sub>BR</sub> = 1 mA	6	_	11	V
Reverse current	I <sub>R</sub>		V <sub>RWM</sub> = 5 V	_	5	50	nA
Clamp voltage	V <sub>C</sub>	(Note 1), (Note 3)	I <sub>PP</sub> = 1 A	_	13	_	V
			I <sub>PP</sub> = 2 A	_	15	20	V
Dynamic resistance	R <sub>DYN</sub>	(Note 2)	—	_	1	_	Ω
Total capacitance	Ct	(Note 3)	V <sub>R</sub> = 0 V, f = 1 MHz	—	0.2	0.4	pF

Note 1: Based on IEC61000-4-5 8/20  $\mu s$  pulse.

Note 2: TLP parameter: Z0 = 50  $\Omega$ , tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns,

extraction of dynamic resistance using a least-squares fit of TLP characteristics at  $I_{PP}$  between 8 A to 16 A. Note 3: Guaranteed by design.

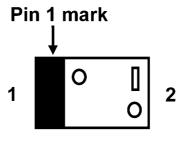


Fig. 5.1 Marking

6. Land Pattern Dimensions (for reference only)

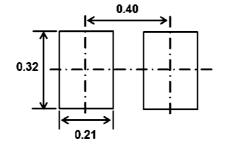
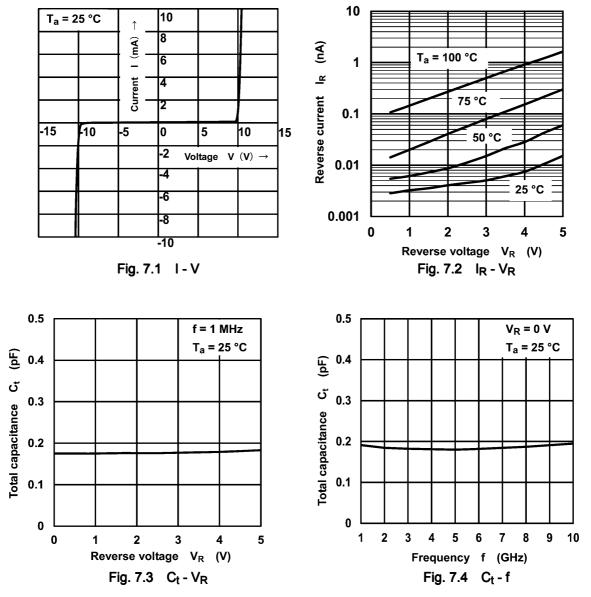


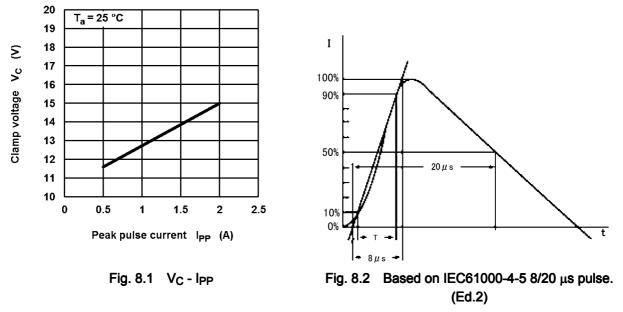
Fig. 6.1 Land Pattern Dimensions (Unit: mm)

### 7. Characteristics Curves (Note)



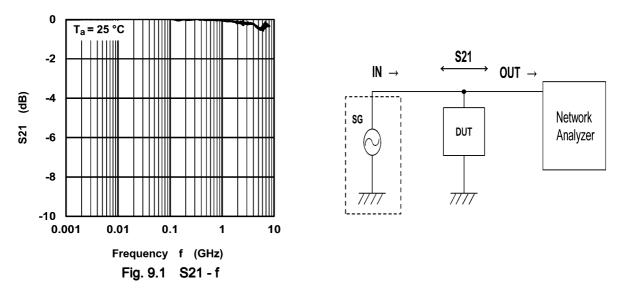
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

8. Clamp Voltage V<sub>C</sub> - Peak Pulse Current (IPP) (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

#### 9. Insertion Loss (S21) (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

### 10. ESD Clamp Waveform (Note)

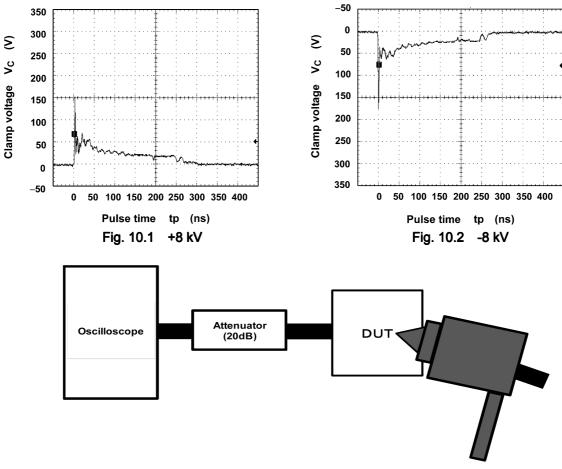
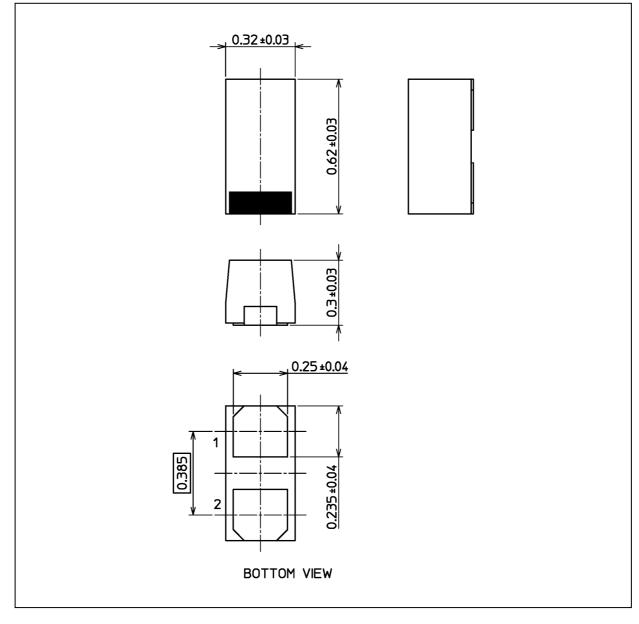


Fig. 10.3 IEC61000-4-2 (Contact)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

### Package Dimensions

Unit: mm



#### Weight: 0.2 mg (typ.)

Package Name(s)		
TOSHIBA: 1-1AL1A		
Nickname: SL2		

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