

TK28V65W5

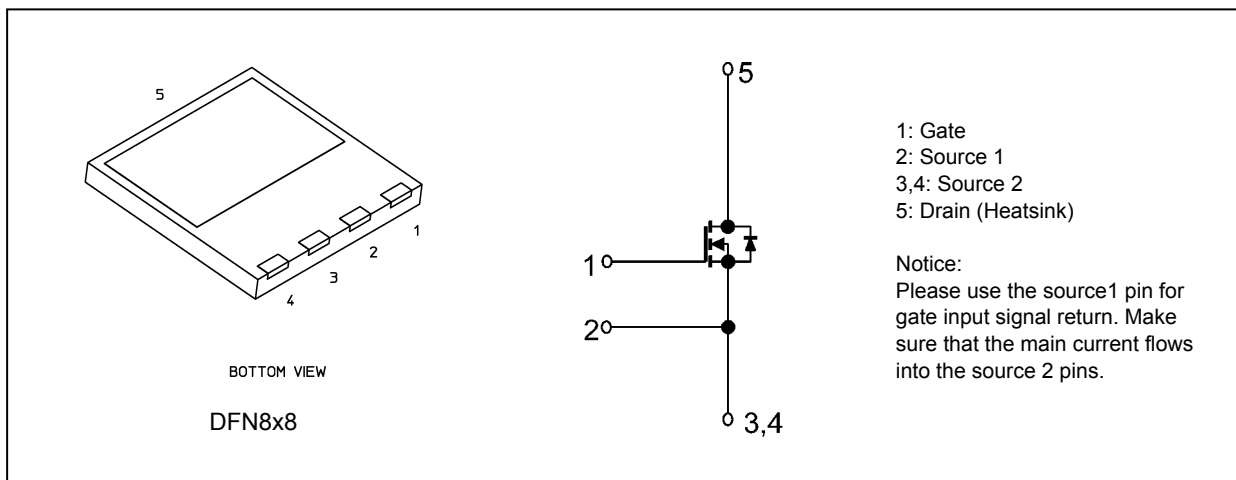
1. Applications

- Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 0.115 \Omega$ (typ.)
by using Super Junction Structure: DTMOS
- (2) Easy to control Gate switching
- (3) Enhancement mode: $V_{th} = 3$ to 4.5 V ($V_{DS} = 10$ V, $I_D = 1.6$ mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25 \text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	650	V
Gate-source voltage	V_{GSS}	± 30	
Drain current (DC)	I_D	27.6	A
Drain current (pulsed)	I_{DP}	110	
Power dissipation	P_D	240	W
Single-pulse avalanche energy	E_{AS}	347	mJ
Single-pulse avalanche current	I_{AS}	7	A
Reverse drain current (DC)	I_{DR}	27.6	
Reverse drain current (pulsed)	I_{DRP}	110	
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production

2016-09

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	0.520	°C/W

Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: $V_{DD} = 90\text{ V}$, $T_{ch} = 25\text{ °C}$ (initial), $L = 12.56\text{ mH}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 7\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	—	—	100	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	650	—	—	V
Gate threshold voltage	V_{th}	$V_{DS} = 10\text{ V}, I_D = 1.6\text{ mA}$	3	—	4.5	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 13.8\text{ A}$	—	0.115	0.14	Ω

6.2. Dynamic Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = 300\text{ V}, V_{GS} = 0\text{ V}, f = 100\text{ kHz}$	—	3000	—	μF
Reverse transfer capacitance	C_{rss}		—	8	—	
Output capacitance	C_{oss}		—	70	—	
Effective output capacitance	$C_{o(er)}$	$V_{DS} = 0\text{ to }400\text{ V}, V_{GS} = 0\text{ V}$	—	110	—	
Gate resistance	r_g	$V_{DS} = \text{OPEN}, f = 1\text{ MHz}$	—	2.0	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	50	—	ns
Switching time (turn-on time)	t_{on}		—	100	—	
Switching time (fall time)	t_f		—	7	—	
Switching time (turn-off time)	t_{off}		—	130	—	
MOSFET dv/dt ruggedness	dv/dt	$V_{DD} = 0\text{ to }400\text{ V}, I_D = 13.8\text{ A}$	50	—	—	V/ns

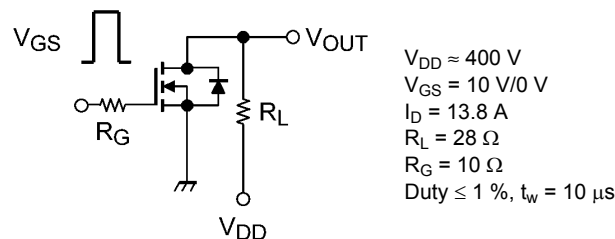


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx 400\text{ V}, V_{GS} = 10\text{ V}, I_D = 27.6\text{ A}$	—	90	—	nC
Gate-source charge 1	Q_{gs1}		—	25	—	
Gate-drain charge	Q_{gd}		—	45	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Diode forward voltage	V_{DSF}	$I_{DR} = 27.6\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.7	V	
Reverse recovery time	t_{rr}	$I_{DR} = 13.8\text{ A}, V_{GS} = 0\text{ V}$ $-dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	115	184	ns	
Reverse recovery charge	Q_{rr}		—	0.69	—		μC
Peak reverse recovery current	I_{rr}		—	12.2	—		A
Diode dv/dt ruggedness	dv/dt	$I_{DR} = 13.8\text{ A}, V_{GS} = 0\text{ V}, V_{DD} = 400\text{ V}$	50	—	—	V/ns	

7. Marking

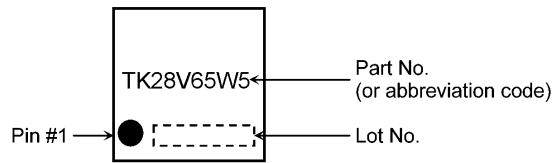


Fig. 7.1 Marking

8. Characteristics Curves (Note)

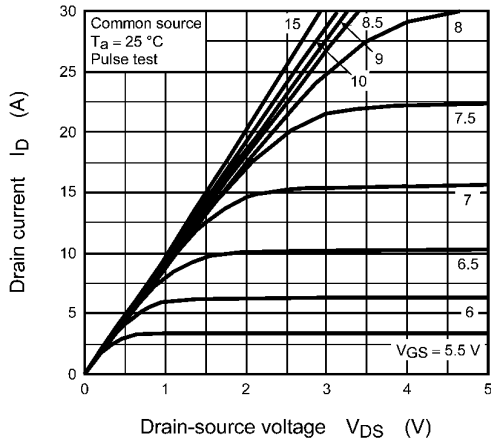


Fig. 8.1 $I_D - V_{DS}$

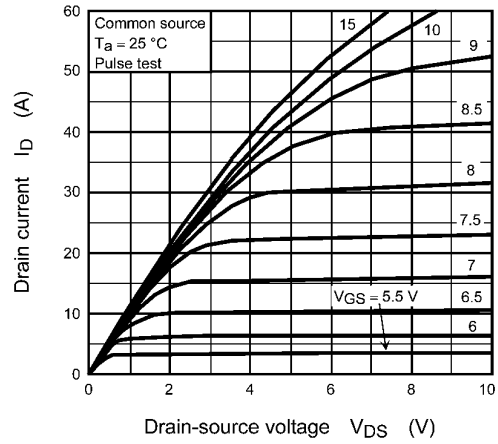


Fig. 8.2 $I_D - V_{DS}$

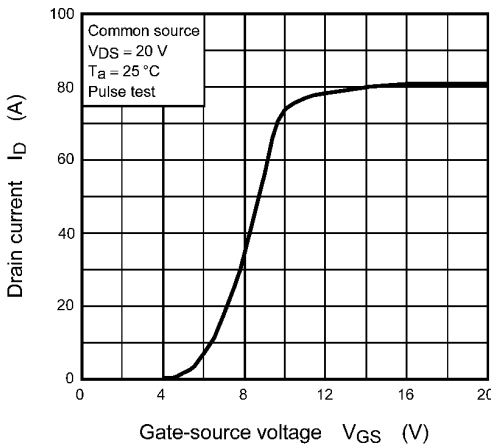


Fig. 8.3 $I_D - V_{GS}$

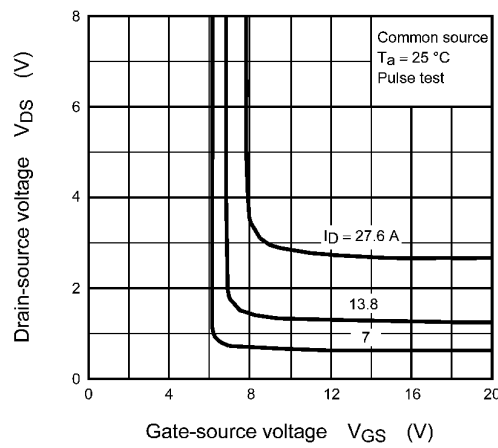


Fig. 8.4 $V_{DS} - V_{GS}$

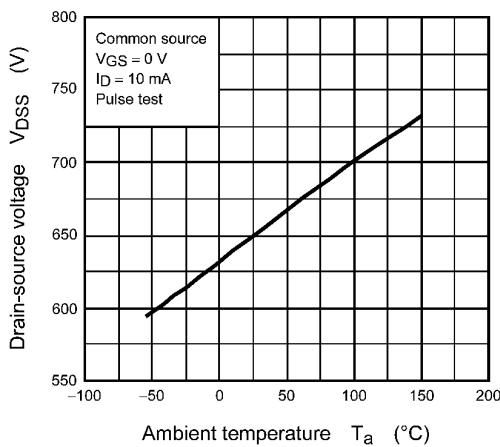


Fig. 8.5 $V_{DSS} - T_a$

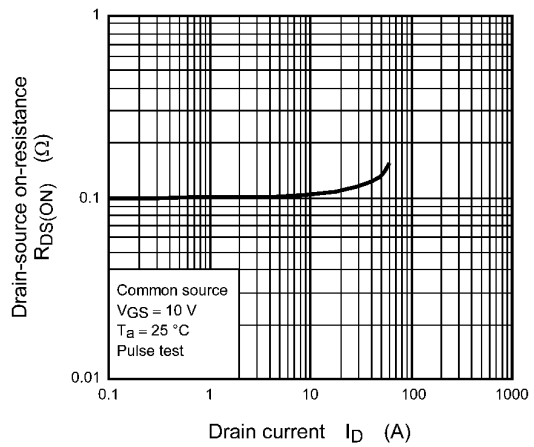


Fig. 8.6 $R_{DS(ON)} - I_D$

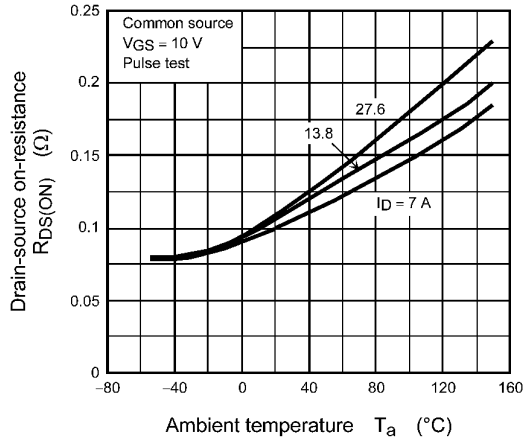


Fig. 8.7 $R_{DS(ON)} - T_a$

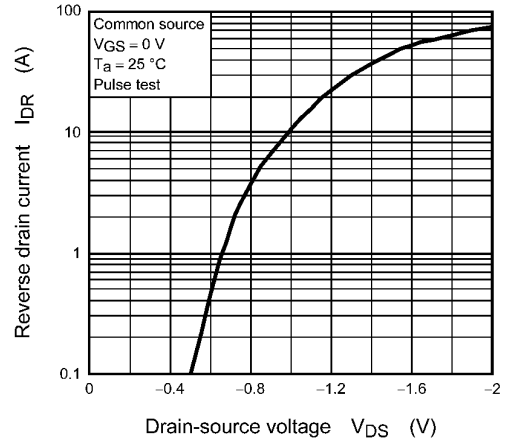


Fig. 8.8 $I_{DR} - V_{DS}$

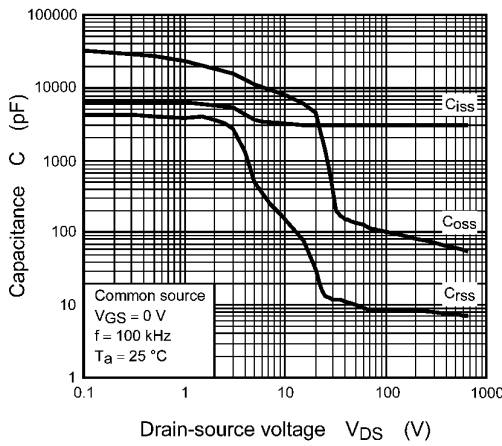


Fig. 8.9 $C - V_{DS}$

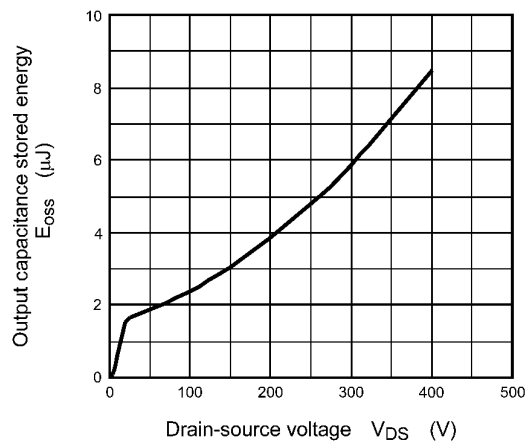


Fig. 8.10 $E_{oss} - V_{DS}$

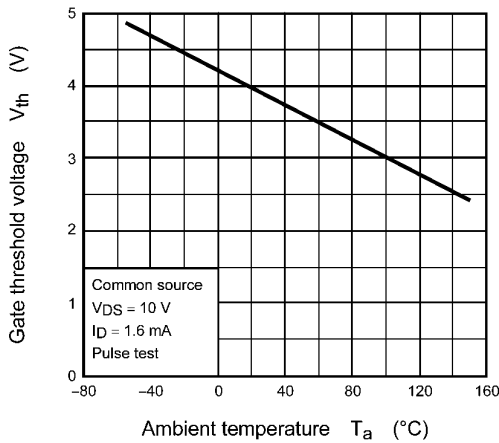


Fig. 8.11 $V_{th} - T_a$

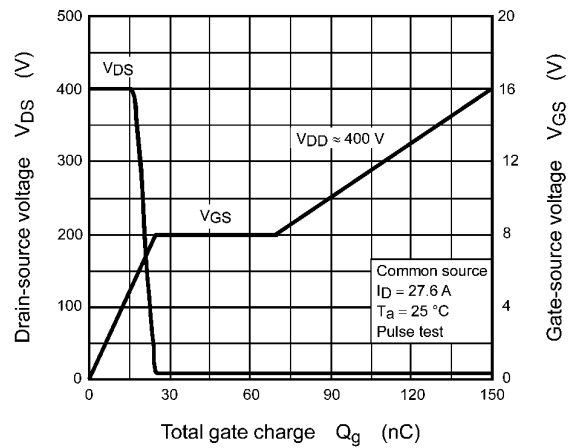


Fig. 8.12 Dynamic Input/Output Characteristics

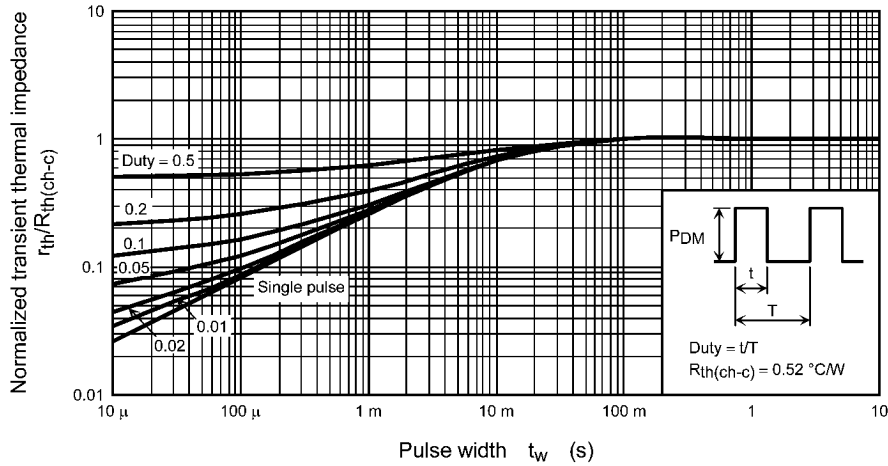


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

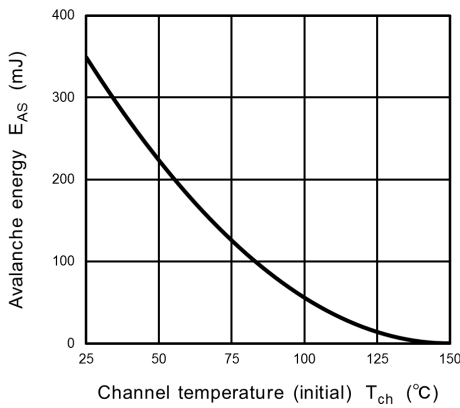


Fig. 8.14 $E_{AS} - T_{ch}$
(Guaranteed Maximum)

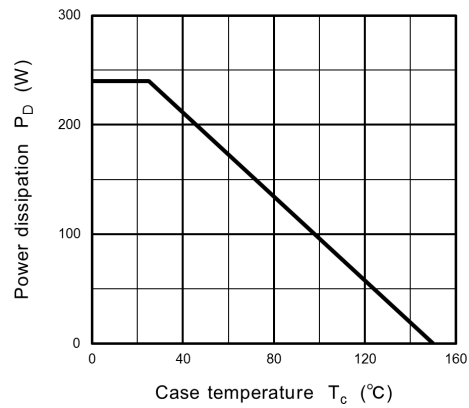


Fig. 8.15 $P_D - T_c$
(Guaranteed Maximum)

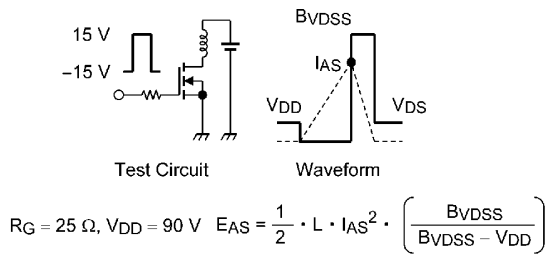


Fig. 8.16 Test Circuit/Waveform

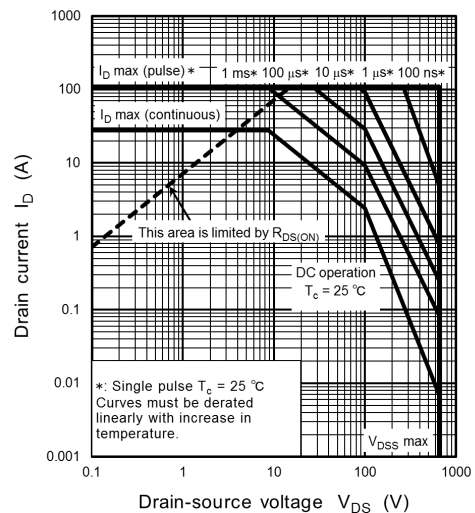


Fig. 8.17 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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