TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7W241FU

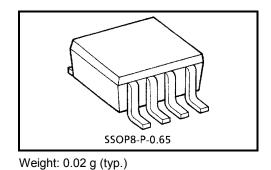
Non-Inverted, 3-State Outputs

The TC7W241FU is a high speed C²MOS Dual Bus Buffers fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the C^2MOS low power dissipation.

It is a non-inverting 3-state buffer has one active-high and one active-low output enable.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Features

- High speed: $t_{pd} = 10 \text{ ns}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 2 \mu A (max)$ at $Ta = 25^{\circ}C$
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 6 \text{ mA} (min)$
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V

Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7	V
DC input voltage	V _{IN}	-0.5 to V_{CC} + 0.5	V
DC output voltage	V _{OUT}	-0.5 to V_{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	IOK	±20	mA
DC output current	IOUT	±35	mA
DC V _{CC} /ground current	ICC	±37.5	mA
Power dissipation	PD	300	mW
Storage temperature range	T _{stg}	-65 to 150	°C
Lead temperature (10 s)	ΤL	260	°C

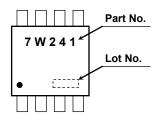
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

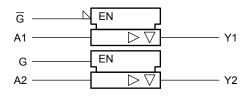
Start of commercial production 1993-04

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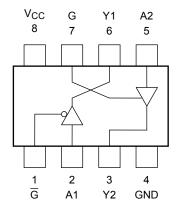
Marking



Logic Diagram



Pin Configuration (top view)



Truth Table

	Output		
IJ	G	А	Y
L	Н	L	L
L	Н	Н	Н
н	L	х	Z

X: Don't care Z: High impedance

Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2 to 6	V
Input voltage	V _{IN}	0 to V _{CC}	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature range	T _{opr}	-40 to 85	°C
		0 to 1000 (V _{CC} = 2.0 V)	
Input rise and fall time	t _r , t _f	0 to 500 (V _{CC} = 4.5 V)	ns
		0 to 400 (V _{CC} = 6.0 V)	

Electrical Characteristics

DC Electrical Characteristics

Characteristics		Symbol	Symbol Test Condition			Ta = 25°C		Ta = -40 to 85°C		Unit	
0.10.000			$V_{CC}\left(V\right)$	Min	Тур.	Max	Min	Max	Offic		
		VIH	_		2.0	1.5		—	1.5		-
	High level				4.5	3.15		_	3.15	_	
Input voltage					6.0	4.2	_	_	4.2	—	V
Input voltage			_		2.0			0.5		0.5	v
	Low level	VIL			4.5			1.35		1.35	
					6.0			1.8		1.8	
	High level		VIN = VIH or VIL	I _{OH} = -20 μA	2.0	1.9	2.0		1.9		- V
		V _{OH}			4.5	4.4	4.5		4.4		
Output					6.0	5.9	6.0	_	5.9	—	
				I _{OH} = -6 mA	4.5	4.18	4.31		4.13	—	
				I _{OH} = -7.8 mA	6.0	5.68	5.80		5.63		
voltage	Low level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 μA	2.0		0	0.1		0.1	
					4.5		0	0.1		0.1	
					6.0	_	0	0.1	_	0.1	
				I _{OL} = 6 mA	4.5	_	0.17	0.26	_	0.33	
				I _{OL} = 7.8 mA	6.0		0.18	0.26		0.33	
3-state output off-state current		I _{OZ}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or } GND$		6.0		_	±0.5	_	±5.0	μA
Input leakage of	current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0			±0.1		±1.0	μA
Quiescent supply current I _{CC} V _{IN} = V _{CC} or GND		6.0			2.0		20.0	μA			

AC Electrical Characteristics (input $t_r = t_f = 6 \text{ ns}$)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
	Cymbol		C _{L(pF)}	$V_{CC}\left(V\right)$	Min	Тур.	Max	Min	Max	Onit
Output transition time	tт∟н tтн∟	_	50	2.0		25	60		75	ns
				4.5		7	12	_	15	
				6.0	_	6	10		13	
		_		2.0	_	36	90		115	
			50	4.5	_	12	18		23	ns
Propagation delay time	t _{pLH}			6.0	_	10	15		20	
Tropagation delay time	t _{pHL}			2.0	_	51	130		165	ns
			150	4.5	_	17	26		33	
				6.0	_	14	22		28	
	t _{pZL}	R _L = 1 kΩ	50	2.0		48	125	_	155	ns
				4.5	_	16	25		31	
Output enable time				6.0	_	14	21		26	
	t _{pZH}		150	2.0	_	63	165		205	
				4.5		21	33	_	41	
				6.0		18	28	_	35	
Output disable time	t _{pLZ} t _{pHZ}	$R_L = 1 \ k\Omega$	50	2.0		32	125	_	155	ns
				4.5	_	15	25		31	
				6.0	_	14	21		26	
Input capacitance	C _{IN}		_	_		5	10		10	pF
Output capacitance	C _{OUT}		_	_		10			_	pF
Power dissipation capacitance	C _{PD}	(Note)	_	_	_	33	_	_		pF

Note: C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

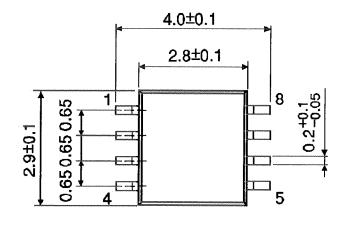
Average operating current can be obtained by the equation: $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per gate)

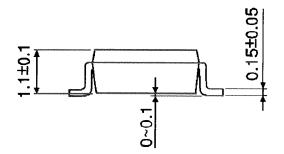
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Package Dimensions

SSOP8-P-0.65

Unit : mm





Weight: 0.02 g (typ.)

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