Photocouplers　Infrared LED & Photo IC

TLP5751

1. Applications

- Induction Cooktop and Home Appliances
- Industrial Inverters
- Air Conditioner Inverters
- MOSFET Gate Drivers
- IGBT Gate Drivers

2. General

The TLP5751 consists of an infrared LED and integrated high-gain, high-speed photodetector and is house in the 6-pin SO6L package.

The TLP5751 is 50 % smaller than the 8-pin DIP package and meets the reinforced insulation class requirements of international safety standards.

Therefore the mounting area can be reduced in equipment requiring the safety standard certification.

The TLP5751 has an internal faraday shield that provides a guaranteed common-mode transient immunity of ±35 kV/μs.

In particular, the TLP5751 has rail to rail output, and this enables stable operation and better switching performance in system.

3. Features

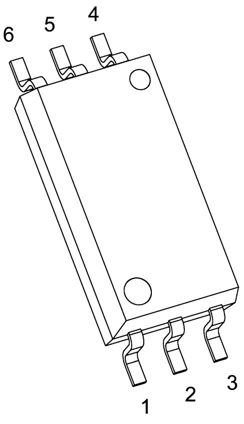
(1) Buffer logic type (totem pole output)
(2) Output peak current: ± 1.0 A (max)
(3) Operating temperature: -40 to 110 ℃
(4) Supply current: 3.0 mA (max)
(5) Supply voltage: 15 to 30 V
(6) Threshold input current: 4 mA (max)
(7) Propagation delay time: 150 ns (max)
(8) Common-mode transient immunity: ±35 kV/μs (min)
(9) Isolation voltage: 5000 Vrms (min)
(10) Safety standards
    UL-recognized: UL 1577, File No.E67349
    cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
    VDE-approved: EN 60747-5-5, EN 62368-1 **(Note 1)**
    CQC-approved: GB4943.1, GB8898 Japan and Thailand Factory

Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

Start of commercial production
2014-06

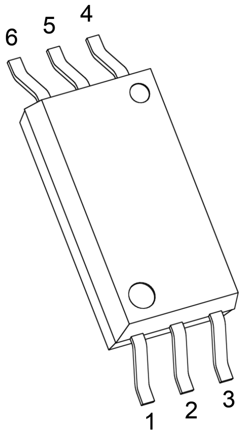
4. Packaging (Note)

TLP5751



11-4N1A

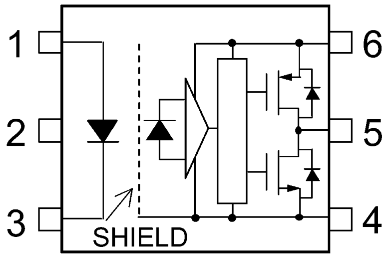
TLP5751(LF4)



11-4N101A

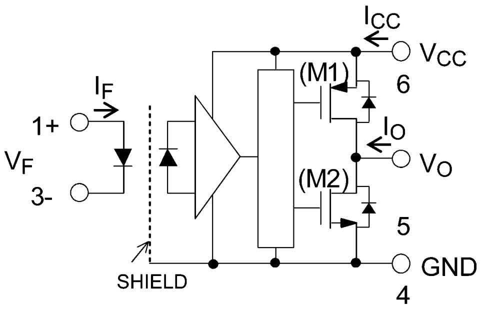
Note: Lead forming option: (LF4)

5. Pin Assignment



1: Anode
2: N.C.
3: Cathode
4: GND
5: V_O (Output)
6: V_{CC}

6. Internal Circuit (Note)



Note: A 1-µF bypass capacitor must be connected between pin 6 and pin 4.

7. Principle of Operation

7.1. Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

7.2. Mechanical Parameters

Characteristics	Size	Unit
Height	2.3 (max)	mm
Creepage distances	8.0 (min)	
Clearance distances	8.0 (min)	
Internal isolation thickness	0.4 (min)	

8. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

	Characteristics		Symbol	Note	Rating	Unit
LED	Input forward current		I_F		20	mA
	Input forward current derating	($T_a \geq$ 105 °C)	$\Delta I_F/\Delta T_a$		-1	mA/°C
	Peak transient input forward current		I_{FPT}	(Note 1)	1	A
	Peak transient input forward current derating	($T_a \geq$ 85 °C)	$\Delta I_{FPT}/\Delta T_a$		-25	mA/°C
	Input reverse voltage		V_R		5	V
	Input power dissipation		P_D		40	mW
	Input power dissipation derating	($T_a \geq$ 85 °C)	$\Delta P_D/\Delta T_a$		-1.0	mW/°C
	Junction temperature		T_j		125	°C
Detector	Peak high-level output current	(T_a = -40 to 110 °C)	I_{OPH}	(Note 2)	-1.0	A
	Peak low-level output current	(T_a = -40 to 110 °C)	I_{OPL}	(Note 2)	+1.0	
	Output voltage		V_O		35	V
	Supply voltage		V_{CC}		35	
	Output power dissipation		P_O		450	mW
	Output power dissipation derating	($T_a \geq$ 85 °C)	$\Delta P_O/\Delta T_a$		-4.5	mW/°C
	Junction temperature		T_j		125	°C
Common	Operating temperature		T_{opr}		-40 to 110	
	Storage temperature		T_{stg}		-55 to 125	
	Lead soldering temperature	(10 s)	T_{sol}	(Note 3)	260	
	Isolation voltage	AC, 60 s, R.H. ≤ 60 %	BV_S	(Note 4)	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width (PW) ≤ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width ≤ 2 μs, f ≤ 15 kHz

Note 3: ≥ 2 mm below seating plane.

Note 4: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

9. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	$I_{F(ON)}$	(Note 1)	6	—	15	mA
Input off-state voltage	$V_{F(OFF)}$		0	—	0.8	V
Supply voltage	V_{CC}	(Note 2)	15	—	30	
Peak high-level output current	I_{OPH}		—	—	-1.0	A
Peak low-level output current	I_{OPL}		—	—	+1.0	
Operating frequency	f	(Note 3)	—	—	50	kHz

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (1 µF) should be connected between pin 6 (V_{CC}) and pin 4 (GND) to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 0.5 µs.

Note 2: Denotes the operating range, not the recommended operating condition.

Note 3: Exponential waveform. $I_{OPH} \geq -1.0$ A ($\leq$ 90 ns), $I_{OPL} \leq 1.0$ A ($\leq$ 90 ns), T_a = 110 °C

10. Electrical Characteristics (Note) (Unless otherwise specified, T_a = -40 to 110 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F			I_F = 10 mA, T_a = 25 °C	1.45	1.55	1.70	V
Input forward voltage temperature coefficient	$\Delta V_F/\Delta T_a$			I_F = 10 mA	—	-1.8	—	mV/°C
Input reverse current	I_R			V_R = 5 V, T_a = 25 °C	—	—	10	µA
Input capacitance	C_t			V = 0 V, f = 1 MHz, T_a = 25 °C	—	60	—	pF
Peak high-level output current	I_{OPH}	(Note 1)	Fig. 13.1.1	I_F = 5 mA, V_{CC} = 30 V, $V_{6\text{-}5}$ = -3.5 V	—	—	-0.5	A
				I_F = 5 mA, V_{CC} = 15 V, $V_{6\text{-}5}$ = -7 V	—	—	-1.0	
Peak low-level output current	I_{OPL}	(Note 1)	Fig. 13.1.2	I_F = 0 mA, V_{CC} = 30 V, $V_{5\text{-}4}$ = 2.5 V	0.5	—	—	
				I_F = 0 mA, V_{CC} = 15 V, $V_{5\text{-}4}$ = 7 V	1.0	—	—	
High-level output voltage	V_{OH}		Fig. 13.1.3	I_F = 4 mA, V_{CC} = 15 V, I_O = -100 mA	14.7	14.9	—	V
Low-level output voltage	V_{OL}		Fig. 13.1.4	V_F = 0.8 V, V_{CC} = 15 V, I_O = 100 mA	—	0.07	0.2	
High-level supply current	I_{CCH}		Fig. 13.1.5	I_F = 10 mA, V_{CC} = 30 V, V_O = Open	—	1.8	3.0	mA
Low-level supply current	I_{CCL}		Fig. 13.1.6	I_F = 0 mA, V_{CC} = 30 V, V_O = Open	—	1.7	3.0	
Threshold input current (L/H)	I_{FLH}			V_{CC} = 15 V, V_O > 1 V	—	1.4	4	
Threshold input voltage (H/L)	V_{FHL}			V_{CC} = 15 V, V_O < 1 V	0.8	—	—	V
Supply voltage	V_{CC}			—	15	—	30	
UVLO threshold voltage	V_{UVLO+}			I_F = 5 mA, V_O > 2.5 V	12.1	12.7	13.5	
	V_{UVLO-}			I_F = 5 mA, V_O < 2.5 V	11.1	11.7	12.4	
UVLO hysteresis	$UVLO_{HYS}$			—	—	1.0	—	

Note: All typical values are at T_a = 25 °C.

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors. Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1: I_O application time $\leq$ 50 µs; single pulse.

11. Isolation Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	V_S = 0 V, f = 1 MHz	—	1.0	—	pF
Isolation resistance	R_S	(Note 1)	V_S = 500 V, R.H. ≤ 60 %	10^{12}	10^{14}	—	Ω
Isolation voltage	BV_S	(Note 1)	AC, 60 s	5000	—	—	Vrms

Note 1: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

12. Switching Characteristics (Note) (Unless otherwise specified, T_a = -40 to 110 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 13.1.7	$I_F = 0 \rightarrow 10$ mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	50	—	150	ns
Propagation delay time (H/L)	t_{pHL}			$I_F = 10 \rightarrow 0$ mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	50	—	150	
Rise time	t_r	(Note 1)		$I_F = 0 \rightarrow 10$ mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	—	15	—	
Fall time	t_f	(Note 1)		$I_F = 10 \rightarrow 0$ mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	—	8	—	
Pulse width distortion	$\lvert t_{pHL}-t_{pLH}\rvert$	(Note 1)		$I_F = 0 \longleftrightarrow 10$ mA, V_{CC} = 30 V, R_g = 10 Ω, C_g = 25 nF	—	—	50	
Propagation delay skew (device to device)	t_{psk}	(Note 1), (Note 2)			-80	—	80	
High-level common-mode transient immunity	CM_H	(Note 3)	Fig. 13.1.8	V_{CM} = 1000 $V_{p\text{-}p}$, I_F = 5 mA, V_{CC} = 30 V, T_a = 25 °C, $V_{O(min)}$ = 26 V	±35	±40	—	kV/µs
Low-level common-mode transient immunity	CM_L	(Note 4)		V_{CM} = 1000 $V_{p\text{-}p}$, I_F = 0 mA, V_{CC} = 30 V, T_a = 25 °C, $V_{O(max)}$ = 1 V	±35	±40	—	

Note: All typical values are at T_a = 25 °C.

Note 1: Input signal (f = 25 kHz, duty = 50 %, t_r = t_f = 5 ns or less).
C_L is less than 15 pF which includes probe and stray wiring capacitance.

Note 2: The propagation delay skew, t_{psk}, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

Note 3: CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 26 V).

Note 4: CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 1 V).

13. Test Circuits and Characteristics Curves

13.1. Test Circuits

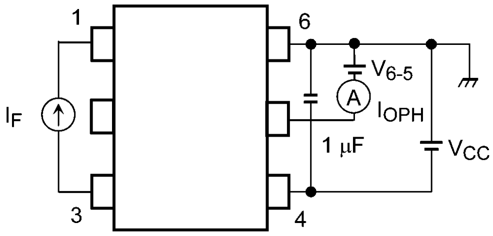


Fig. 13.1.1 I_{OPH} Test Circuit

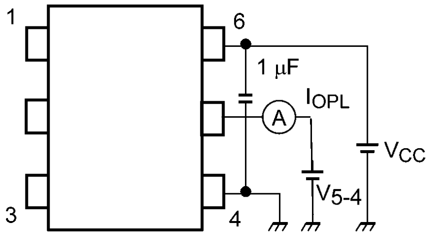
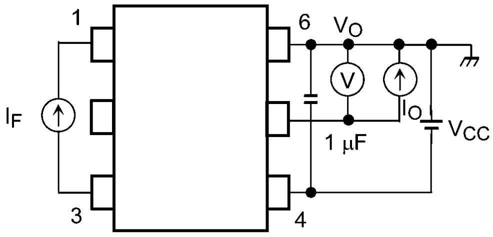


Fig. 13.1.2 I_{OPL} Test Circuit



*$V_{OH} = V_{CC}-V_O$

Fig. 13.1.3 V_{OH} Test Circuit

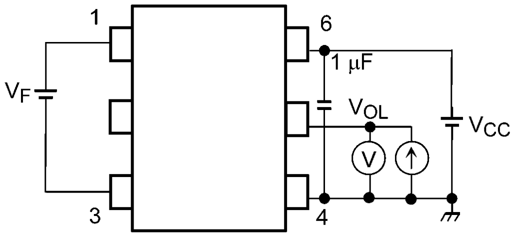


Fig. 13.1.4 V_{OL} Test Circuit

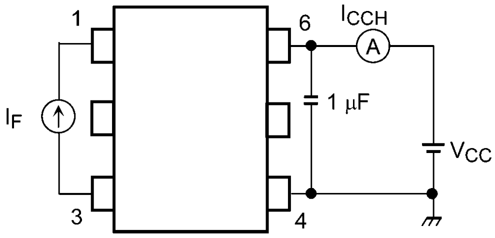


Fig. 13.1.5 I_{CCH} Test Circuit

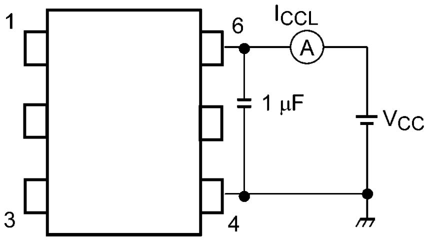


Fig. 13.1.6 I_{CCL} Test Circuit

I_F = 10 mA (P.G.)
(f = 25 kHz, duty = 50 %, t_r = t_f = 5 ns or less)

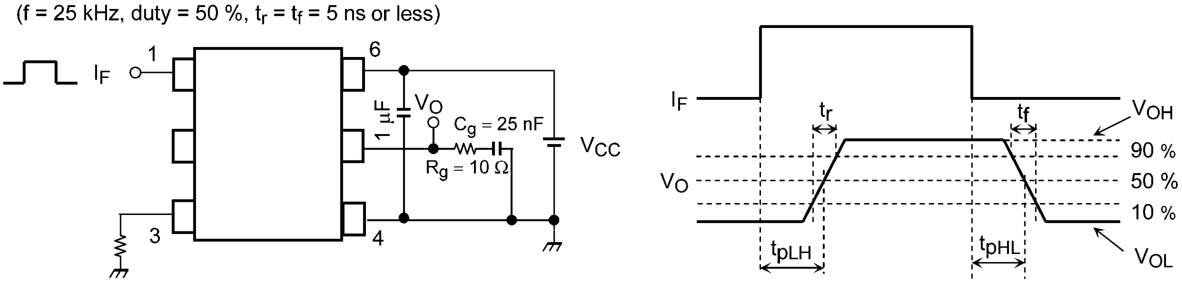


Fig. 13.1.7 Switching Time Test Circuit and Waveform

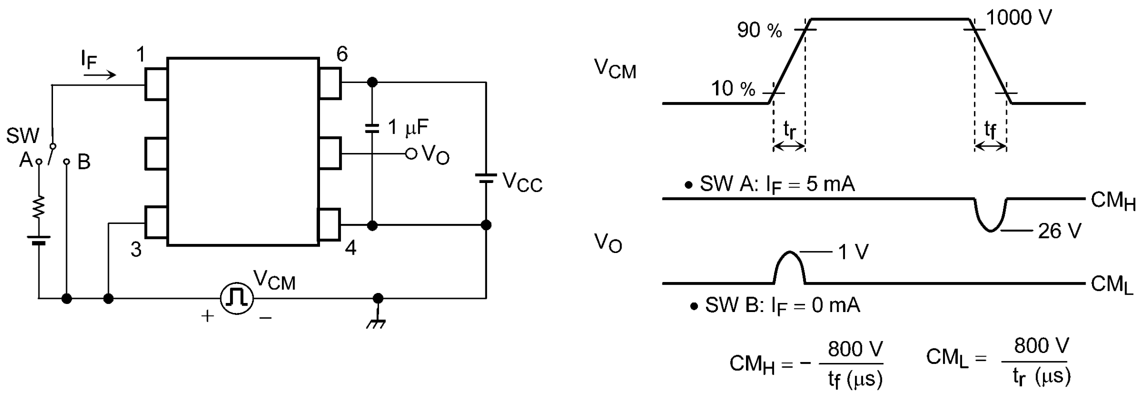


Fig. 13.1.8 Common-Mode Transient Immunity Test Circuit and Waveform

13.2. Characteristics Curves (Note)

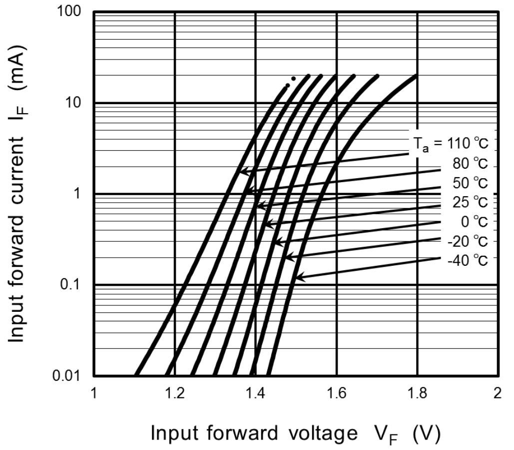


Fig. 13.2.1 I_F - V_F

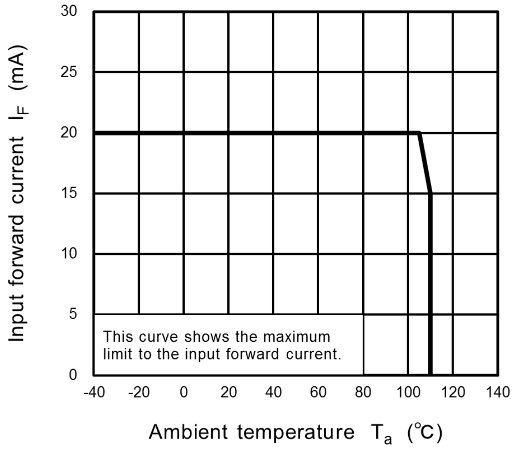


Fig. 13.2.2 I_F - T_a

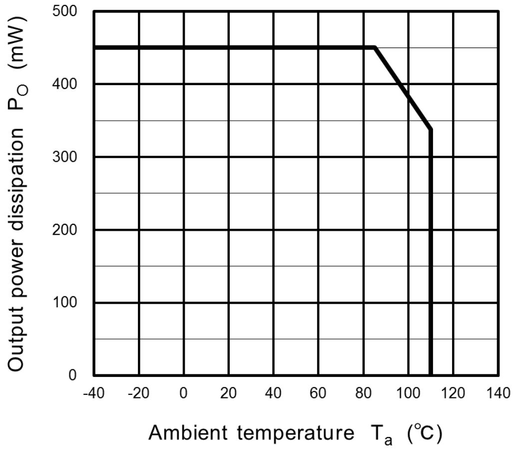


Fig. 13.2.3 P_O - T_a

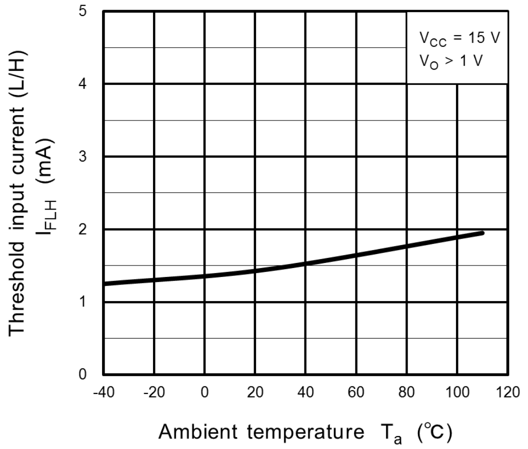


Fig. 13.2.4 I_{FLH} - T_a

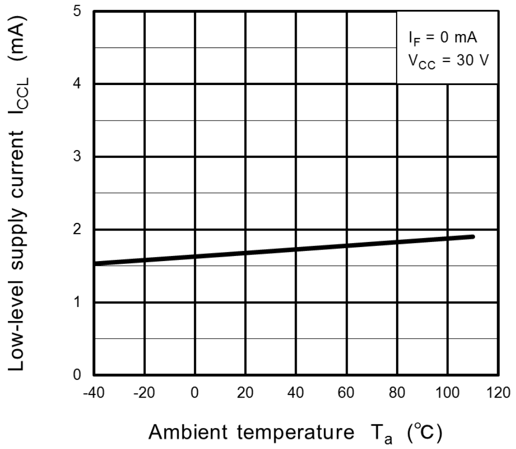


Fig. 13.2.5 I_{CCL} - T_a

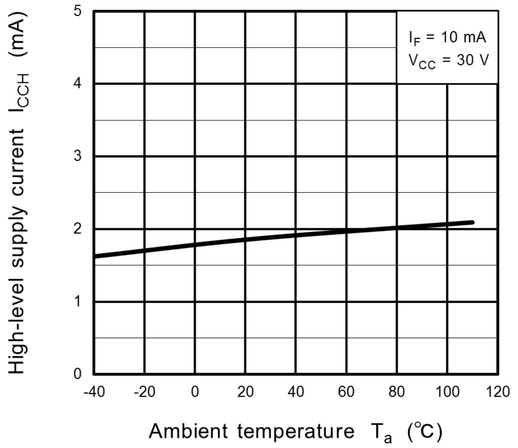


Fig. 13.2.6 I_{CCH} - T_a

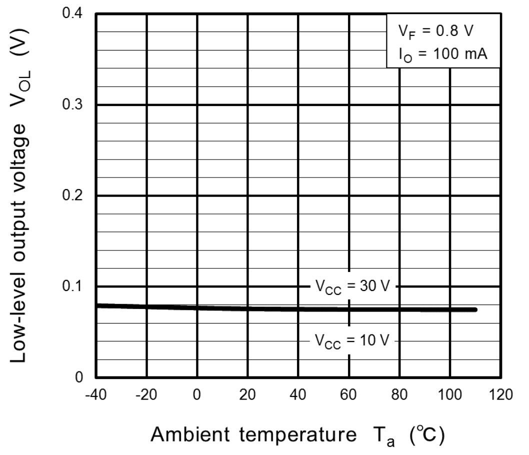


Fig. 13.2.7 V_{OL} - T_a

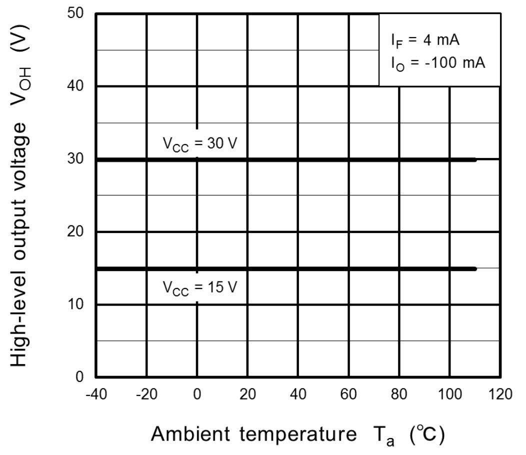


Fig. 13.2.8 V_{OH} - T_a

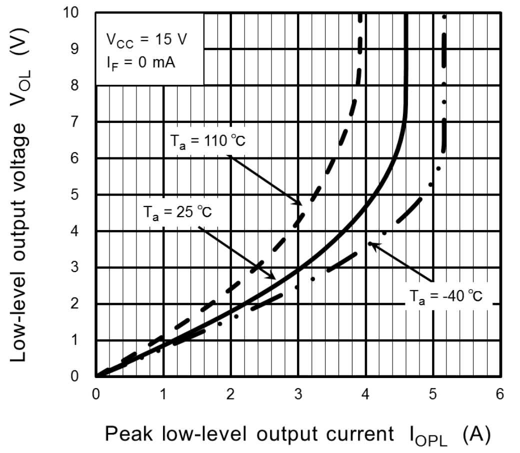


Fig. 13.2.9 V_{OL} - I_{OPL}

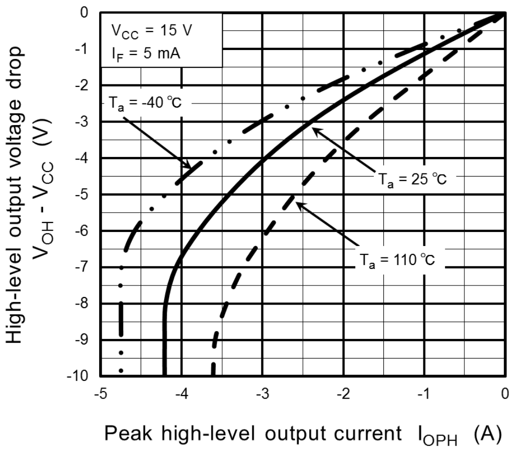


Fig. 13.2.10 (V_{OH}-V_{CC}) - I_{OPH}

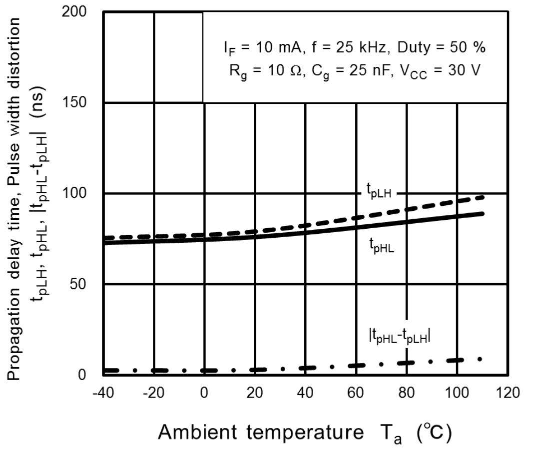


Fig. 13.2.11 t_{pLH},t_{pHL},$|t_{pHL}-t_{pLH}|$ - T_a

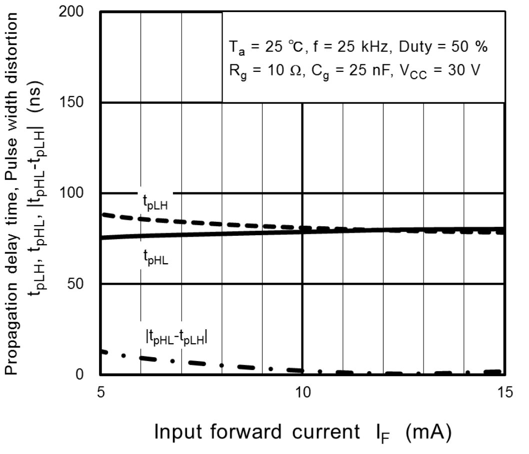


Fig. 13.2.12 t_{pLH},t_{pHL},$|t_{pHL}-t_{pLH}|$ - I_F

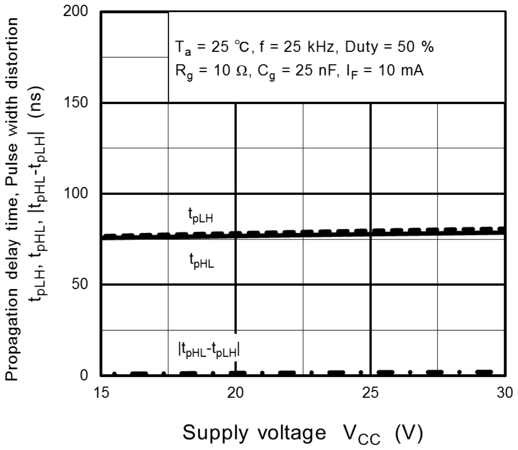


Fig. 13.2.13 $t_{pLH}, t_{pHL}, |t_{pHL}-t_{pLH}|$ - V_{CC}

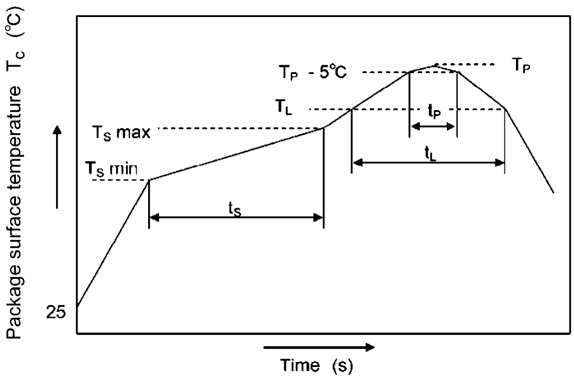
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

14. Soldering and Storage

14.1. Precautions for Soldering

The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.
  The soldering temperature profile is based on the package surface temperature.
  (See the figure shown below, which is based on the package surface temperature.)
  Reflow soldering must be performed once or twice.
  The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



	Symbol	Min	Max	Unit
Preheat temperature	T_S	150	200	°C
Preheat time	t_S	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	150	s
Peak temperature	T_P		260	°C
Time during which T_c is between (T_P – 5) and T_P	t_P		30	s
Ramp-down rate (T_P to T_L)			6	°C/s

Fig. 14.1.1 An example of a temperature profile when lead(Pb)-free solder is used

- When using soldering flow
  Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.
  Mounting condition of 260 °C within 10 seconds is recommended.
  Flow soldering must be performed once.
- When using soldering Iron
  Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C
  Heating by soldering iron must be done only once per lead.

14.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5 °C to 35 °C and 45 % to 75 %, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

15. Land Pattern Dimensions (for reference only)

Unit: mm

TLP5751

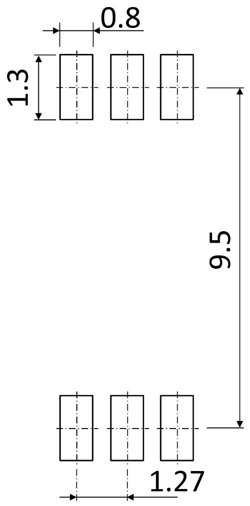


Fig. 15.1 Lead Forming Option (standard)

TLP5751(LF4)

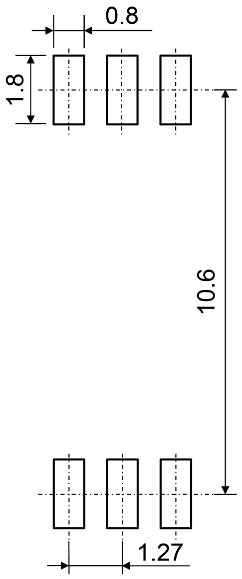
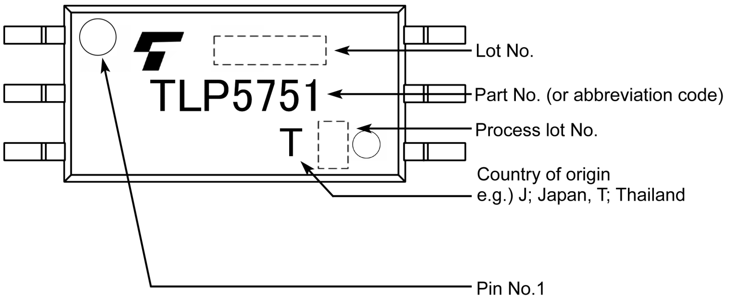


Fig. 15.2 Lead Forming Option (LF4)

16. Marking



17. EN 60747-5-5 Option (D4) Specification

- Part number: TLP5751 **(Note 1)**
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN 60747.

  Example: TLP5751(D4-TP,E

  D4: EN 60747 option
  TP: Tape type
  E: [[G]]/RoHS COMPATIBLE **(Note 2)**

Note 1: Use TOSHIBA standard type number for safety standard application.
e.g., TLP5751(D4-TP,E → TLP5751

Note 2: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.
RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

Description	Symbol	Rating	Unit
Application classification for rated mains voltage ≤ 600 Vrms for rated mains voltage ≤ 1000 Vrms		I-IV I-III	—
Climatic classification		40 / 110 / 21	—
Pollution degree		2	—
Maximum operating insulation voltage	V_{IORM}	1230	Vpeak
Input to output test voltage, Method A V_{pr} = 1.6 × V_{IORM}, type and sample test t_p = 10 s, partial discharge < 5 pC	V_{pr}	1970	Vpeak
Input to output test voltage, Method B V_{pr} = 1.875 × V_{IORM}, 100 % production test t_p = 1 s, partial discharge < 5 pC	V_{pr}	2310	Vpeak
Highest permissible overvoltage (transient overvoltage, t_{pr} = 60 s)	V_{TR}	8000	Vpeak
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve) current (input current I_F, P_{so} = 0) power (output or total power dissipation) temperature	I_{si} P_{so} T_s	300 700 150	mA mW °C
Insulation resistance V_{IO} = 500 V, T_a = 25 °C V_{IO} = 500 V, T_a = 100 °C V_{IO} = 500 V, T_a = T_s	R_{si}	≥ 10^{12} ≥ 10^{11} ≥ 10^{9}	Ω

Fig. 17.1 EN 60747 Insulation Characteristics

Minimum creepage distance	Cr	8.0 mm
Minimum clearance	Cl	8.0 mm
Minimum insulation thickness	ti	0.4 mm
Comparative tracking index	CTI	175

Fig. 17.2 Insulation Related Specifications (Note)

Note: This photocoupler is suitable for safe electrical isolation only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

Fig. 17.3 Marking on Packing

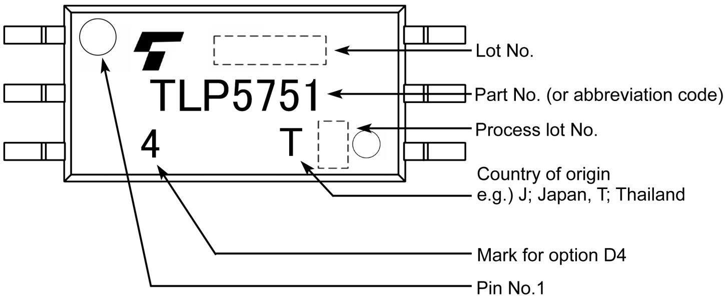


Fig. 17.4 Marking Example (Note)

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.

Figure 1 Partial discharge measurement procedure according to EN 60747
Destructive test for qualification and sampling tests.

Method A

(for type and sampling tests,
destructive tests)

t_1, t_2 = 1 to 10 s
t_3, t_4 = 1 s
t_p (Measuring time for partial discharge) = 10 s
t_b = 12 s
t_{ini} = 60 s

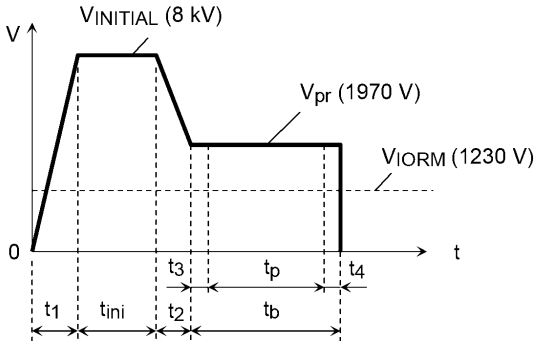


Figure 2 Partial discharge measurement procedure according to EN 60747
Non-destructive test for 100 % inspection.

Method B

(for sample test,non-
destructive test)

t_3, t_4 = 0.1 s
t_p (Measuring time for partial discharge) = 1 s
t_b = 1.2 s

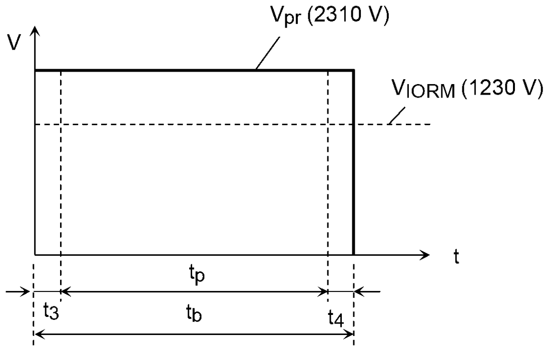


Figure 3 Dependency of maximum safety ratings on ambient temperature

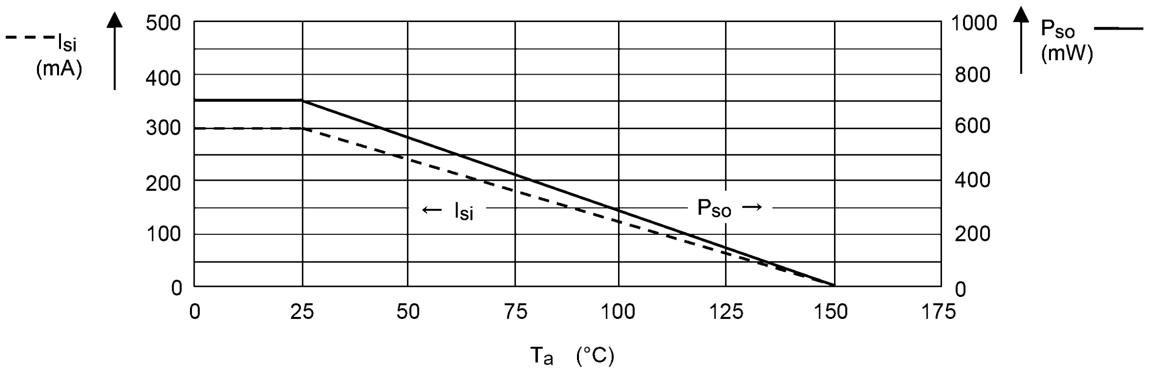


Fig. 17.5 Measurement Procedure

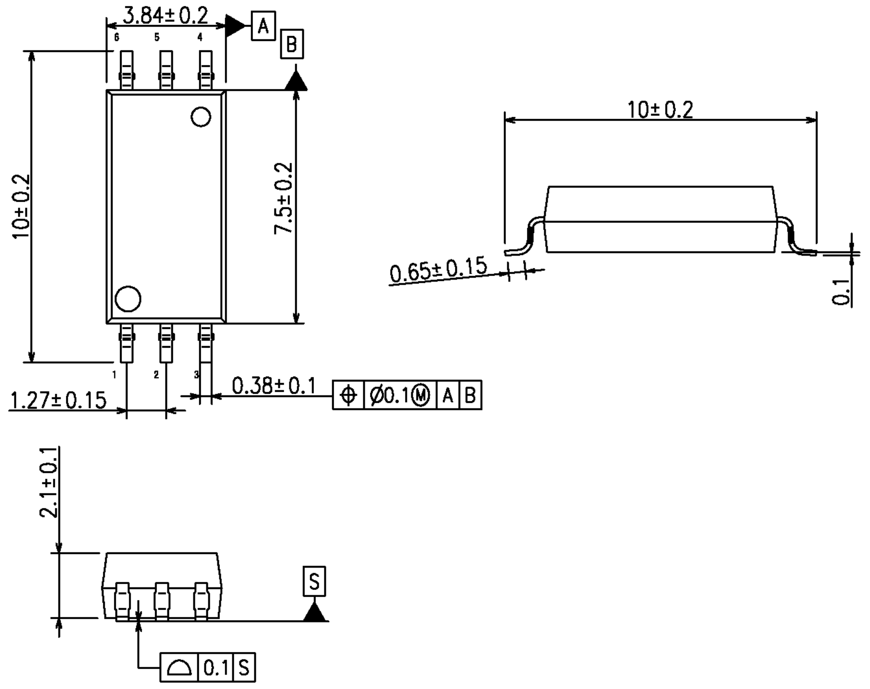
18. Ordering Information (Example of Item Name)

Item Name	Packaging	VDE Option	Packing (MOQ)
TLP5751(E			Magazine (125 pcs)
TLP5751(TP,E			Tape and reel (1500 pcs)
TLP5751(D4,E		EN 60747-5-5	Magazine (125 pcs)
TLP5751(D4-TP,E		EN 60747-5-5	Tape and reel (1500 pcs)
TLP5751(LF4,E	LF4, Wide forming		Magazine (125 pcs)
TLP5751(TP4,E	LF4, Wide forming		Tape and reel (1500 pcs)
TLP5751(D4-LF4,E	LF4, Wide forming	EN 60747-5-5	Magazine (125 pcs)
TLP5751(D4-TP4,E	LF4, Wide forming	EN 60747-5-5	Tape and reel (1500 pcs)

Package Dimensions

Unit: mm

TLP5751



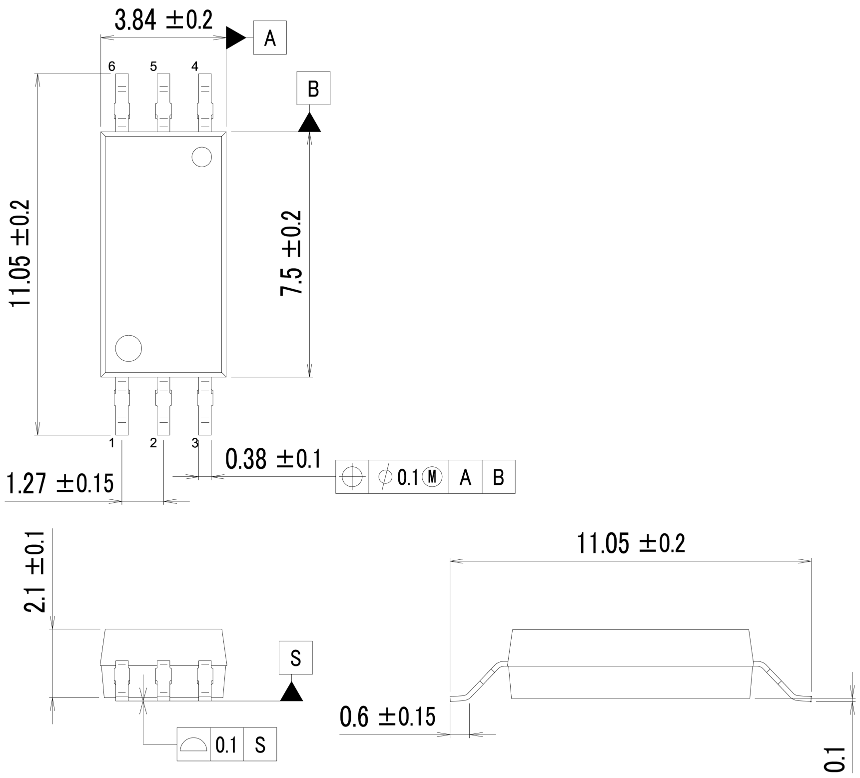
Weight: 0.126 g (typ.)

Package Name(s)
TOSHIBA: 11-4N1A

Package Dimensions

Unit: mm

TLP5751(LF4)



Weight: 0.126 g (typ.)

Package Name(s)
TOSHIBA: 11-4N101A

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