

MOSFETs Silicon N-channel MOS (U-MOS<sup>III</sup>-H)

# SSM3K361TU

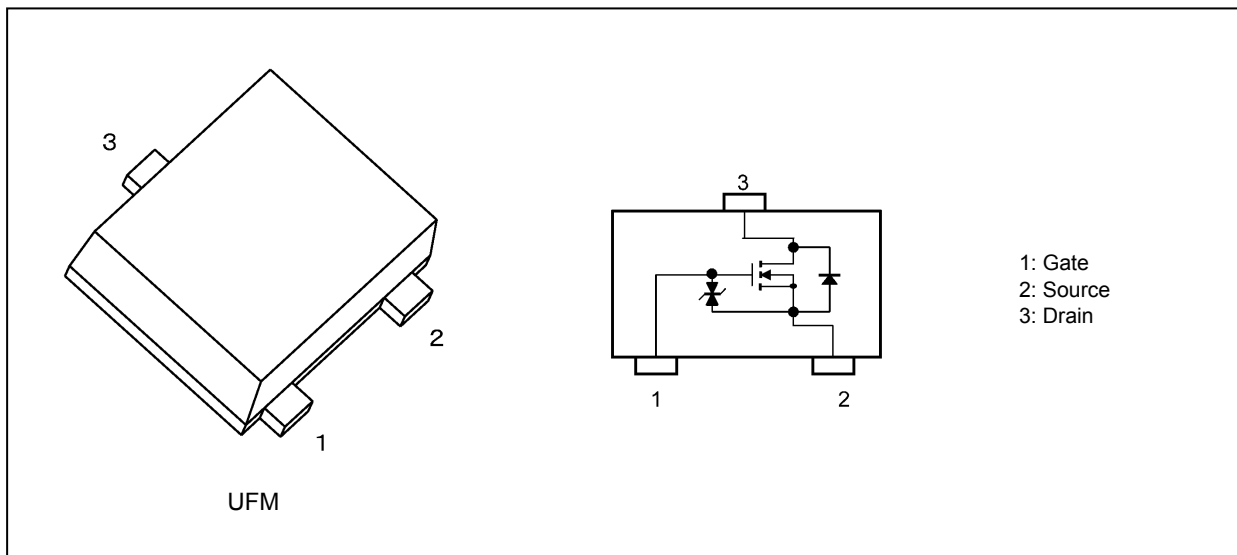
### 1. Applications

- Power Management Switches
- DC-DC Converters

### 2. Features

- (1) AEC-Q101 qualified (Please see the orderable part number list)
- (2) 175 °C MOSFET
- (3) 4.5 V drive
- (4) Low drain-source on-resistance  
 :  $R_{DS(ON)} = 65 \text{ m}\Omega$  (typ.) (@ $V_{GS} = 4.5 \text{ V}$ )  
 $R_{DS(ON)} = 51 \text{ m}\Omega$  (typ.) (@ $V_{GS} = 10 \text{ V}$ )

### 3. Packaging and Pin Assignment



### 4. Orderable part number

Orderable part number	AEC-Q101	Note
SSM3K361TU,LF	—	General Use
SSM3K361TU,LXGF	YES (Note 1)	Unintended Use (Note 1)
SSM3K361TU,LXHF	YES	Automotive Use

Note 1: For detail information, please contact our sales.

Start of commercial production  
2016-12

### 5. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	100	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC) (Note 1)	$I_D$	3.5	A
Drain current (pulsed) (Note 1), (Note 2)	$I_{DP}$	14	
Power dissipation (Note 3)	$P_D$	1.0	W
Power dissipation (t = 10 s) (Note 3)	$P_D$	1.8	
Single-pulse avalanche energy (Note 4)	$E_{AS}$	9.1	mJ
Avalanche current	$I_{AR}$	3.5	A
Channel temperature (Note 5)	$T_{ch}$	175	$^\circ\text{C}$
Storage temperature (Note 5)	$T_{stg}$	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

Note 2: Pulse width  $\leq 10\text{ ms}$ , Duty  $\leq 1\%$

Note 3: Device mounted on a  $25.4\text{ mm} \times 25.4\text{ mm} \times 1.6\text{ mm}$  FR4 glass epoxy board (Cu pad:  $645\text{ mm}^2$ )

Note 4:  $V_{DD} = 25\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (Initial state),  $L = 1\text{ mH}$ ,  $R_G = 25\ \Omega$

Note 5: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 6. Electrical Characteristics

#### 6.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	—	—	$\pm 10$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	100	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	80	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 0.1\text{ mA}$	1.5	—	2.5	V
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = 1\text{ A}, V_{GS} = 4.5\text{ V}$	—	65	92	$\text{m}\Omega$
		$I_D = 2\text{ A}, V_{GS} = 10\text{ V}$	—	51	69	

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (0.1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 6.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	430	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	22	—	
Output capacitance	$C_{oss}$		—	160	—	
Switching time (rise time)	$t_r$	$V_{DD} = 30\text{ V}, I_D = 1.0\text{ A},$ $V_{GS} = 0\text{ to }4.5\text{ V}, R_G = 50\ \Omega$ Duty $\leq 1\%$ , Input: $t_r, t_f < 5\text{ ns}$ , Common source, See Chapter 6.3.	—	9	—	ns
Switching time (turn-on time)	$t_{on}$		—	21	—	
Switching time (fall time)	$t_f$		—	7	—	
Switching time (turn-off time)	$t_{off}$		—	16	—	

#### 6.3. Switching Time Test Circuit

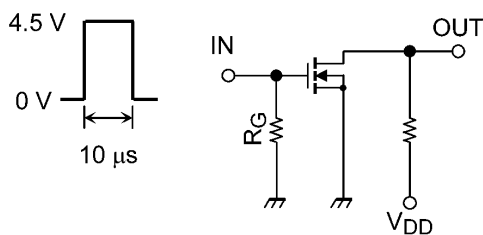


Fig. 6.3.1 Switching Time Test Circuit

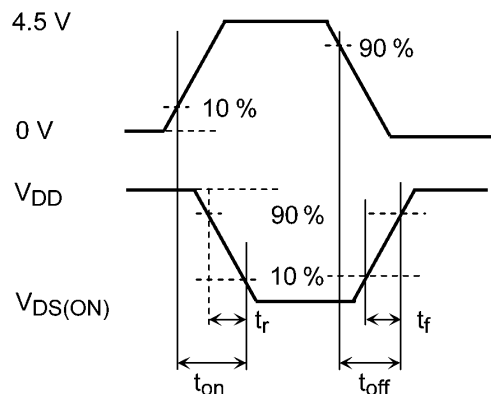


Fig. 6.3.2 Input Waveform/Output Waveform

#### 6.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = 50\text{ V}, I_D = 2.0\text{ A},$ $V_{GS} = 4.5\text{ V}$	—	3.2	—	nC
Gate-source charge 1	$Q_{gs1}$		—	1.1	—	
Gate-drain charge	$Q_{gd}$		—	1.5	—	

## 6.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = -3.5\text{ A}, V_{GS} = 0\text{ V}$	—	-0.9	-1.5	V

Note 1: Pulse measurement.

## 7. Marking

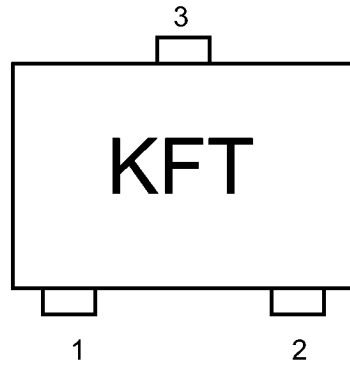


Fig. 7.1 Marking

### 8. Characteristics Curves (Note)

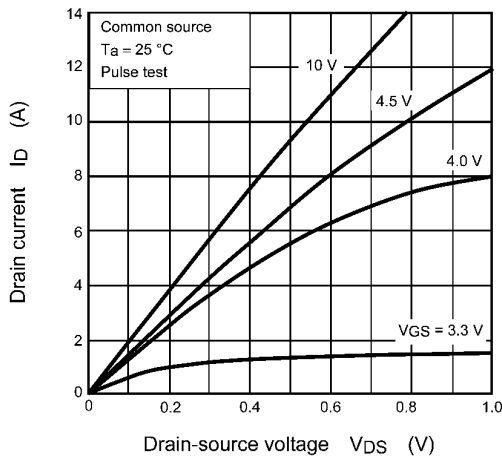


Fig. 8.1  $I_D - V_{DS}$

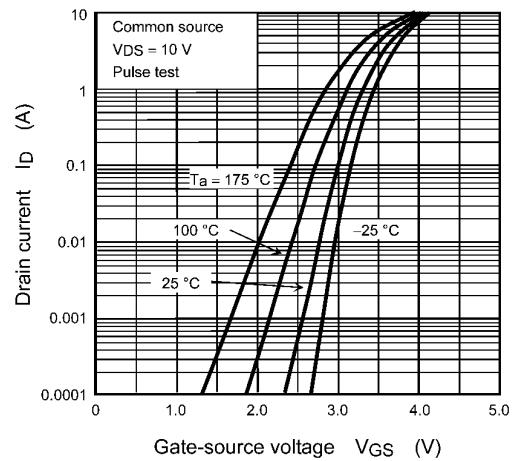


Fig. 8.2  $I_D - V_{GS}$

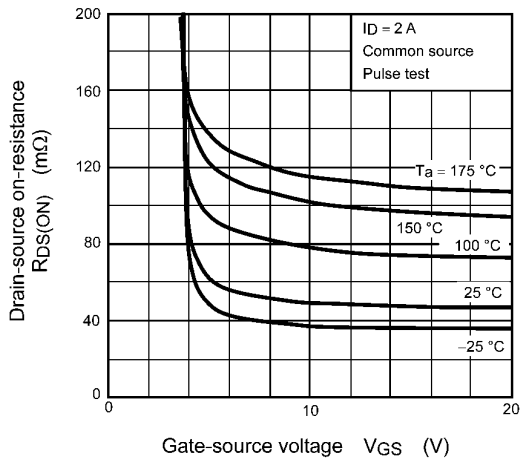


Fig. 8.3  $R_{DS(ON)} - V_{GS}$

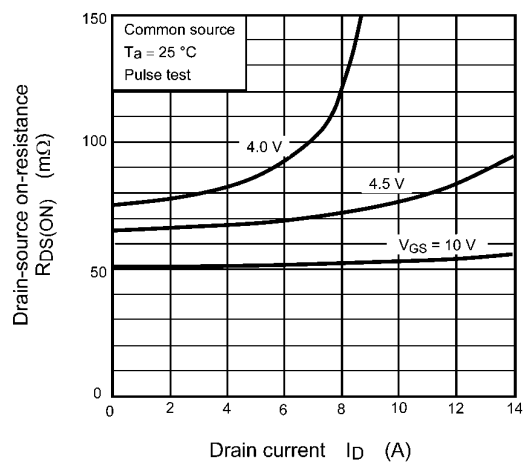


Fig. 8.4  $R_{DS(ON)} - I_D$

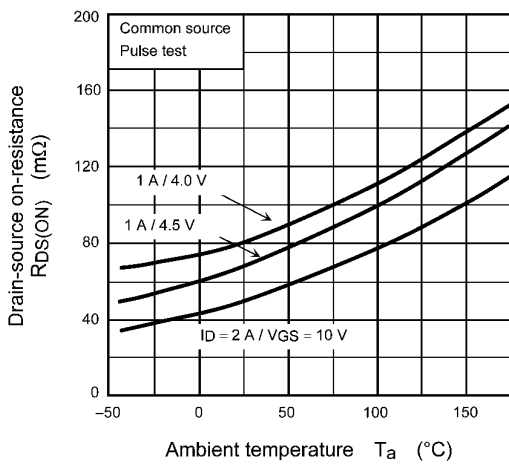


Fig. 8.5  $R_{DS(ON)} - T_a$

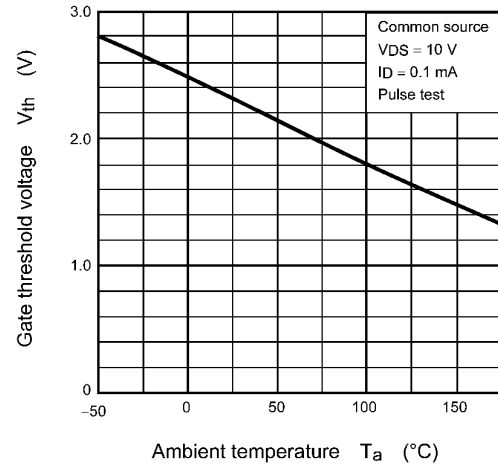
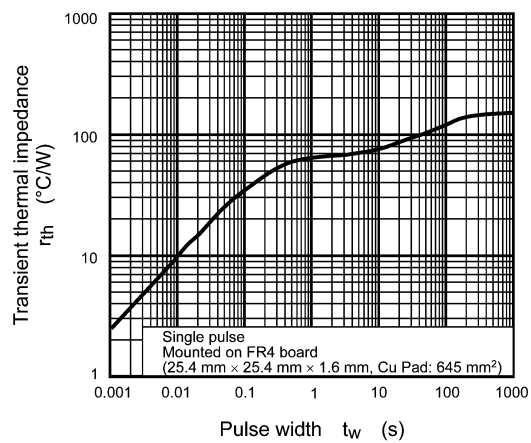
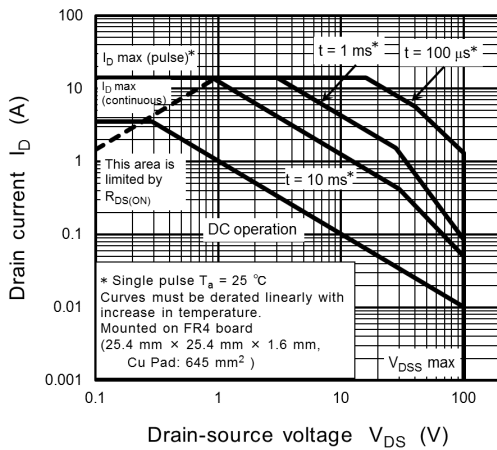
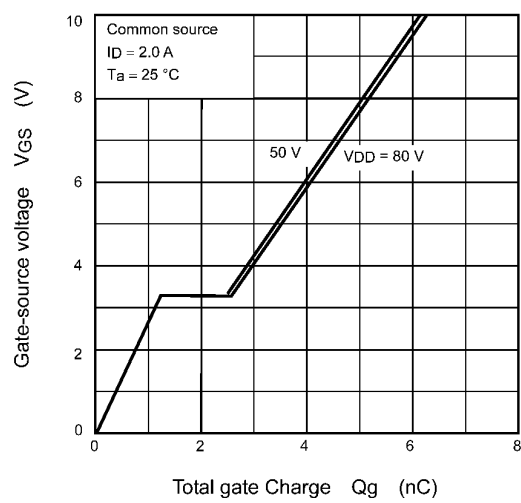
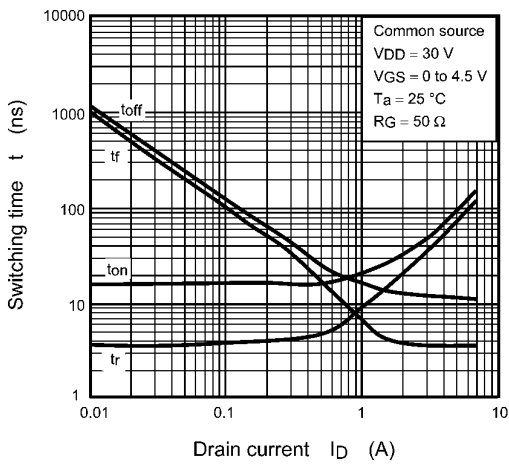
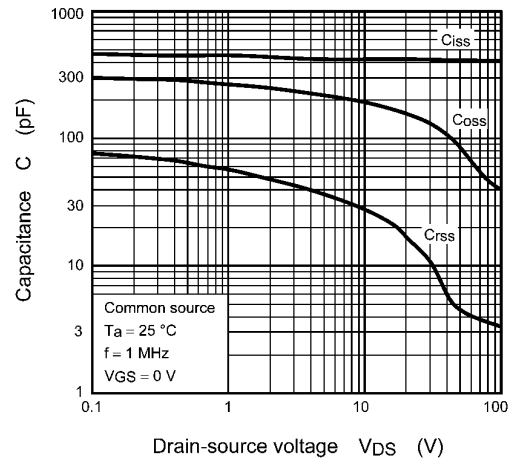
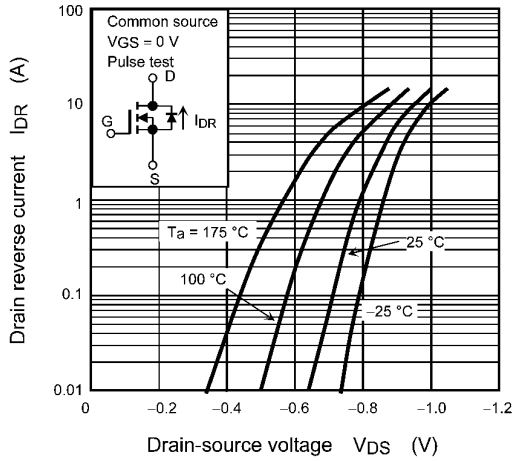


Fig. 8.6  $V_{th} - T_a$



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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