

TLP750

- Digital Logic Ground Isolation
- Line Receiver
- Microprocessor System Interfaces
- Switching Power Supply Feedback Control
- Analog Signal Isolation
- Transistor Inverter

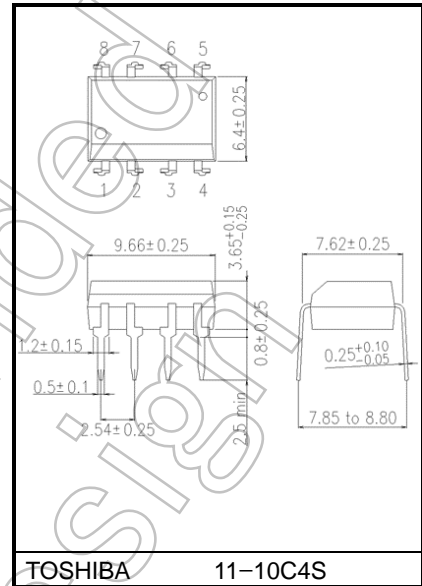
Unit: mm

The TOSHIBA TLP750 consists of a high-output infrared light emitting diode optically coupled to a high-speed photodiode with a transistor amplifier and is housed in an 8-pin DIP. The TLP750 has no internal base connection and features noise immunity, thus it is suitable for inverter drivers for variable-speed motor drives.

- Switching speed: $t_{pHL}=0.3\mu s$ (typ.)
- Switching speed: $t_{pLH}=0.5\mu s$ (typ.) ($R_L=1.9k\Omega$)
- Isolation voltage: 5000 V_{rms} (min)
- UL-recognized: UL 1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
- VDE-approved: EN 60747-5-5 (Note 1)

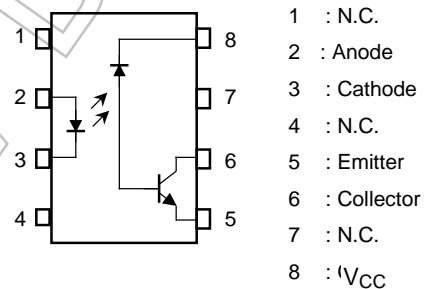
Note 1 : When a VDE approved type is needed, please designate the **Option(D4)**.

- Creepage distance: 6.4mm (min)
- Clearance: 6.4mm (min)
- Insulation thickness: 0.4mm (min)

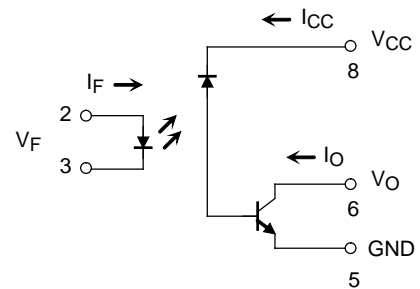


Weight: 0.54 g (typ.)

Pin Configuration (top view)



Schematic



Start of commercial production
1989-10

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Note 1)	IF	25	mA
	Pulse forward current (Note 2)	IFP	50	mA
	Peak transient forward current (Note 3)	IFPT	1	A
	Reverse voltage	VR	5	V
	Diode power dissipation (Note 4)	PD	45	mW
Detector	Output current	IO	8	mA
	Peak output current	IOP	16	mA
	Output voltage	VO	-0.5 to 15	V
	Supply voltage	VCC	-0.5 to 15	V
	Output power dissipation (Note 5)	PO	100	mW
Operating temperature range		Topr	-55 to 100	°C
Storage temperature range		Tstg	-55 to 125	°C
Lead solder temperature(10 s) (Note 6)		Tsol	260	°C
Isolation voltage (AC, 60 s, R.H.= 60 %) (Note 7)		BVs	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8 mA / °C above 70 °C.

(Note 2) 50 % duty cycle, 1ms pulse width.
Derate 1.6 mA / °C above 70 °C.

(Note 3) Pulse width ≤ 1 μs, 300 pps.

(Note 4) Derate 0.9 mW / °C above 70 °C.

(Note 5) Derate 2 mW / °C above 70 °C.

(Note 6) Soldering portion of lead: Up to 2mm from the body of the device.

(Note 7) Device considered a two terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit															
LED	Forward voltage	V_F	$I_F = 16 \text{ mA}$	—	1.65	1.85	V															
	Forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$	$I_F = 16 \text{ mA}$	—	-2	—	mV / °C															
	Reverse current	I_R	$V_R = 5 \text{ V}$	—	—	10	μA															
	Capacitance between terminal	C_T	$V_F = 0 \text{ V}, f = 1 \text{ MHz}$	—	45	—	pF															
Detector	High level output current	$I_{OH(1)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 5.5 \text{ V}$	—	3	500	nA															
		$I_{OH(2)}$	$I_F = 0 \text{ mA}, V_{CC} = V_O = 15 \text{ V}$	—	—	5	μA															
		I_{OH}	$I_F = 0 \text{ mA}, V_{CC} = V_O = 15 \text{ V}, T_a = 70 \text{ }^\circ\text{C}$	—	—	50	μA															
	High level supply voltage	I_{CCH}	$I_F = 0 \text{ mA}, V_{CC} = 15 \text{ V}$	—	0.01	1	μA															
Coupled/ Insulation	Current transfer ratio	I_O/I_F	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}, V_O = 0.4 \text{ V}$	$T_a = 25 \text{ }^\circ\text{C}$	10	30	—	%														
				Rank: O	19	30	—															
				$T_a = 0 \text{ to } 70 \text{ }^\circ\text{C}$	5	—	—															
	Low level output voltage	V_{OL}	$I_F = 16 \text{ mA}, V_{CC} = 4.5 \text{ V}, I_O = 1.1 \text{ mA}$ (rank O: $I_O = 2.4 \text{ mA}$)			—	—	0.4	V													
										Isolation resistance	R_S	$R.H. \leq 60 \%, V_S = 500 \text{ V}_{DC}$ (Note 7)	1×10^{12}	10^{14}	—	Ω						
																	Capacitance between input to output	C_S	$V_S = 0 \text{ V}, f = 1 \text{ MHz}$ (Note 7)	—	0.8	—
Isolation Voltage																						

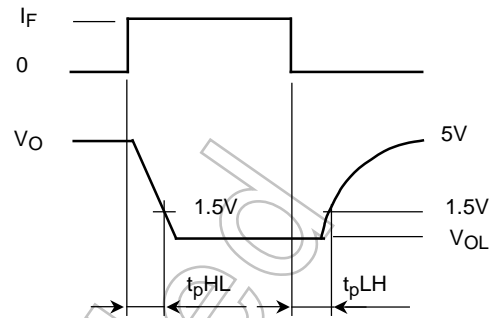
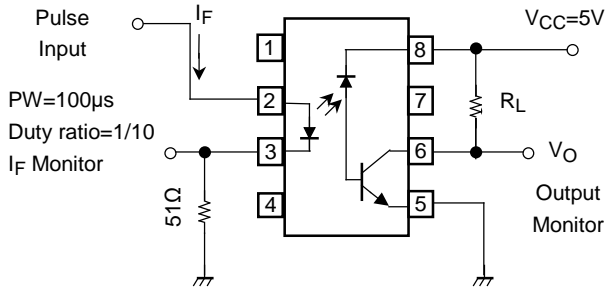
Switching Characteristics (Ta = 25°C, Vcc = 5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (H→L)	t_{pHL}	1	$I_F = 16 \text{ mA}, R_L = 4.1 \text{ k}\Omega$	—	0.2	0.8	μs
			Rank O: $R_L = 1.9 \text{ k}\Omega$	—	0.3	0.8	
Propagation delay time (L→H)	t_{pLH}	1	$I_F = 16 \text{ mA}, R_L = 4.1 \text{ k}\Omega$	—	1	2	μs
			Rank O: $R_L = 1.9 \text{ k}\Omega$	—	0.5	1.2	
Common mode transient immunity at logic high output (Note 8)	CM_H	2	$I_F = 0 \text{ mA}, V_{CM} = 200 \text{ V}_{p-p}, R_L = 4.1 \text{ k}\Omega$ (Rank O: $R_L = 1.9 \text{ k}\Omega$)	—	1500	—	V / μs
Common mode transient immunity at logic low output (Note 8)	CM_L	2	$I_F = 16 \text{ mA}, V_{CM} = 200 \text{ V}_{p-p}, R_L = 4.1 \text{ k}\Omega$ (Rank O: $R_L = 1.9 \text{ k}\Omega$)	—	-1500	—	V / μs

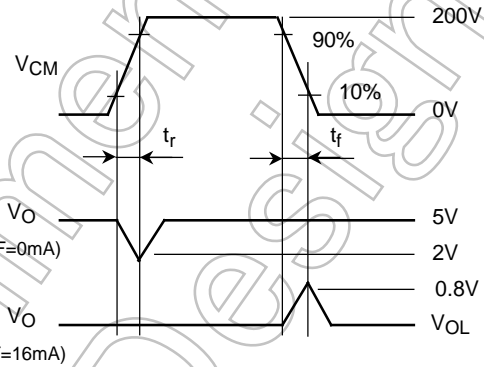
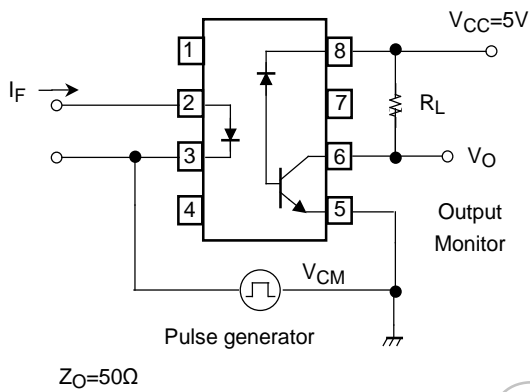
(Note 8) CML is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8 \text{ V}$).

CMH is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0 \text{ V}$).

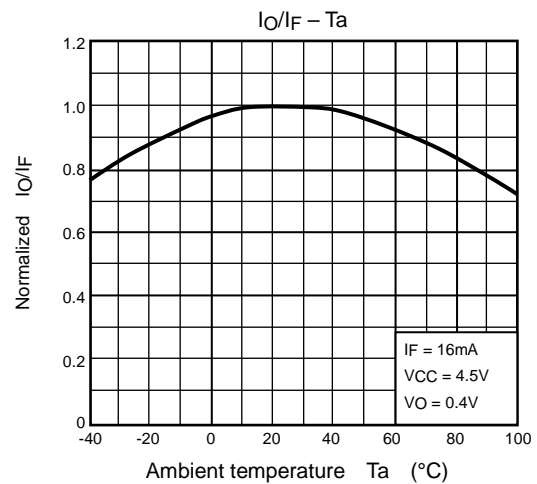
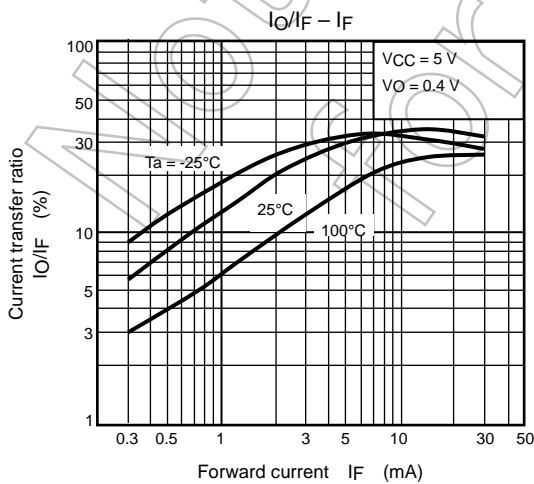
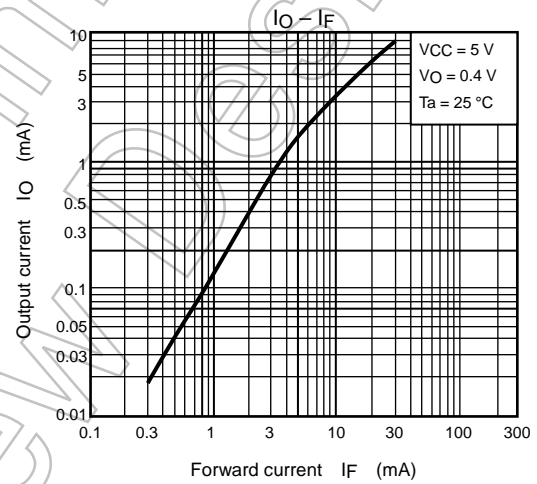
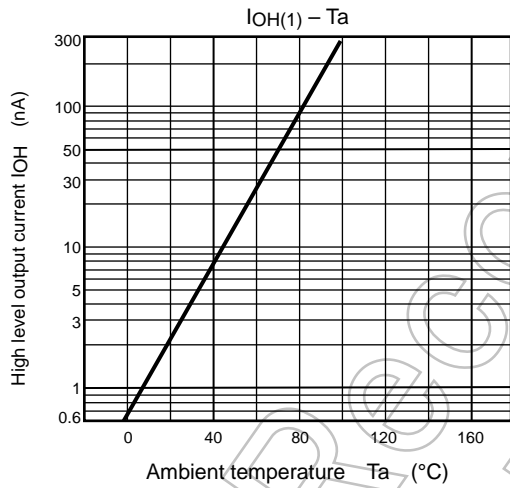
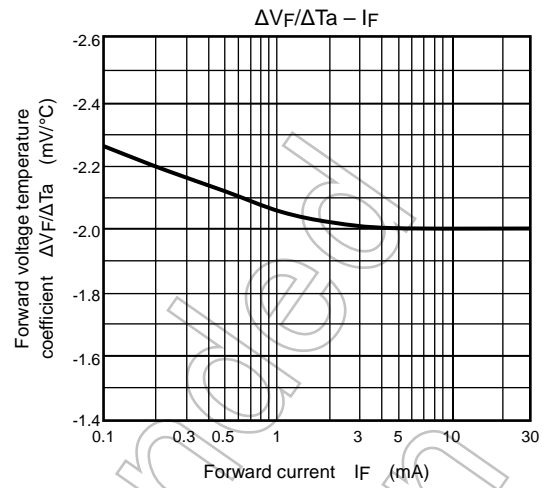
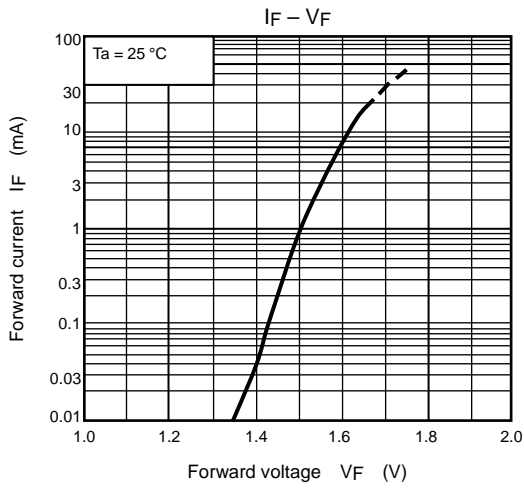
Test Circuit 1: Switching Time Test Circuit



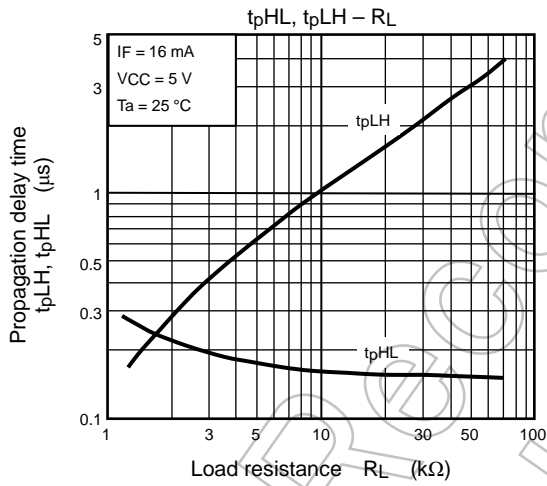
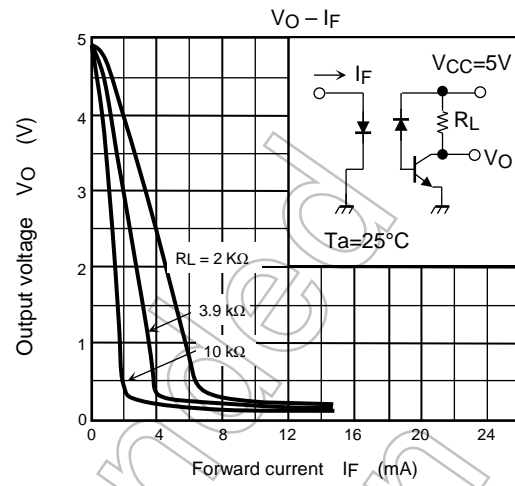
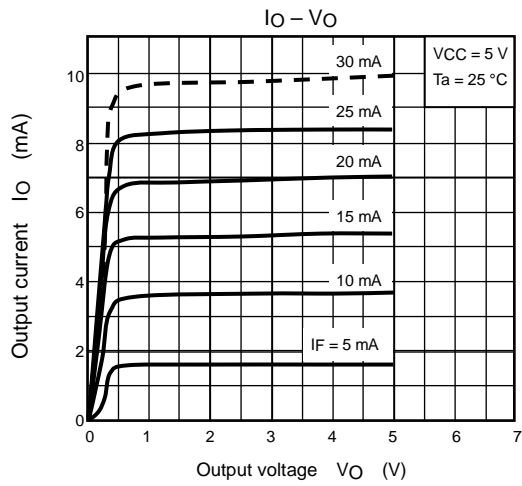
Test Circuit 2: Common Mode Noise Immunity Test Circuit



$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$



NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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