

MOSFETs Silicon P-Channel MOS

# SSM6J401TU

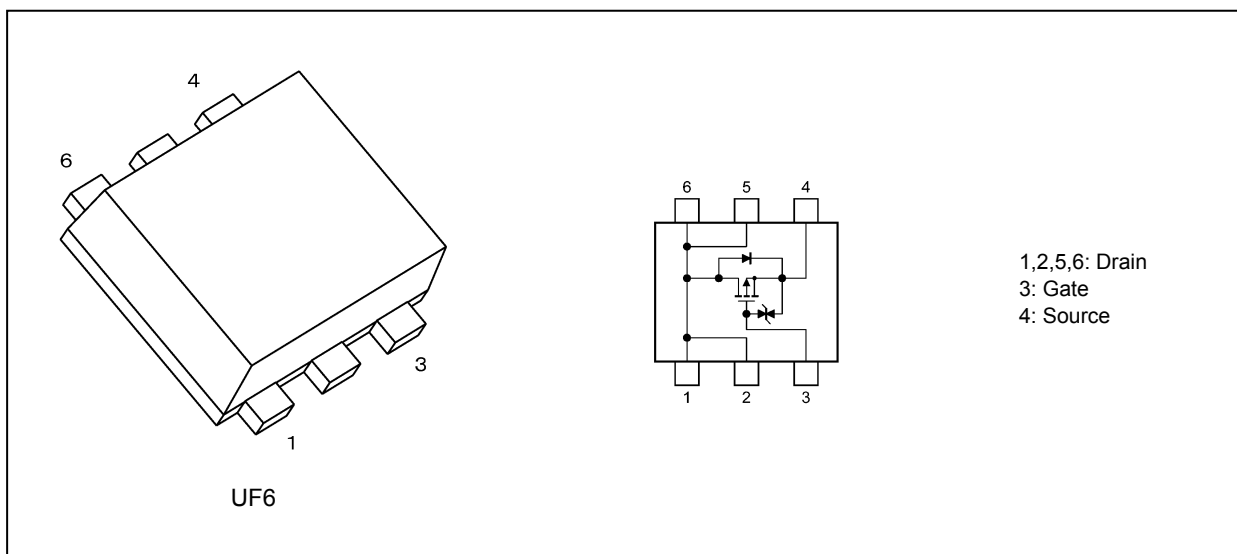
## 1. Applications

- DC-DC Converters
- High-Speed Switching

## 2. Features

- (1) 4.0 V gate drive voltage.
- (2) Low drain-source on-resistance  
:  $R_{DS(ON)} = 145 \text{ m}\Omega$  (max) (@ $V_{GS} = -4 \text{ V}$ )  
 $R_{DS(ON)} = 73 \text{ m}\Omega$  (max) (@ $V_{GS} = -10 \text{ V}$ )

## 3. Packaging and Pin Assignment



Start of commercial production  
2007-07

### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	-30	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	V
Drain current (DC)	$I_D$	-2.5	A
Drain current (pulsed)	$I_{DP}$	-5.0	
Power dissipation (Note 1)	$P_D$	500	mW
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Device mounted on a FR4 board.

(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad : 645 mm<sup>2</sup>)

Note: The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

Note: The channel-to-ambient thermal resistance,  $R_{th(ch-a)}$ , and the drain power dissipation,  $P_D$ , vary according to the board material, board area, board thickness and pad area. When using this device, be sure to take heat dissipation fully into account.

### 5. Electrical Characteristics

#### 5.1. Static Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	—	—	-10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0\text{ V}$	-30	—	—	V
Drain-source breakdown voltage (Note 1)	$V_{(BR)DSX}$	$I_D = -1\text{ mA}, V_{GS} = 20\text{ V}$	-15	—	—	
Gate threshold voltage (Note 2)	$V_{th}$	$V_{DS} = -5\text{ V}, I_D = -1\text{ mA}$	-1.2	—	-2.6	
Drain-source on-resistance (Note 3)	$R_{DS(ON)}$	$I_D = -1.5\text{ A}, V_{GS} = -4\text{ V}$	—	85	145	$\text{m}\Omega$
		$I_D = -2.0\text{ A}, V_{GS} = -10\text{ V}$	—	53	73	
Forward transfer admittance (Note 3)	$ Y_{fs} $	$V_{DS} = -5\text{ V}, I_D = -2.0\text{ A}$	3.1	6.2	—	S

Note 1: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

Note 2: Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to below (-1 mA for this device). Then, for normal switching operation,  $V_{GS(ON)}$  must be higher than  $V_{th}$ , and  $V_{GS(OFF)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .

Take this into consideration when using the device.

Note 3: Pulse measurement.

#### 5.2. Dynamic Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$	—	730	—	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	90	—	
Output capacitance	$C_{oss}$		—	110	—	
Switching time (turn-on time)	$t_{on}$	$V_{DD} = -15\text{ V}, I_D = -2.0\text{ A},$ $V_{GS} = 0\text{ to }-4.0\text{ V}, R_G = 10\text{ }\Omega$ Duty $\leq 1\%$ , Input: $t_r, t_f < 5\text{ ns}$ Common source	—	33	—	ns
Switching time (turn-off time)	$t_{off}$		—	27	—	

#### 5.3. Switching Time Test Circuit

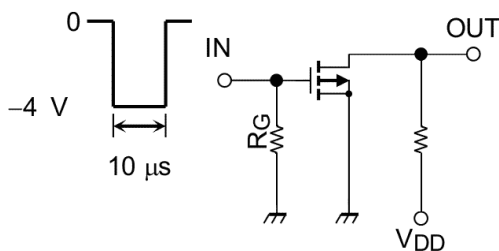


Fig. 5.3.1 Switching Time Test Circuit

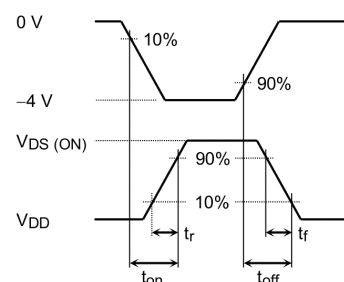


Fig. 5.3.2 Input Waveform/Output Waveform

#### 5.4. Gate Charge Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DS} = -15\text{ V}, I_D = -2.5\text{ A},$ $V_{GS} = -10\text{ V}$	—	16.0	—	nC
Gate-source charge	$Q_{gs}$		—	12.8	—	
Gate-drain charge	$Q_{gd}$		—	3.2	—	

## 5.5. Source-Drain Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage (Note 1)	$V_{DSF}$	$I_D = 2.5\text{ A}, V_{GS} = 0\text{ V}$	—	0.8	1.2	V

Note 1: Pulse measurement.

## 6. Marking

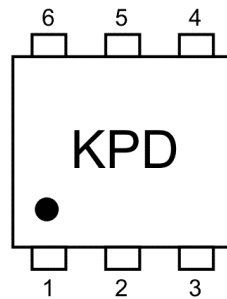


Fig. 6.1 Marking

### 7. Characteristics Curves (Note)

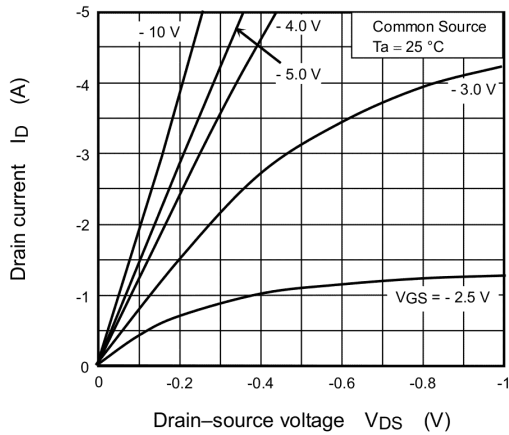


Fig. 7.1  $I_D - V_{DS}$

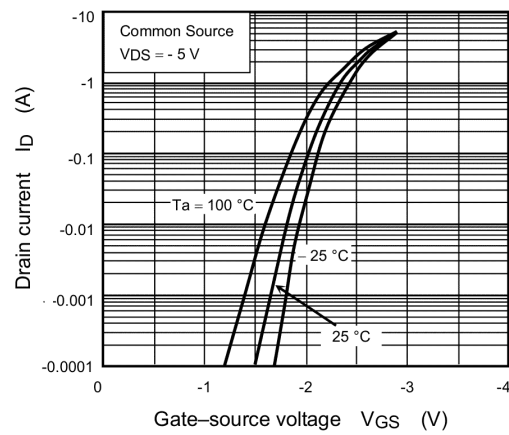


Fig. 7.2  $I_D - V_{GS}$

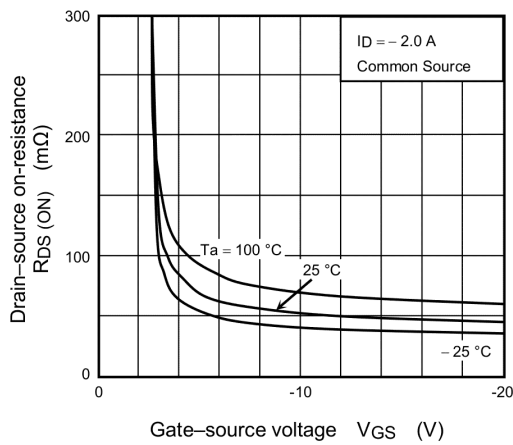


Fig. 7.3  $R_{DS(ON)} - V_{GS}$

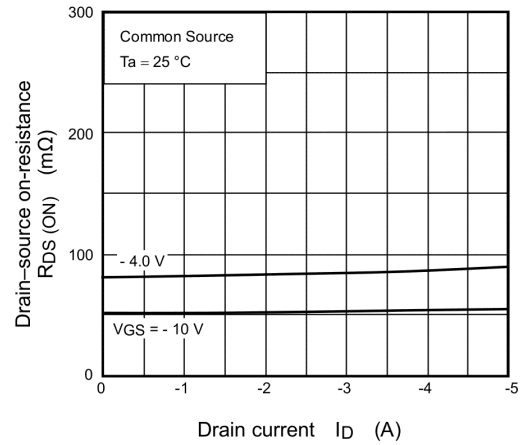


Fig. 7.4  $R_{DS(ON)} - I_D$

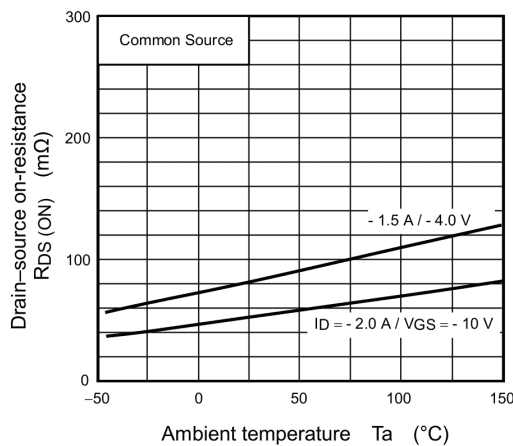


Fig. 7.5  $R_{DS(ON)} - T_a$

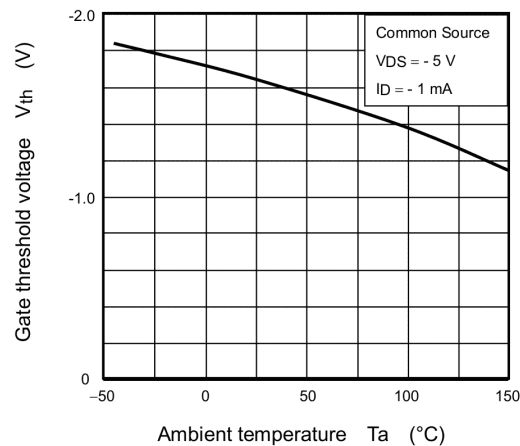


Fig. 7.6  $V_{th} - T_a$

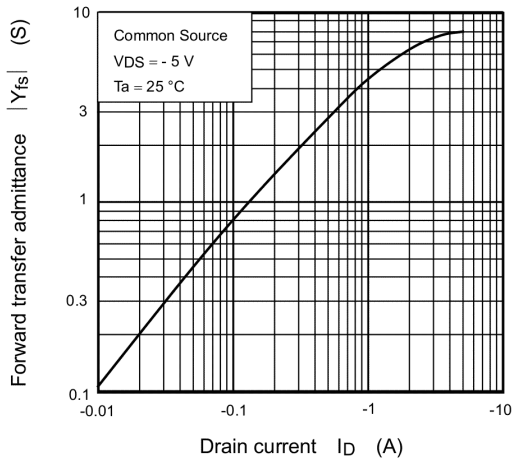


Fig. 7.7  $|Y_{fs}| - I_D$

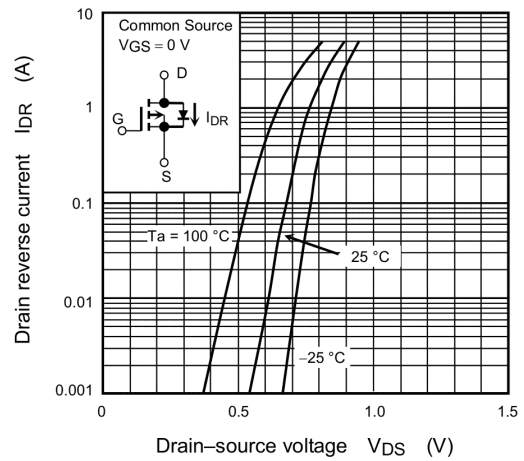


Fig. 7.8  $I_{DR} - V_{DS}$

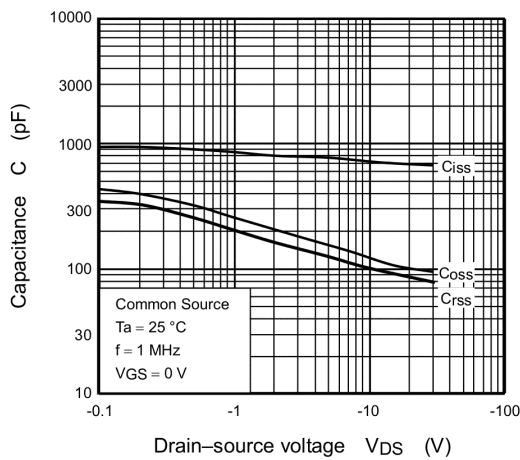


Fig. 7.9  $C - V_{DS}$

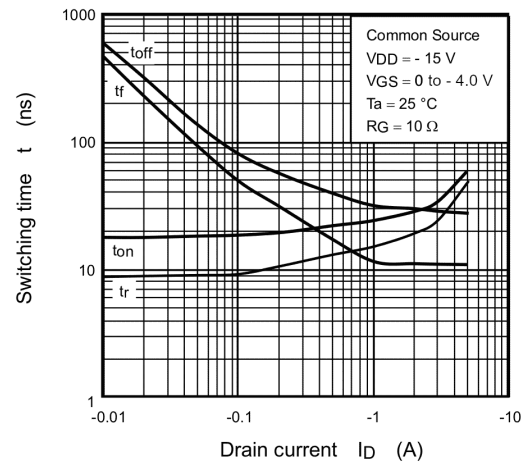


Fig. 7.10  $t - I_D$

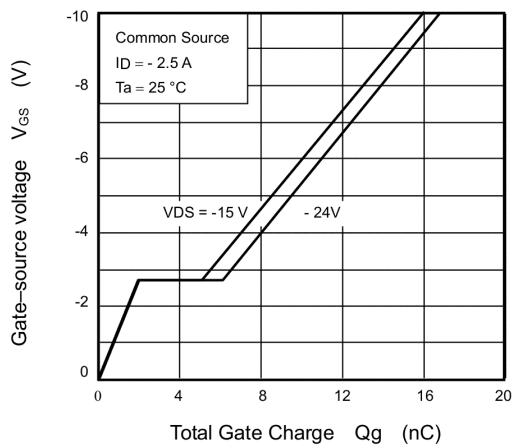


Fig. 7.11 Dynamic Input Characteristics

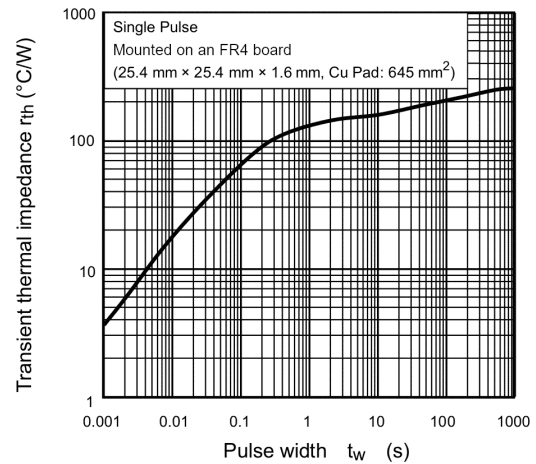
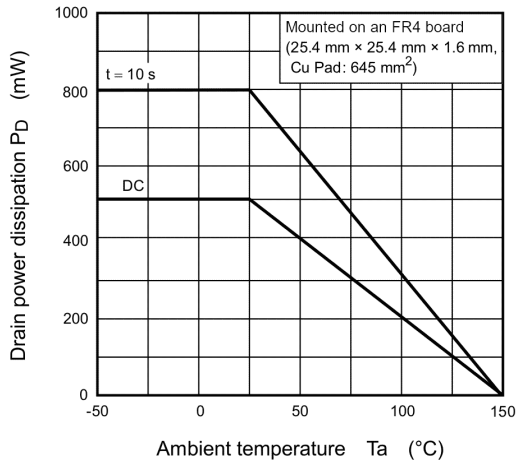
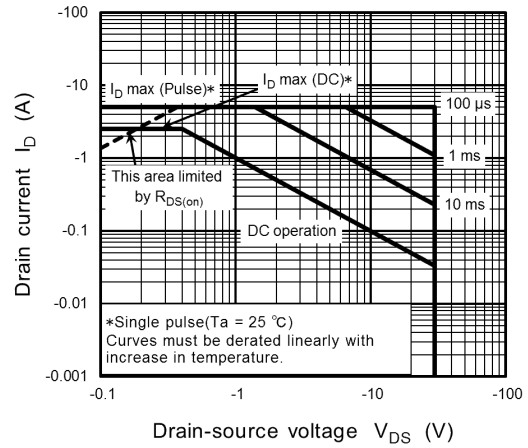


Fig. 7.12  $r_{th} - t_w$



**Fig. 7.13  $P_D - T_a$**



**Fig. 7.14 Safe Operating Area**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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