

# TLP701AF

## 1. Applications

- Industrial Inverters
- MOSFET Gate Drivers
- IGBT Gate Drivers
- Induction Cooktop and Home Appliances

## 2. General

The TLP701AF is a photocoupler in a SDIP6 package that consists of an infrared LED optically coupled to an integrated high-gain, high-speed photodetector IC chip. The TLP701AF is physically smaller than the one in an 8-pin DIP package and compliant with international safety standards for reinforced insulation. It thus provides a smaller footprint solution for applications that require safety standard certification. The TLP701AF has an internal Faraday shield that provides a guaranteed Common-mode transient immunity of  $\pm 20$  kV/ $\mu$ s. It has a totem-pole output that can both sink and source current. It is ideal for IGBT and power MOSFET gate drive. Leads of the TLP701AF is bend to satisfy 8 mm PC board spacing requirements. Absolute maximum ratings and electrical characteristics are the same as in the TLP701A.

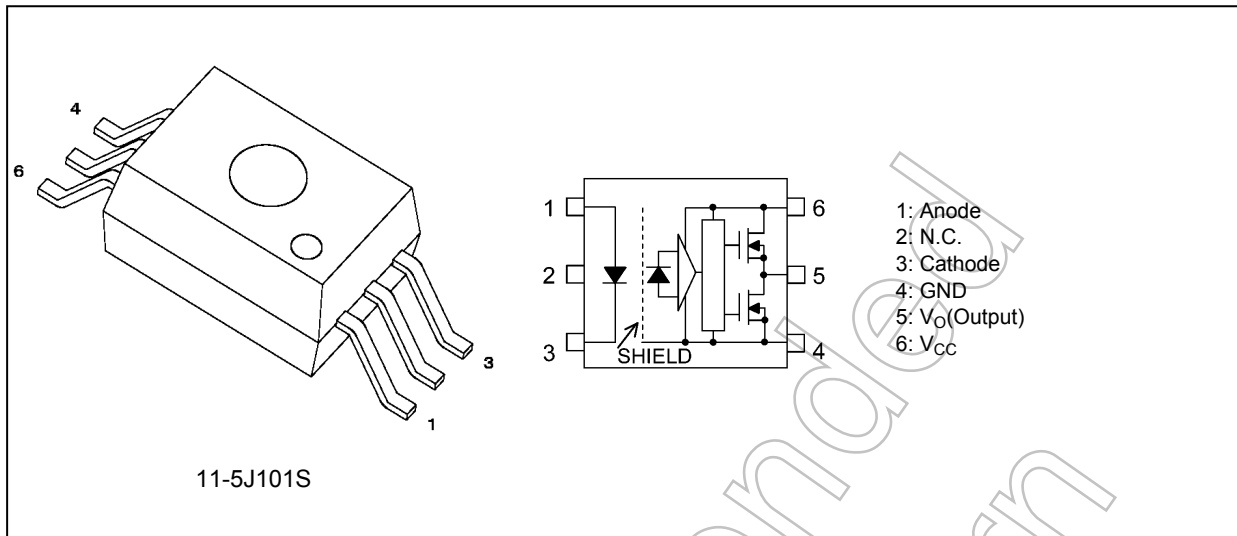
## 3. Features

- (1) Output peak current:  $\pm 0.6$  A (max)
- (2) Operating temperature:  $-40$  to  $100^{\circ}\text{C}$
- (3) Supply current: 2 mA (max)
- (4) Supply voltage: 10 to 30 V
- (5) Threshold input current: 5 mA (max)
- (6) Propagation delay time: 500 ns (max)
- (7) Common-mode transient immunity:  $\pm 20$  kV/ $\mu$ s (min)
- (8) Isolation voltage: 5000 V<sub>rms</sub> (min)
- (9) Safety standards
  - UL-recognized: UL 1577, File No.E67349
  - cUL-recognized: CSA Component Acceptance Service No.5A File No.E67349
  - VDE-approved: EN 60747-5-5, EN 62368-1 (**Note 1**)

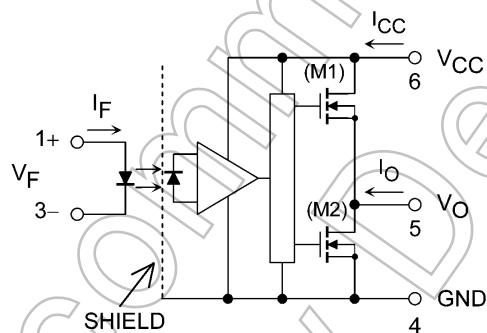
Note 1: When a VDE approved type is needed, please designate the **Option (D4)**.

Start of commercial production  
2011-01

## 4. Packaging and Pin Configuration



## 5. Internal Circuit (Note)



Note: A 0.1- $\mu$ F bypass capacitor must be connected between pin 6 and pin 4.

## 6. Principle of Operation

### 6.1. Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

### 6.2. Mechanical Parameters

Characteristics	7.62-mm Pitch TLP701A	10.16-mm Pitch TLP701AF	Unit
Creepage distances	7.0 (min)	8.0 (min)	mm
Clearance distances	7.0 (min)	8.0 (min)	
Internal isolation thickness	0.4 (min)	0.4 (min)	

## 7. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^\circ\text{C}$ )

	Characteristics	Symbol	Note	Rating	Unit
LED	Input forward current	$I_F$		25	mA
	Input forward current derating ( $T_a \geq 85^\circ\text{C}$ )	$\Delta I_F/\Delta T_a$		-0.67	mA/ $^\circ\text{C}$
	Peak transient input forward current	$I_{FPT}$	(Note 1)	1	A
	Peak transient input forward current derating ( $T_a \geq 85^\circ\text{C}$ )	$\Delta I_{FPT}/\Delta T_a$		-25	mA/ $^\circ\text{C}$
	Input reverse voltage	$V_R$		5	V
	Input power dissipation	$P_D$		40	mW
	Input power dissipation derating ( $T_a \geq 85^\circ\text{C}$ )	$\Delta P_D/\Delta T_a$		-1.0	mW/ $^\circ\text{C}$
Detector	Peak high-level output current ( $T_a = -40$ to $100^\circ\text{C}$ )	$I_{OPH}$	(Note 2)	-0.6	A
	Peak low-level output current ( $T_a = -40$ to $100^\circ\text{C}$ )	$I_{OPL}$	(Note 2)	+0.6	
	Output voltage	$V_O$		35	V
	Output power dissipation	$P_O$		80	mW
	Output power dissipation derating ( $T_a \geq 85^\circ\text{C}$ )	$\Delta P_O/\Delta T_a$		-2.0	mW/ $^\circ\text{C}$
	Supply voltage	$V_{CC}$		35	V
Common	Operating temperature	$T_{opr}$		-40 to 100	$^\circ\text{C}$
	Storage temperature	$T_{stg}$		-55 to 125	
	Lead soldering temperature (10 s)	$T_{sol}$	(Note 3)	260	
	Isolation voltage AC, 60 s, R.H. $\leq 60\%$ , $T_a = 25^\circ\text{C}$	$BV_S$	(Note 4)	5000	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Pulse width (PW)  $\leq 1 \mu\text{s}$ , 300 pps

Note 2: Exponential waveform. Pulse width  $\leq 2 \mu\text{s}$ ,  $f \leq 15 \text{ kHz}$

Note 3:  $\geq 2 \text{ mm}$  below seating plane.

Note 4: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

## 8. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Input on-state current	$I_{F(ON)}$	(Note 1)	6.5	—	15	mA
Input off-state voltage	$V_{F(OFF)}$		0	—	0.8	V
Supply voltage	$V_{CC}$	(Note 2)	10	—	30	
Peak high-level output current	$I_{OPH}$		—	—	-0.2	A
Peak low-level output current	$I_{OPL}$		—	—	+0.2	
Operating frequency	$f$	(Note 3)	—	—	25	kHz

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performance of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note: A ceramic capacitor (0.1  $\mu\text{F}$ ) should be connected between pin 6 and pin 4 to stabilize the operation of a high-gain linear amplifier. Otherwise, this photocoupler may not switch properly. The bypass capacitor should be placed within 1 cm of each pin.

Note 1: The rise and fall times of the input on-current should be less than 0.5  $\mu\text{s}$ .

Note 2: Denotes the operating range, not the recommended operating condition.

Note 3: Exponential waveform.  $I_{OPH} \geq -0.3 \text{ A}$  ( $\leq 2.0 \mu\text{s}$ ),  $I_{OPL} \leq 0.3 \text{ A}$  ( $\leq 2.0 \mu\text{s}$ ),  $T_a = 100^\circ\text{C}$

## 9. Electrical Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $100^\circ\text{C}$ )

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	$V_F$		—	$I_F = 10 \text{ mA}$ , $T_a = 25^\circ\text{C}$	1.40	1.57	1.80	V
Input forward voltage temperature coefficient	$\Delta V_F / \Delta T_a$		—	$I_F = 10 \text{ mA}$	—	-1.8	—	mV/ $^\circ\text{C}$
Input reverse current	$I_R$		—	$V_R = 5 \text{ V}$ , $T_a = 25^\circ\text{C}$	—	—	10	$\mu\text{A}$
Input capacitance	$C_t$		—	$V = 0 \text{ V}$ , $f = 1 \text{ MHz}$ , $T_a = 25^\circ\text{C}$	—	60	—	pF
Peak high-level output current	$I_{OPH}$	(Note 1)	Fig. 12.1.1	$I_F = 5 \text{ mA}$ , $V_{CC} = 15 \text{ V}$ , $V_{6-5} = 4 \text{ V}$	—	-0.38	-0.2	A
				$I_F = 5 \text{ mA}$ , $V_{CC} = 15 \text{ V}$ , $V_{6-5} = 10 \text{ V}$	—	-0.6	-0.4	
Peak low-level output current	$I_{OPL}$	(Note 1)	Fig. 12.1.2	$I_F = 0 \text{ mA}$ , $V_{CC} = 15 \text{ V}$ , $V_{5-4} = 2 \text{ V}$	0.2	0.36	—	A
				$I_F = 0 \text{ mA}$ , $V_{CC} = 15 \text{ V}$ , $V_{5-4} = 10 \text{ V}$	0.4	0.62	—	
High-level output voltage	$V_{OH}$		Fig. 12.1.3	$I_F = 5 \text{ mA}$ , $V_{CC} = 10 \text{ V}$ , $I_O = -100 \text{ mA}$	6.0	8.5	—	V
Low-level output voltage	$V_{OL}$		Fig. 12.1.4	$V_F = 0.8 \text{ V}$ , $V_{CC} = 10 \text{ V}$ , $I_O = 100 \text{ mA}$	—	0.4	1.0	V
High-level supply current	$I_{CCH}$		Fig. 12.1.5	$I_F = 10 \text{ mA}$ , $V_{CC} = 10$ to $30 \text{ V}$ , $V_O = \text{Open}$	—	1.4	2.0	mA
Low-level supply current	$I_{CCL}$		Fig. 12.1.6	$I_F = 0 \text{ mA}$ , $V_{CC} = 10$ to $30 \text{ V}$ , $V_O = \text{Open}$	—	1.3	2.0	
Threshold input current (L/H)	$I_{FLH}$		—	$V_{CC} = 15 \text{ V}$ , $V_O > 1 \text{ V}$	—	2.5	5	V
Threshold input voltage (H/L)	$V_{FHL}$		—	$V_{CC} = 15 \text{ V}$ , $V_O < 1 \text{ V}$	0.8	—	—	
Supply voltage	$V_{CC}$		—	—	10	—	30	V

Note: All typical values are at  $T_a = 25^\circ\text{C}$ .

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors.

Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1:  $I_O$  application time  $\leq 50 \mu\text{s}$ , single pulse.

## 10. Isolation Characteristics (Unless otherwise specified, $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Note	Test Conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	$C_S$	(Note 1)	$V_S = 0 \text{ V}$ , $f = 1 \text{ MHz}$	—	1.0	—	pF
Isolation resistance	$R_S$	(Note 1)	$V_S = 500 \text{ V}$ , R.H. $\leq 60 \%$	$10^{12}$	$10^{14}$	—	$\Omega$
Isolation voltage	$BV_S$	(Note 1)	AC, 60 s	5000	—	—	Vrms

Note 1: This device is considered as a two-terminal device: Pins 1, 2 and 3 are shorted together, and pins 4, 5 and 6 are shorted together.

## 11. Switching Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to $100^\circ\text{C}$ )

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	$t_{pLH}$	(Note 1)	Fig. 12.1.7	$I_F = 0 \rightarrow 5 \text{ mA}$ , $V_{CC} = 30 \text{ V}$ , $R_g = 47 \Omega$ , $C_g = 3 \text{ nF}$	30	—	500	ns
Propagation delay time (H/L)	$t_{pHL}$	(Note 1)		$I_F = 5 \rightarrow 0 \text{ mA}$ , $V_{CC} = 30 \text{ V}$ , $R_g = 47 \Omega$ , $C_g = 3 \text{ nF}$	30	—	500	
Rise time	$t_r$	(Note 1)		$I_F = 0 \rightarrow 5 \text{ mA}$ , $V_{CC} = 30 \text{ V}$ , $R_g = 47 \Omega$ , $C_g = 3 \text{ nF}$	—	50	—	
Fall time	$t_f$	(Note 1)		$I_F = 5 \rightarrow 0 \text{ mA}$ , $V_{CC} = 30 \text{ V}$ , $R_g = 47 \Omega$ , $C_g = 3 \text{ nF}$	—	50	—	
Pulse width distortion	$ t_{pHL} - t_{pLH} $	(Note 1)		$I_F = 0 \leftrightarrow 5 \text{ mA}$ , $V_{CC} = 30 \text{ V}$ , $R_g = 47 \Omega$ , $C_g = 3 \text{ nF}$	—	—	350	
High-level common-mode transient immunity	$CM_H$	(Note 2)	Fig. 12.1.8	$V_{CM} = 1000 V_{p-p}$ , $I_F = 5 \text{ mA}$ , $V_{CC} = 30 \text{ V}$ , $T_a = 25^\circ\text{C}$ , $V_{O(min)} = 26 \text{ V}$	$\pm 20$	$\pm 25$	—	kV/ $\mu\text{s}$
Low-level common-mode transient immunity	$CM_L$	(Note 3)		$V_{CM} = 1000 V_{p-p}$ , $I_F = 0 \text{ mA}$ , $V_{CC} = 30 \text{ V}$ , $T_a = 25^\circ\text{C}$ , $V_{O(max)} = 1 \text{ V}$	$\pm 20$	$\pm 25$	—	

Note: All typical values are at  $T_a = 25^\circ\text{C}$ .

Note 1: Input signal (  $f = 25 \text{ kHz}$ , duty = 50 %,  $t_r = t_f = 5 \text{ ns}$  or less ).

$C_L$  is less than 15 pF which includes probe and stray wiring capacitance.

Note 2:  $CM_H$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state ( $V_O > 26 \text{ V}$ ).

Note 3:  $CM_L$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O < 1 \text{ V}$ ).

Not Recommended for New Design

## 12. Test Circuits and Characteristics Curves

### 12.1. Test Circuits

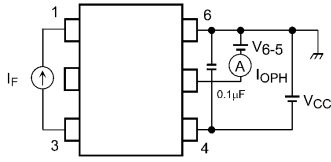


Fig. 12.1.1  $I_{OPH}$  Test Circuit

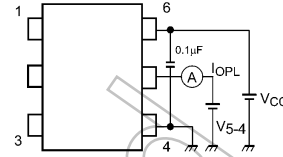
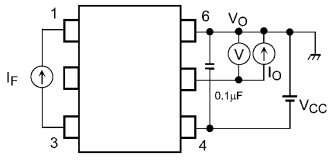


Fig. 12.1.2  $I_{OPL}$  Test Circuit



\* $V_{OH} = V_{CC} - V_O$

Fig. 12.1.3  $V_{OH}$  Test Circuit

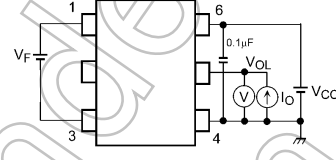


Fig. 12.1.4  $V_{OL}$  Test Circuit

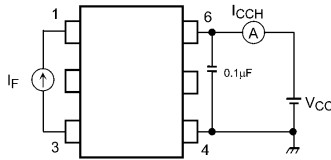


Fig. 12.1.5  $I_{CCH}$  Test Circuit

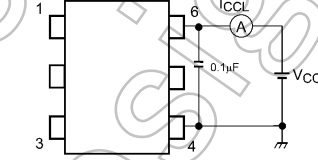
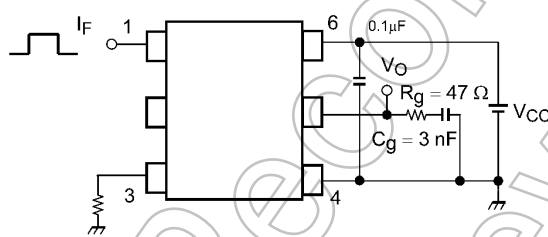


Fig. 12.1.6  $I_{CCL}$  Test Circuit

$I_F = 5 \text{ mA (P.G.)}$   
 $(f = 25 \text{ kHz, duty} = 50\%, t_r = t_f = 5 \text{ ns or less})$



P.G.: Pulse Generator

Fig. 12.1.7 Switching Time Test Circuit and Waveform

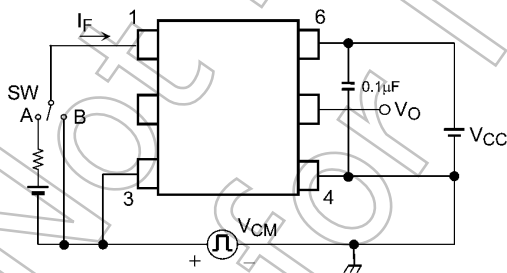
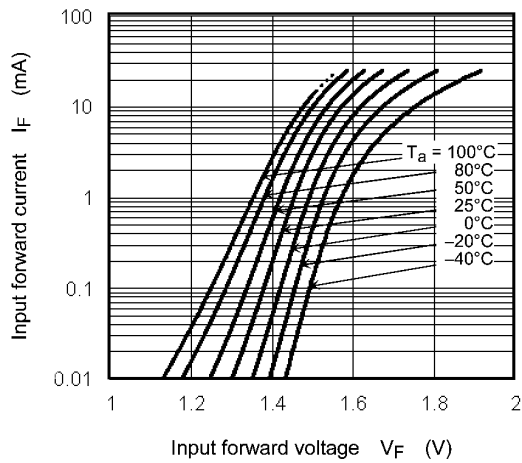
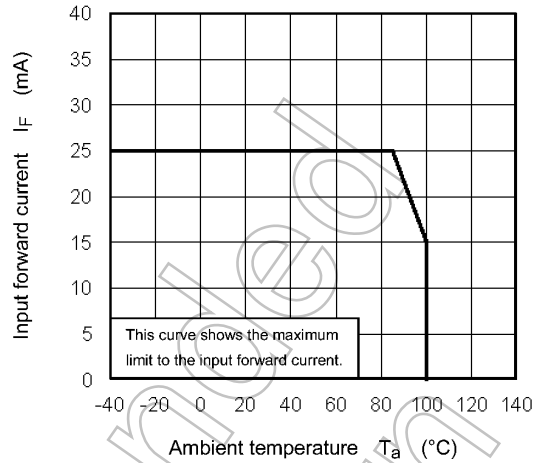


Fig. 12.1.8 Common-Mode Transient Immunity Test Circuit and Waveform

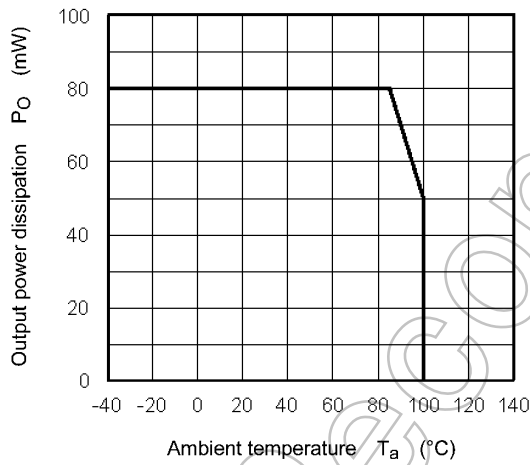
## 12.2. Characteristics Curves (Note)



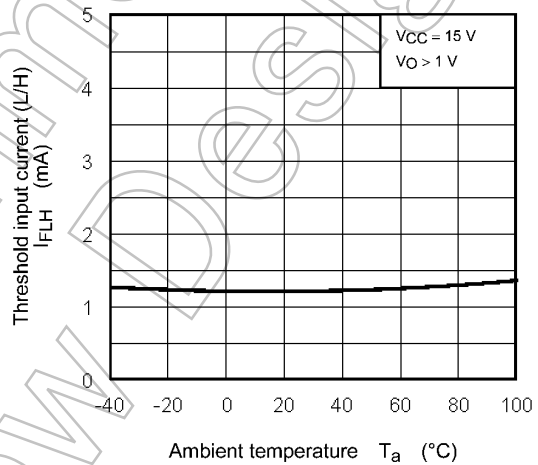
**Fig. 12.2.1**  $I_F - V_F$



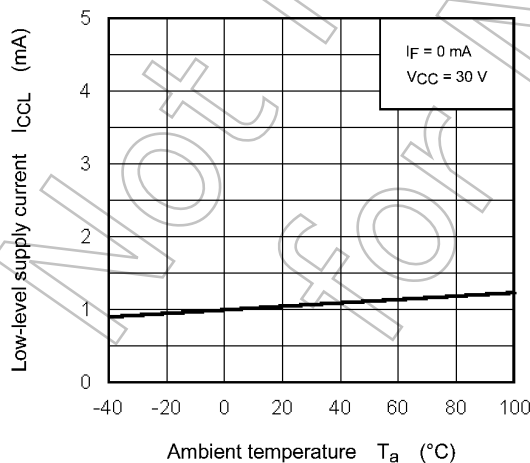
**Fig. 12.2.2**  $I_F - T_a$



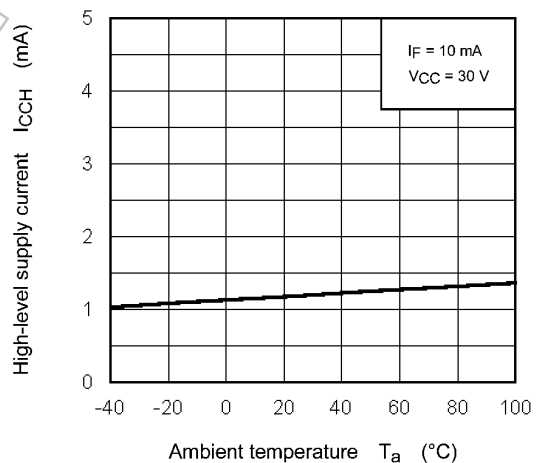
**Fig. 12.2.3**  $P_O - T_a$



**Fig. 12.2.4**  $I_{FLH} - T_a$



**Fig. 12.2.5**  $I_{CCL} - T_a$



**Fig. 12.2.6**  $I_{CCH} - T_a$

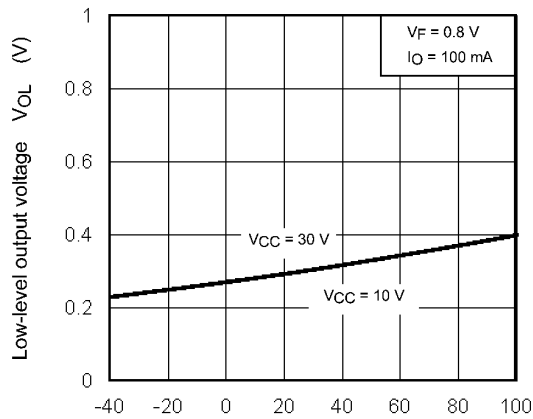


Fig. 12.2.7  $V_{OL} - T_a$

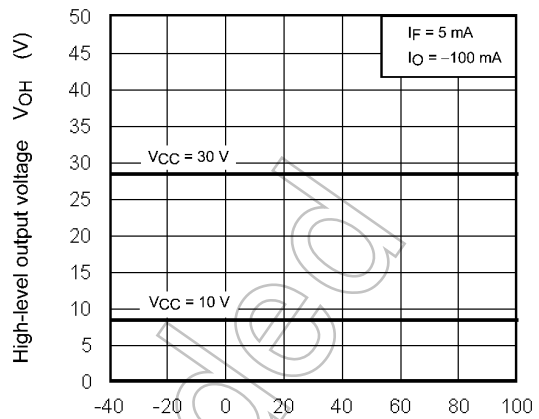


Fig. 12.2.8  $V_{OH} - T_a$

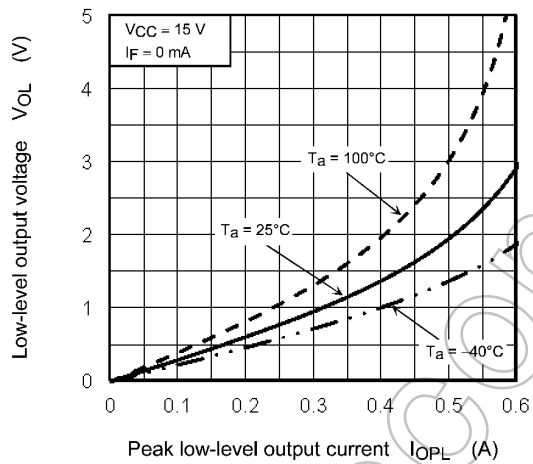


Fig. 12.2.9  $V_{OL} - I_{OPL}$

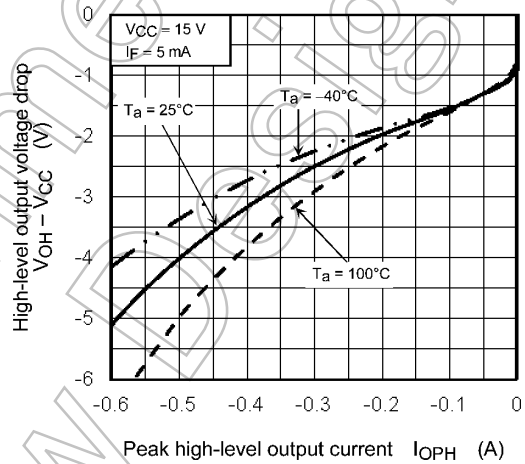


Fig. 12.2.10  $(V_{OH} - V_{CC}) - I_{OPH}$

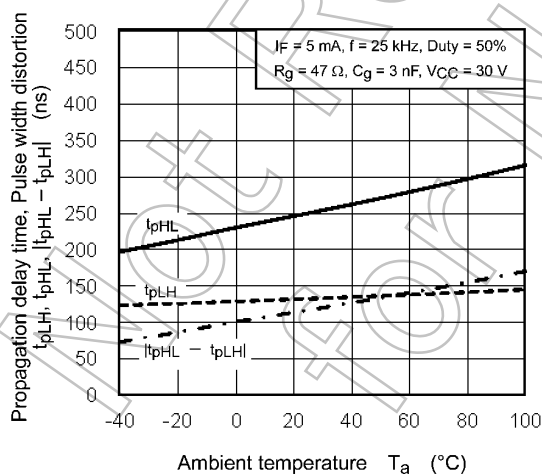


Fig. 12.2.11  $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - T_a$

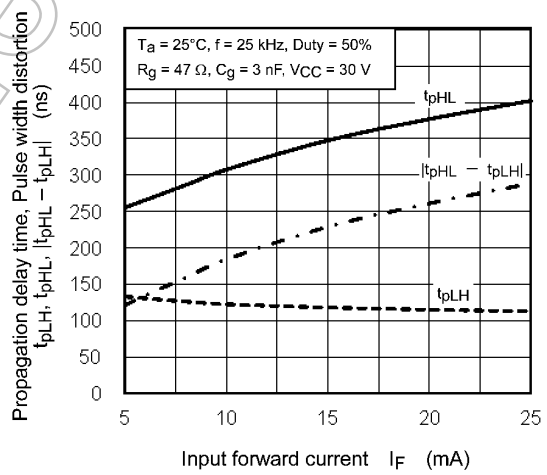
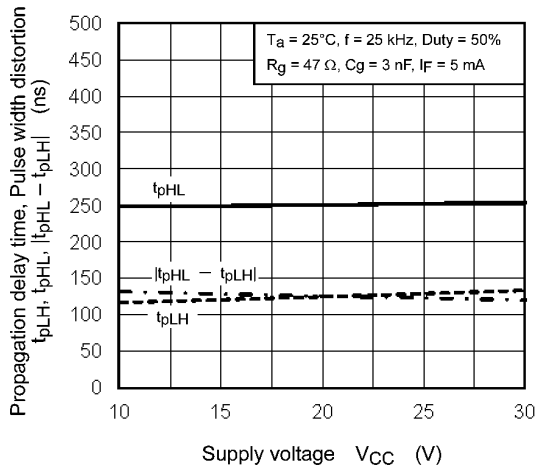


Fig. 12.2.12  $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - I_F$





**Fig. 12.2.13**  $t_{pLH}, t_{pHL}, |t_{pHL} - t_{pLH}| - V_{CC}$

NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Not Recommended for New Design

## 13. Soldering and Storage

### 13.1. Precautions for Soldering

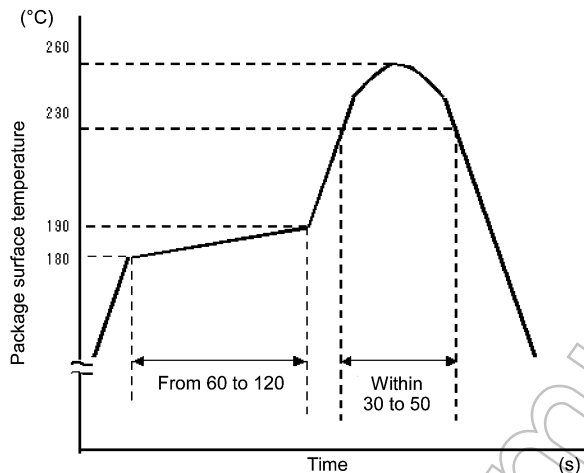
The soldering temperature should be controlled as closely as possible to the conditions shown below, irrespective of whether a soldering iron or a reflow soldering method is used.

- When using soldering reflow.

The soldering temperature profile is based on the package surface temperature.  
(See the figure shown below, which is based on the package surface temperature.)

Reflow soldering must be performed once or twice.

The mounting should be completed with the interval from the first to the last mountings being 2 weeks.



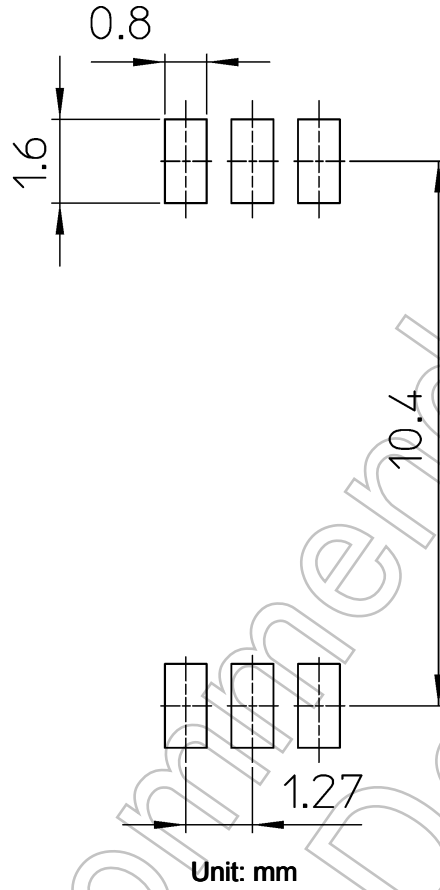
**Fig. 13.1.1 An Example of a Temperature Profile When Lead(Pb)-free Solder Is Used**

- When using soldering flow  
Preheat the device at a temperature of 150 °C (package surface temperature) for 60 to 120 seconds.  
Mounting condition of 260 °C within 10 seconds is recommended.  
Flow soldering must be performed once.
- When using soldering Iron  
Complete soldering within 10 seconds for lead temperature not exceeding 260 °C or within 3 seconds not exceeding 350 °C  
Heating by soldering iron must be done only once per lead.

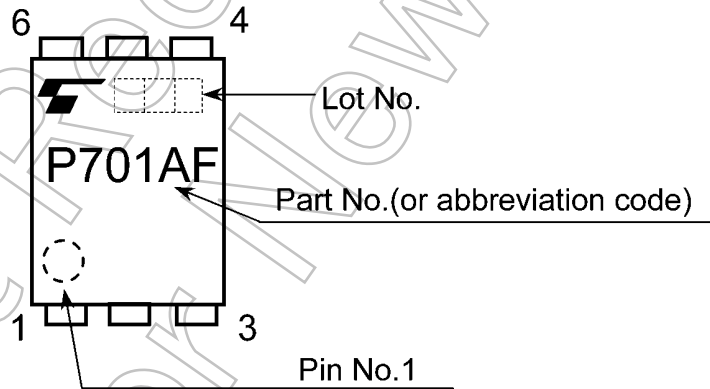
### 13.2. Precautions for General Storage

- Avoid storage locations where devices may be exposed to moisture or direct sunlight.
- Follow the precautions printed on the packing label of the device for transportation and storage.
- Keep the storage location temperature and humidity within a range of 5°C to 35°C and 45% to 75%, respectively.
- Do not store the products in locations with poisonous gases (especially corrosive gases) or in dusty conditions.
- Store the products in locations with minimal temperature fluctuations. Rapid temperature changes during storage can cause condensation, resulting in lead oxidation or corrosion, which will deteriorate the solderability of the leads.
- When restoring devices after removal from their packing, use anti-static containers.
- Do not allow loads to be applied directly to devices while they are in storage.
- If devices have been stored for more than two years under normal storage conditions, it is recommended that you check the leads for ease of soldering prior to use.

## 14. Land Pattern Dimensions for Reference Only



## 15. Marking



### 16. EN60747-5-5 Option (D4) Specification

- Part number: TLP701A, TLP701AF (**Note 1**)
- The following part naming conventions are used for the devices that have been qualified according to option (D4) of EN 60747.

Example: TLP701A(D4-TP,F)

D4: EN 60747 option

TP: Tape type

F: [[G]]/RoHS COMPATIBLE (**Note 2**)

Note: Use TOSHIBA standard type number for safety standard application.



e.g., TLP701A(D4-TP,F) → TLP701A

Note 1: Please contact your Toshiba sales representative for details on environmental information such as the product's RoHS compatibility.

RoHS is the Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronics equipment.

Description		Symbol	Rating	Unit
Application classification			I-IV I-III	—
for rated mains voltage ≤ 300 Vrms for rated mains voltage ≤ 600 Vrms				
Climatic classification			40 / 100 / 21	—
Pollution degree			2	—
Maximum operating insulation voltage	TLPxxx type	V <sub>IORM</sub>	890	V <sub>peak</sub>
	TLPxxxF type		1140	
Input to output test voltage, Method A V <sub>pr</sub> = 1.6 × V <sub>IORM</sub> , type and sample test t <sub>p</sub> = 10 s, partial discharge < 5 pC	TLPxxx type	V <sub>pr</sub>	1424	V <sub>peak</sub>
	TLPxxxF type		1824	
Input to output test voltage, Method B V <sub>pr</sub> = 1.875 × V <sub>IORM</sub> , 100 % production test t <sub>p</sub> = 1 s, partial discharge < 5 pC	TLPxxx type	V <sub>pr</sub>	1670	V <sub>peak</sub>
	TLPxxxF type		2140	
Highest permissible overvoltage (transient overvoltage, t <sub>pr</sub> = 60 s)		V <sub>TR</sub>	8000	V <sub>peak</sub>
Safety limiting values (max. permissible ratings in case of fault, also refer to thermal derating curve)				
current (input current I <sub>F</sub> , P <sub>so</sub> = 0)		I <sub>si</sub>	300	mA
power (output or total power dissipation)		P <sub>so</sub>	700	mW
temperature		T <sub>s</sub>	150	°C
Insulation resistance	V <sub>IO</sub> = 500 V, T <sub>a</sub> = 25 °C V <sub>IO</sub> = 500 V, T <sub>a</sub> = 100 °C V <sub>IO</sub> = 500 V, T <sub>a</sub> = T <sub>s</sub>	R <sub>si</sub>	≥ 10 <sup>12</sup> ≥ 10 <sup>11</sup> ≥ 10 <sup>9</sup>	Ω

Fig. 16.1 EN 60747 Isolation Characteristics

		 7.62-mm pitch TLPxxx type	 10.16-mm pitch TLPxxxF type
Minimum creepage distance	Cr	7.0 mm	8.0 mm
Minimum clearance	Cl	7.0 mm	8.0 mm
Minimum insulation thickness	ti	0.4 mm	
Comparative tracking index	CTI	175	

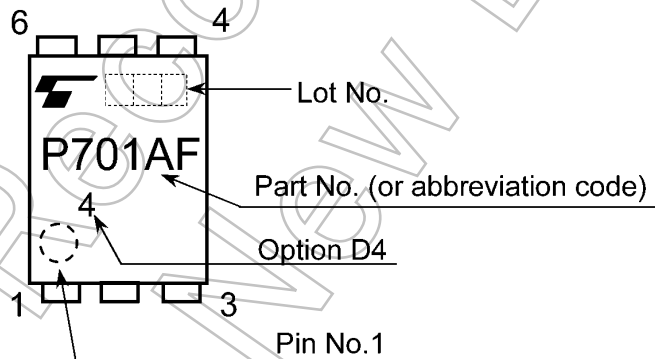
**Fig. 16.2 Insulation Related Specifications (Note)**

Note: If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value. (e. g., at a standard distance between soldering eye centers of 7.5 mm). If this is not permissible, the user shall take suitable measures.

Note: This photocoupler is suitable for **safe electrical isolation** only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.



**Fig. 16.3 Marking on Packing**



**Fig. 16.4 Marking Example (Note)**

Note: The above marking is applied to the photocouplers that have been qualified according to option (D4) of EN 60747.

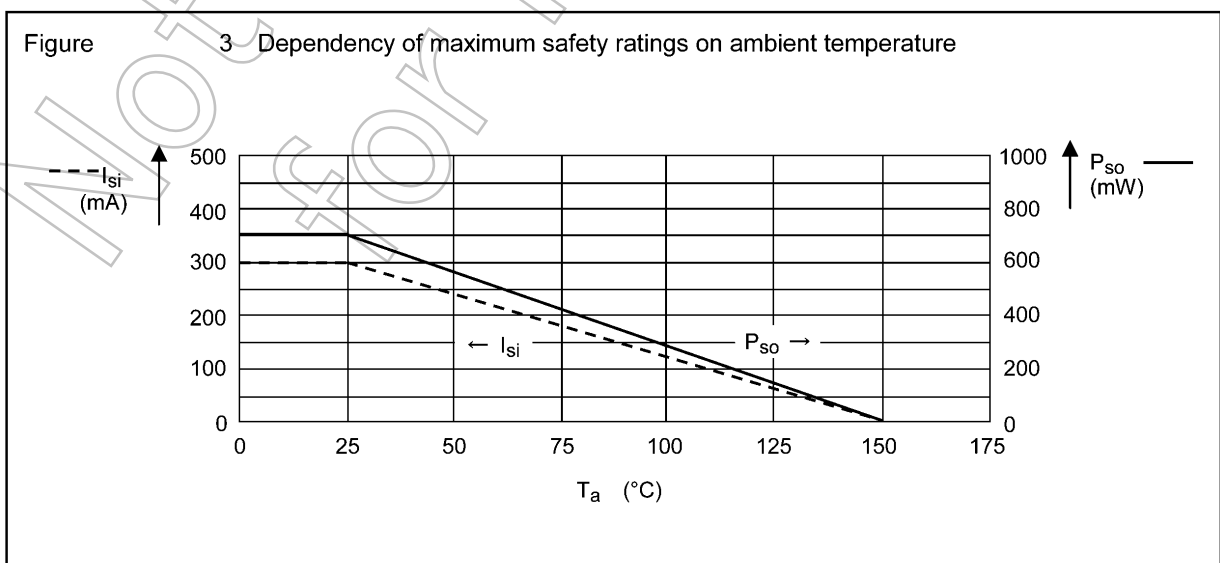
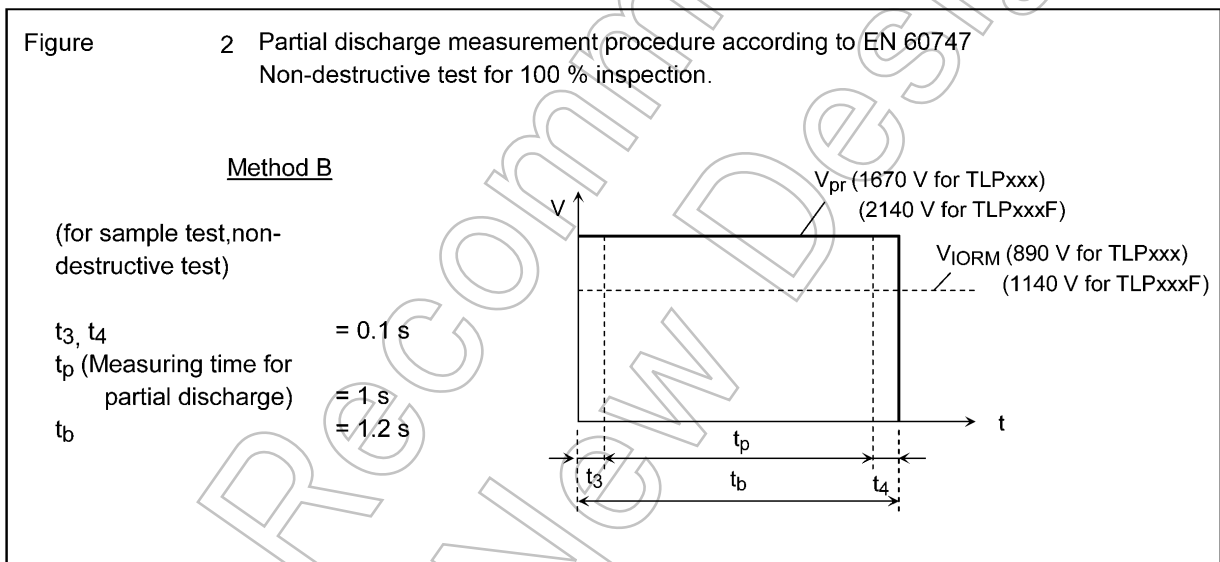
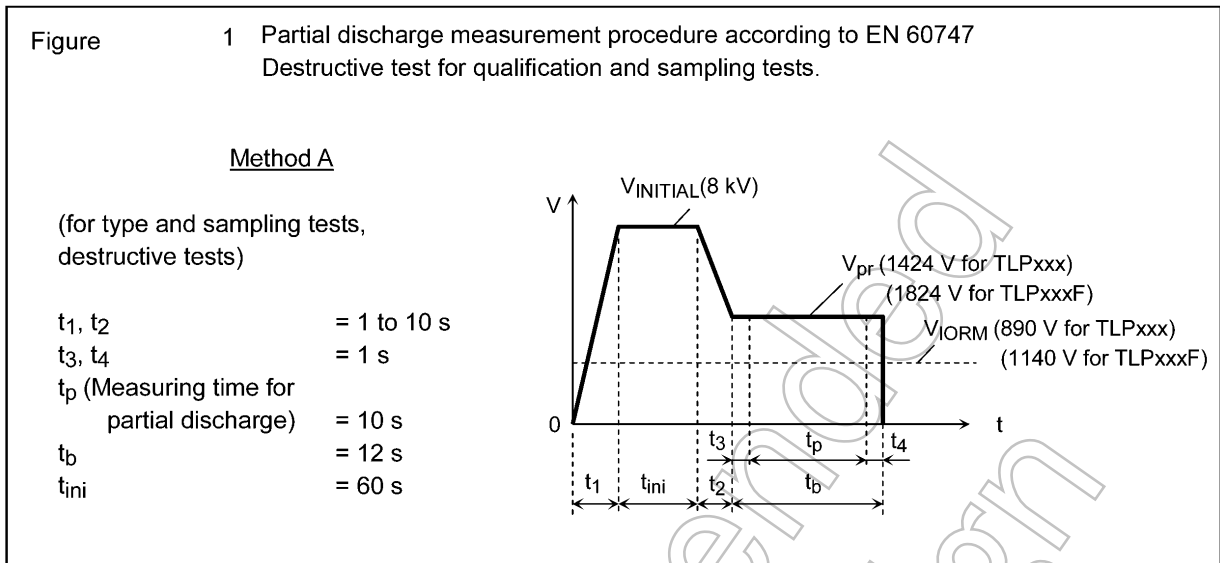
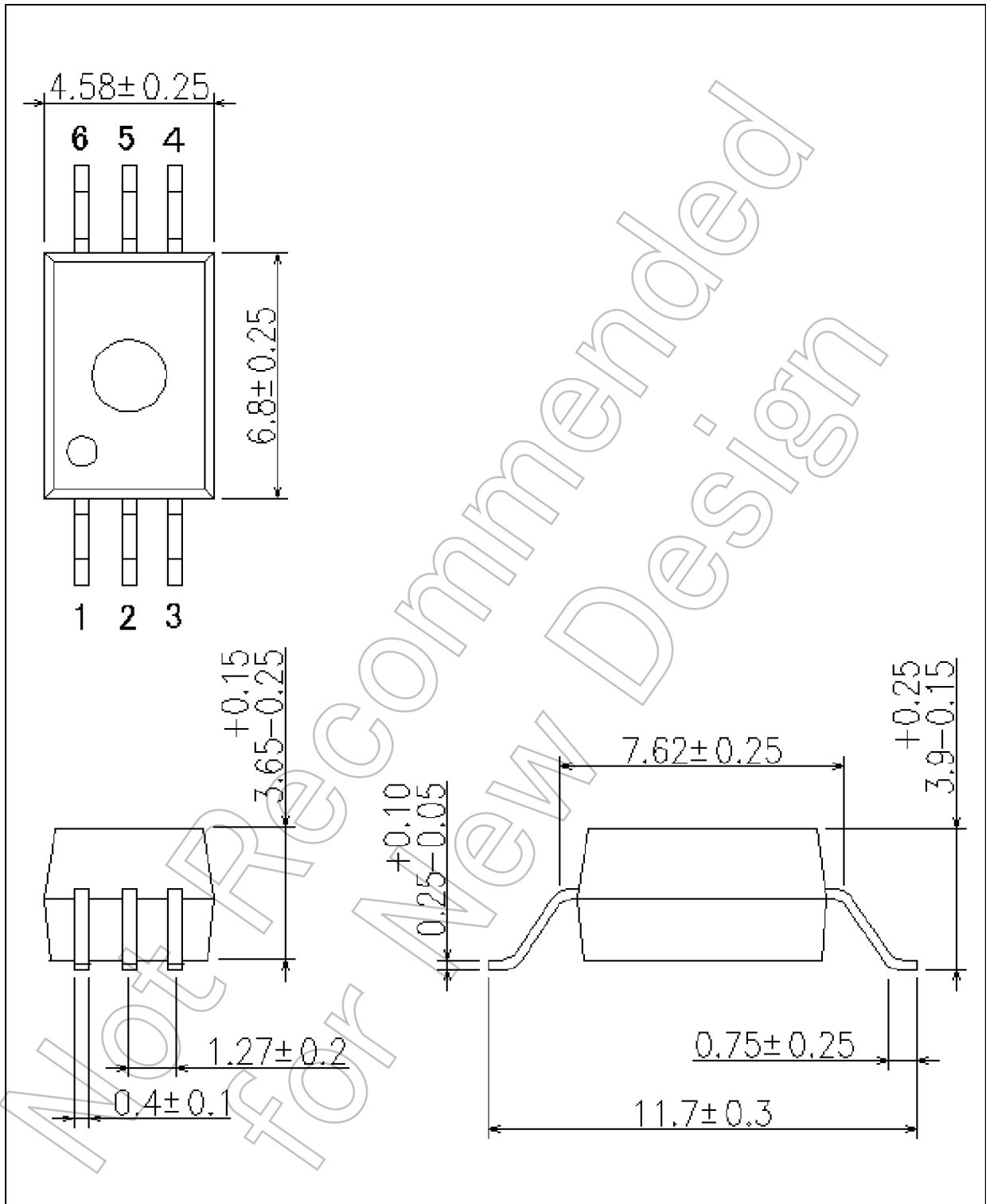


Fig. 16.5 Measurement Procedure

## Package Dimensions

Unit: mm



Weight: 0.26 g (typ.)

Package Name(s)
TOSHIBA: 11-5J101S

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