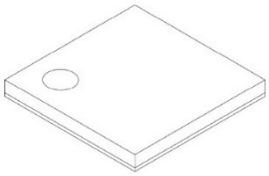
CMOS Digital Integrated Circuit Silicon Monolithic

TC358770AXBG/TC358777XBG

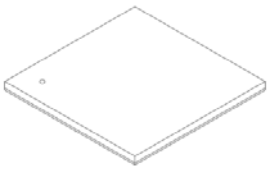
Mobile Peripheral Devices

TC358770AXBG



P-VFBGA100-0505-0.40-001
Weight: 40 mg (Typ.)

TC358777XBG



P-VFBGA80-0707-0.65-001
Weight: 65 mg (Typ.)

Overview

This Functional Specification defines operation of TC358770AXBG / TC358777XBG chip, which concatenates two DSI streams of video packets, one from each DSI link into a single DisplayPort™ video stream.

The only difference between TC358770AXBG and TC3587777XBG is the package size. TC358770AXBG housed in a 5.0 mm by 5.0 mm size package with 0.4 mm ball pitch. While TC358777XBG housed in a 7.0 mm by 7.0 mm size package with 0.65 mm ball pitch.

TC358770AXBG / TC358777XBG exhibits two independent 4-data lane DSI receivers and one 4-lane DisplayPort transmitter. Each DSI link data lane can receive data up to 1 Gbps/lane, with up to 8 Gbps total input data rate. Each DSI receiver link can activate 0-, 1-, 2-, 3- or 4-data lanes independently. DP main link can toggle bit rate at either 1.62 or 2.7 Gbps per lane, with maximum output data rate at 8.64 Gbps. DP transmitter is able to operate with 1-, 2 or 4-lanes in its main link.

The target application is for high resolution DisplayPort panels, whose bandwidth requirement cannot be met by a single 4-data lane DSI link @4 Gbps. TC358770AXBG is an ideal bridge chip which enables application processors, or hosts, with dual DSI links to drive up to 2560 x 2048 x 24 (or 18) DisplayPort panels @60fps.

Features

- TC358770AXBG / TC358777XBG follows the following standards:
  - ✧ MIPI® DSI version 1.02, Jan 2010.
  - ✧ MIPI® D-PHY version 1.0, May 2009.
  - ✧ VESA DisplayPort™ Standard version 1.1a, Jan. 11 2008.
  - ✧ Digital Content Protection LLC, HDCP version 1.3 with DisplayPort™ amendment revision 1.1, Jan. 15 2010.
- DSI Receiver
  - ✧ Dual 4-Data Lane DSI Link with Bi-direction support at Data Lane 0, it can be used in 1-, 2-, 3- or 4-data lane configuration.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Video input data formats: RGB-565, RGB-666 and RGB-888.
  - ✧ New DSI V1.02 Data Type, 16-bit YCbCr 422, is supported.
  - ✧ Interlaced video mode is not supported.
  - ✧ Provide path for DSI host/transmitter to control TC358770AXBG / TC358777XBG and its attached panel.
  - ✧ DSI Link High Speed clock, DSIClk or an external clock, RefClk, is required before programming TC358770AXBG.
- DisplayPort™ Source/Transmitter
  - ✧ VESA DisplayPort™ Rev 1.1a Standard.
    - Bit Rate @ 1.62 or 2.7 Gbps, Voltage Swing @0.4, 0.6, 0.8 or 1.2 V, Pre-Emphasis Level @0, 3.5 or 6dB.
    - There are four lanes available in DP main Link, which can operate in 1-, 2- or 4-lane configuration.
    - AUX channel with nominal bit rate at 1 Mbps.
  - ✧ After receiving DSI link burst data, TC358770AXBG / TC358777XBG retimes video data to DP panel's pixel clock for Synchronous (to DisplayPort™ link symbol clock, LSClk) Clock Mode operation.
  - ✧ SSCG with up to 30 kHz modulation to reduce EMI.
  - ✧ Built in PRBS7 Generator to test DisplayPort™ Link without DSI input.
  - ✧ Built in Color Bar Generator to verify DisplayPort™ protocol.
  - ✧ Support HDCP encryption Version 1.3 with DisplayPort™ amendment Revision 1.1.
  - ✧ Secure ASSR (Alternate Scrambler Seed Reset) support for eDP panels
    - System designer connects ASSR_DisablePad to an inner ring VSS_IO pad, e.g. pad E4, to enable eDP panels and ASSR

- Drive ASSR_DisablePad with an inner ring VDDS pad, e.g. pad D5, for using DP panels and disable ASSR
- System software read Revision ID field, 0x0500[7:0]:
  - ➢ 0x01 indicates eDP panels are used, DPCD register bit 0x0010A[0] of eDP panel should be set.
  - ➢ 0x03 assumes DP panels are connected, DPCD register bit 0x0010A[0] of DP panel should Not be set.

● I²C Slave Port
- ✧ Support for normal (100 kHz), fast (400 kHz) and ultra fast modes (2 MHz, depending on SysClk frequency).
- ✧ External I²C master can access TC358770AXBG / TC358777XBG internal registers via this port.
- ✧ Address auto increment is supported.
- ✧ TC358770AXBG / TC358777XBG Slave Port address is 0x68, (binary 1101_000x) where x = 1 for read and x = 0 for write. The slave address can be changed to 0x0F (binary 0001_111x) by tying pin SPI_SS/I2C_ADR_SEL to high.

● SPI Slave Interface
- ✧ Slave select pin supported.
- ✧ Clock Polarity and Phase as per SPI MODE0 (polarity = 0, phase = 0).
- ✧ Transfer Frame size of 48 bits.
- ✧ Maximum clock speed is up to 30 MHz.

● Audio Interface
- ✧ Support either I2S or TDM (Time Division Multiplex) mode.
- ✧ TDM mode can support 2, 4, 6 and 8 channel of audio data.
- ✧ Support 16, 18, 20 or 24-bit PCM audio data word.
- ✧ Sample frequency, fs, supported: 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
- ✧ 512 * fs audio oversample clock is required to generate accurate auido clock timestamps in order for the DisplayPort™ panel to recover audio clock correctly.
- ✧ Ability to insert IEC60958 status bits and preamble bits per channel.

● Operation
- ✧ Host programs TC358770AXBG / TC358777XBG either by using DSI link 0(DSI0), I²C bus or SPI bus.
- ✧ TC358770AXBG / TC358777XBG provides "mailbox registers," 20-bit AuxAddr and 16-byte AuxData, for Host to access DisplayPort™ Panel's DisplayPort™ Configuration Data, DPCD, registers.
- ✧ Host splits a video line data into two streams of DSI video packets. Host has two options to split the video line data:
  - Left-Right Side: Left (first) side video packet goes to DSI0 and Right side data to DSI1.
  - Even-Odd Group: Even (first) groups of pixels are transmitted in DSI0 while Odd ones are carried by DSI1.
    - ➢ The number of pixels per group is programmable; from 1 to 64.
    - ➢ The number of pixels per group and/or the number of groups in each video packet can be different between the two DSI links. This feature in connection with TC358770AXBG's capability to support configurable number of data lanes.
  - It is recommended that host pack the split video line data into one video packet for each DSI link before transmitting. However, TC358770AXBG / TC358777XBG supports multiple DSI packets per horizontal line time as long as DSI link bandwidth is enough for the overhead.
- ✧ TC358770AXBG / TC358777XBG is responsible to generate video frame timing based on the register values set by the Host. Host does not have to care/generate video horizontal timings, such as Horizontal Front/Back Porch and Horizontal Pulse width. Host is responsible to send the video data packets to TC358770AXBG / TC358777XBG in time line-by-line and separated each line data by HSS.
  - Host is expected to send exactly one line of video data per horizontal sync period between the two DSI links.
  - Host is expected to start HSS_0, HSS packet of DSI0, and HSS_1, HSS packet of DSI1, either at "the same time" or with fixed delay/skew between them (HSS_0 earlier than that of HSS_1).
    - ➢ "The same time" means within +/- 5 clock cycles.
  - The time skew between the two DSI links' Hsync Start, HSS, packet cannot drift more than one video line time within one video frame period.
    - ➢ Host is recommended to use the same clock source to generate both DSI link clocks in order to prevent these two clocks from drifting away.
    - ➢ Otherwise, clock sources with 50 ppm accuracy are required.
  - It is recommended that each DSI link sends HSS and video packets back-to-back. Host can insert variable length of blanking packet between HSS and video packets as long as the bandwidth is allowed.

✧ TC358770AXBG / TC358777XBG concatenates two (streams of) video packets, one (stream) from each DSI link, into a single DisplayPort™ video stream before transmitting it out to the panel.

● Clock Source:

✧ An external reference clock, RefClk, is used to drive PLLs for generating DisplayPort™'s stream/pixel clock, StrmClk/PixelClk, and Link Symbol Clock, LSClk.

- Support DisplayPort™ Synchronous (StrmClk and LSClk) Clock Mode.
- Allowed RefClk Frequency Value: 13, 19.2, 26, 38.4 MHz.

✧ Optionally, DSI DSIClk can be used/divided down to replace RefClk and drive PLLs used to generate the required clocks.

- The divisor, from DSI ByteClk, can be either
  - ➢ 3 $(115.2 \div 3 = 38.4)$
  - ➢ 4 $(104 \div 4 = 26)$
  - ➢ 5 $(96 \div 5 = 19.2)$
  - ➢ 9 $(117 \div 9 = 13)$

● Power Supply

✧ MIPI® D-PHY and DP PHY: 1.2 V

✧ Core: 1.2 V

✧ DP-PHY: 1.8 V

✧ I/O: 1.8 V to 3.3 V (all IO pins must be same power level)

✧ HPD Input Pad 3.3 V

● Power Consumption (Typical Condition)

✧ Sleep State, with RESX asserted

- 12 mW

✧ Typical Operation:

- 2560 × 1440 × 24@60fps
- Dual DSIRx, each link @3.7 Gbps
  - ➢ 31 mW for both Links
- Core
  - ➢ 165 mW
- DP Tx (2.7 Gbps Link speed @4 lanes, 0.4 V Swing without Pre-Emphasis)
  - ➢ 168.5 mW
- Total = 364.5 mW

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- MIPI is registered trademark of MIPI Alliance, Inc.
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REFERENCES

1. MIPI D-PHY, "MIPI Alliance Specification for D-PHY Version 1.00.00 14-May-2009"
2. MIPI Alliance Standard for DSI Version 1.02.00 – 28 June 2010
3. VESA DisplayPort Standard (Version 1, Revision 1a January 11, 2008)
4. VESA Embedded DisplayPort (eDP) Standard (Version 1.1 October 23, 2009)
5. Digital Content Protection LLC, HDCP (Version 1.3 with DisplayPort amendment Revision 1.1, Jan. 15 2010)
6. I^2C bus specification, version 2.1, January 2000, Philips Semiconductor

1. Introduction

This Functional Specification defines operation of TC358770AXBG / TC358777XBG chip, which concatenates two DSI streams of video packets, one from each DSI link into a single DisplayPort™ video stream.

The only difference between TC358770AXBG and TC3587777XBG is the package size. TC358770AXBG housed in a 5.0 mm by 5.0 mm size package with 0.4 mm ball pitch. While TC358777XBG housed in a 7.0 mm by 7.0 mm size package with 0.65 mm ball pitch.

TC358770AXBG / TC358777XBG exhibits two independent 4-data lane DSI receivers and one 4-lane DisplayPort™ transmitter. Each DSI link data lane can receive data up to 1 Gbps/lane, with up to 8 Gbps total input data rate. Each DSI receiver link can activate 0-, 1-, 2-, 3- or 4-data lanes independently. DP main link can toggle bit rate at either 1.62 or 2.7 Gbps per lane, with maximum output data rate at 8.64 Gbps. DP transmitter is able to operate with 1-, 2 or 4-lanes in its main link.

The target application is for high resolution DisplayPort™ panels, whose bandwidth requirement cannot be met by a single 4-data lane DSI link @4 Gbps. TC358770AXBG is an ideal bridge chip which enables application processors, or hosts, with dual DSI links to drive up to 2560 × 2048 × 24 (or 18) DisplayPort™ panels @60fps.

DSI host controls/configures TC358770AXBG / TC358777XBG chip by using DSI's Generic Long Write packets. TC358770AXBG / TC358777XBG provides mail box registers for host to control (command) DisplayPort™ panel's DisplayPort™ Configuration Data, DPCD, registers. After host writes to these mail box registers, TC358770AXBG starts Aux channel bus cycles to communicate with the DisplayPort™ panel. TC358770AXBG / TC358777XBG supports both Aux native mode and I^2C mapped mode.

TC358770AXBG / TC358777XBG supports bi-directional DSI link. Host can read TC358770AXBG's registers by using DSI's Generic Short Read (2 parameter) packets. The read data is returned to host via DSI's reverse direction Low Power packets in data lane 0. Host can also access the DPCD status registers of DisplayPort™ panel by issuing read commands via TC358770AXBG's mail box registers. The maximum read data length is limited to 8 bytes per DSI link read.

Host can also access TC358770AXBG's registers, and DP panel's DPCD registers, by using an I^2C bus by addressing TC358770AXBG's slave address 0x68 (1101_000x). Either an external reference clock, RefClk, or DSI link's high speed, HS, clock needs to toggle before programming TC358770AXBG. RefClk is limited to 13, 19.2, 26 or 38.4 MHz only.

TC358770AXBG / TC358777XBG exhibits a SPI slave port, which provides host as third path to program its registers. Since SPI port shares the same pins as those of I^2C's, only one slave port can be used by the Host. I^2C slave port is active by default, asserting input pin SPI_I2C activates SPI interface. Please tie the unused input pins to ground.

Audio interface can accept I2S or Time Domain Multiplex, TDM, type of audio data. This audio data is packed as Secondary Data Packets which are muxed with video stream before routing out to DP panel via DP's main link. Host needs to provide a 512 * fs, audio sample clock frequency, clock in order for the DisplayPort™ Panel to recover audio clock precisely.

This document assumes that both DSI links use the same clock source to generate DSI links timing. The unintentional clock skews due to two clock sources used to generate DSI links' timing is discussed in "2 Features."

The target system diagram and TC358770AXBG / TC358777XBG block diagram are shown in Figure 1.1 and Figure 1.2, respectively.

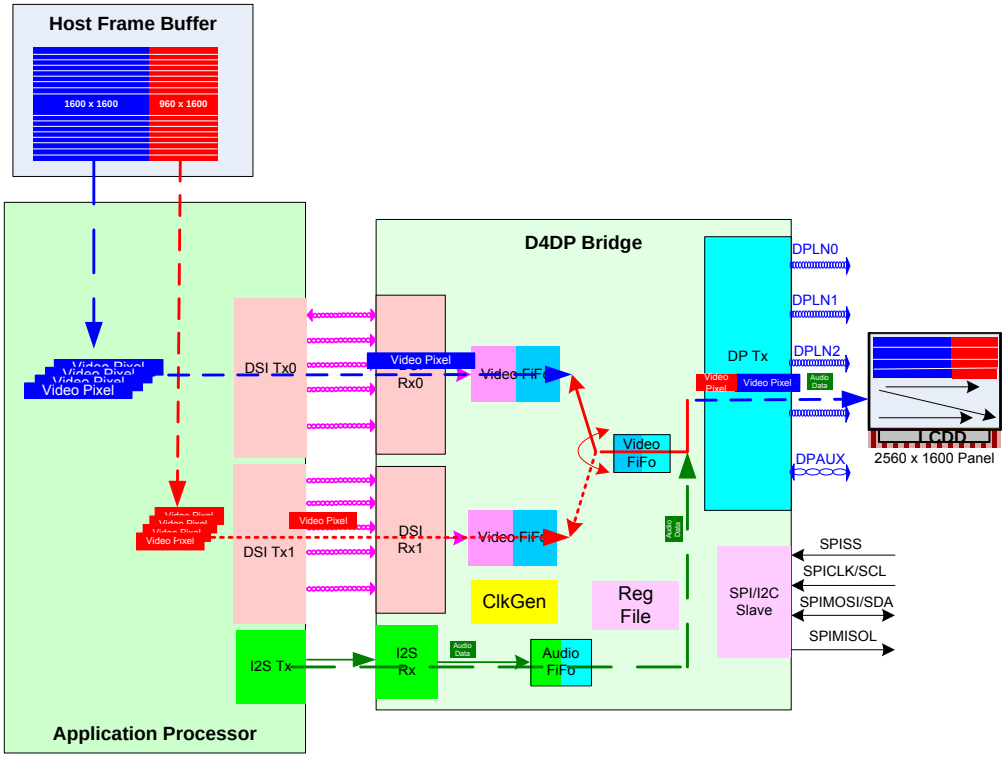


Figure 1.1 TC358770AXBG / TC358777XBG in System Application

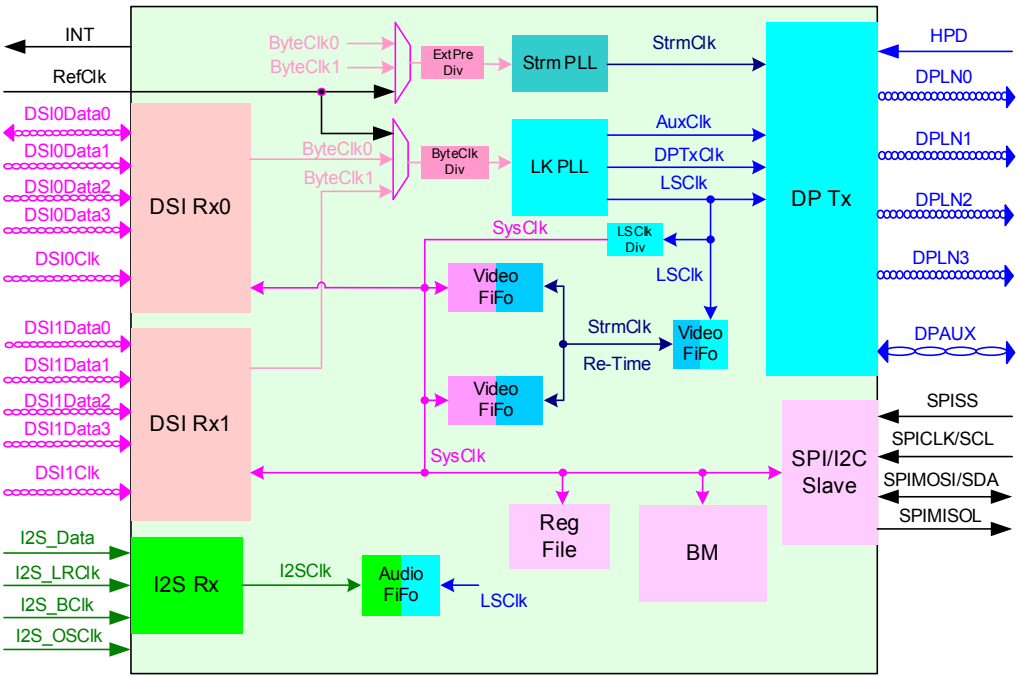


Figure 1.2 TC358770AXBG / TC358777XBG Block Diagram and Functional

2. Features

- TC358770AXBG / TC358777XBG follows the following standards**:**
  - ✧ MIPI® DSI version 1.02, Jan 2010.
  - ✧ MIPI® D-PHY version 1.0, May 2009.
  - ✧ VESA DisplayPortTM Standard version 1.1a, Jan. 11 2008.
  - ✧ Digital Content Protection LLC, HDCP version 1.3 with DisplayPortTM amendment revision 1.1, Jan. 15 2010.

- DSI Receiver
  - ✧ Dual 4-Data Lane DSI Link with Bi-direction support at Data Lane 0, it can be used in 1-, 2-, 3- or 4-data lane configuration.
  - ✧ Maximum speed at 1 Gbps/lane.
  - ✧ Video input data formats**:** RGB-565, RGB-666 and RGB-888.
  - ✧ New DSI V1.02 Data Type, 16-bit YCbCr 422, is supported.
  - ✧ Interlaced video mode is not supported.
  - ✧ Provide path for DSI host/transmitter to control TC358770AXBG / TC358777XBG and its attached panel.
  - ✧ DSI Link High Speed clock, DSIClk or an external clock, RefClk, is required before programming TC358770AXBG.

- DisplayPort™ Source/Transmitter
  - ✧ VESA DisplayPort™ Rev 1.1a Standard.
    - Bit Rate @ 1.62 or 2.7 Gbps, Voltage Swing @0.4, 0.6, 0.8 or 1.2 V, Pre-Emphasis Level @0, 3.5 or 6 dB.
    - There are four lanes available in DP main Link, which can operate in 1-, 2- or 4-lane configuration.
    - AUX channel with nominal bit rate at 1 Mbps.
  - ✧ After receiving DSI link burst data, TC358770AXBG / TC358777XBG retimes video data to DP panel's pixel clock for Synchronous (to DisplayPort™ link symbol clock, LSClk) Clock Mode operation.
  - ✧ SSCG with up to 30 kHz modulation to reduce EMI.
  - ✧ Built in PRBS7 Generator to test DisplayPortTM Link without DSI input.
  - ✧ Built in Color Bar Generator to verify DisplayPortTM protocol.
  - ✧ Support HDCP encryption Version 1.3 with DisplayPortTM amendment Revision 1.1.
  - ✧ Secure ASSR (Alternate Scrambler Seed Reset) support for eDP panels
    - System designer connects ASSR_DisablePad to an inner ring VSS_IO pad, e.g. pad E4, to enable eDP panels and ASSR
    - Drive ASSR_DisablePad with an inner ring VDDS pad, e.g. pad D5, for using DP panels and disable ASSR
    - System software read Revision ID field, 0x0500[7**:**0]**:**
      - ➢ 0x01 indicates eDP panels are used, DPCD register bit 0x0010A[0] of eDP panel should be set
      - ➢ 0x03 assumes DP panels are connected, DPCD register bit 0x0010A[0] of DP panel should Not be set

- I^2C Slave Port
  - ✧ Support for normal (100 kHz), fast (400 kHz) and ultra fast modes (2 MHz, depending on SysClk frequency).
  - ✧ External I^2C master can access TC358770AXBG / TC358777XBG internal registers via this port.
  - ✧ Address auto increment is supported.
  - ✧ TC358770AXBG / TC358777XBG Slave Port address is 0x68, (binary 1101_000x) where x = 1 for read and x = 0 for write. The slave address can be changed to 0x0F (binary 0001_111x) by tying pin SPI_SS/I2C_ADR_SEL to high.

- SPI Slave Interface
  - ✧ Slave select pin supported.
  - ✧ Clock Polarity and Phase as per SPI MODE0 (polarity = 0, phase = 0).
  - ✧ Transfer Frame size of 48 bits.
  - ✧ Maximum clock speed is up to 30 MHz.

- Audio Interface
  - ✧ Support either I2S or TDM (Time Division Multiplex) mode.
  - ✧ TDM mode can support 2, 4, 6 and 8 channel of audio data.
  - ✧ Support 16, 18, 20 or 24-bit PCM audio data word.
  - ✧ Sample frequency, fs, supported**:** 32, 44.1, 48, 88.2, 96, 176.4 & 192 kHz.
  - ✧ 512 * fs audio oversample clock is required to generate accurate auido clock timestamps in order for the DisplayPortTM panel to recover audio clock correctly.
  - ✧ Ability to insert IEC60958 status bits and preamble bits per channel.

- Operation
  - ✧ Host programs TC358770AXBG / TC358777XBG either by using DSI link 0 (DSI0), I^2C bus or SPI bus.
  - ✧ TC358770AXBG / TC358777XBG provides "mailbox registers," 20-bit AuxAddr and 16-byte AuxData, for Host to access DisplayPort™ Panel's DisplayPort™ Configuration Data, DPCD, registers.
  - ✧ Host splits a video line data into two streams of DSI video packets. Host has two options to split the video line data**:**
    - Left-Right Side**:** Left (first) side video packet goes to DSI0 and Right side data to DSI1.
    - Even-Odd Group**:** Even (first) groups of pixels are transmitted in DSI0 while Odd ones are carried by DSI1.
      - ➢ The number of pixels per group is programmable; from 1 to 64.
      - ➢ The number of pixels per group and/or the number of groups in each video packet can be different between the two DSI links. This feature in connection with TC358770AXBG's capability to support configurable number of data lanes.
    - It is recommended that host pack the split video line data into one video packet for each DSI link before transmitting. However, TC358770AXBG / TC358777XBG supports multiple DSI packets per horizontal line time as long as DSI link bandwidth is enough for the overhead.
  - ✧ TC358770AXBG / TC358777XBG is responsible to generate video frame timing based on the register values set by the Host. Host does not have to care/generate video horizontal timings, such as Horizontal Front/Back Porch and Horizontal Pulse width. Host is responsible to send the video data packets to TC358770AXBG / TC358777XBG in time line-by-line and separated each line data by HSS.
    - Host is expected to send exactly one line of video data per horizontal sync period between the two DSI links.
    - Host is expected to start HSS_0, HSS packet of DSI0, and HSS_1, HSS packet of DSI1, either at "the same time" or with fixed delay/skew between them (HSS_0earlier than that of HSS_1).
      - ➢ "The same time" means within +/- 5 clock cycles.
    - The time skew between the two DSI links' Hsync Start, HSS, packet cannot drift more than one video line time within one video frame period.
      - ➢ Host is recommended to use the same clock source to generate both DSI link clocks in order to prevent these two clocks from drifting away.
      - ➢ Otherwise, clock sources with 50 ppm accuracy are required.
    - It is recommended that each DSI link sends HSS and video packets back-to-back. Host can insert variable length of blanking packet between HSS and video packets as long as the bandwidth is allowed.
  - ✧ TC358770AXBG / TC358777XBG concatenates two (streams of) video packets, one (stream) from each DSI link, into a single DisplayPort™ video stream before transmitting it out to the panel.

- Clock Source:
  - ✧ An external reference clock, RefClk, is used to drive PLLs for generating DisplayPort™'s stream/pixel clock, StrmClk/PixelClk, and Link Symbol Clock, LSClk.
    - Support DisplayPort™ Synchronous (StrmClk and LSClk) Clock Mode.
    - Allowed RefClk Frequency Value: 13, 19.2, 26, 38.4 MHz.
  - ✧ Optionally, DSI DSIClk can be used/divided down to replace RefClk and drive PLLs used to generate the required clocks.
    - The divisor, from DSI ByteClk, can be either
      - ➢ 3 $(115.2 \div 3 = 38.4)$
      - ➢ 4 $(104 \div 4 = 26)$
      - ➢ 5 $(96 \div 5 = 19.2)$
      - ➢ 9 $(117 \div 9 = 13)$

- Power Supply
  - ✧ MIPI® D-PHY and DP PHY: 1.2 V
  - ✧ Core: 1.2 V
  - ✧ DP-PHY: 1.8 V
  - ✧ I/O: 1.8 V to 3.3 V (all IO pins must be same power level)
  - ✧ HPD Input Pad: 3.3 V

- Power Consumption (Typical Condition)
  - ✧ Sleep State, with RESX asserted
    - 12 mW
  - ✧ Typical Operation:
    - 2560 × 1440 × 24@60fps
    - Dual DSIRx, each link @3.7 Gbps
      - ➢ 31 mW for both Links
    - Core
      - ➢ 165 mW
    - DP Tx (2.7 Gbps Link speed @4 lanes, 0.4 V Swing without Pre-Emphasis)
      - ➢ 168.5 mW
    - Total = 364.5 mW
    - The breakdown of each power rail is shown in the table below

	VDD_DSI (1.2 V)	VDDC (1.2 V)	PLL9 (1.2 V)	DP_12 (1.2 V)	DP_18 (1.8 V)	DPA_18 (1.8 V)	VDDS (1.8 V)	Total Power	Unit
Typical Operation	25.84	153.23	2.27	50.87	56.99	2.69	0		mA
	31.01	162.28	2.73	61.05	102.58	4.84	0	364.5	mW
Power Down	0.1	3.8	0	2.1	0	2.7	0		mA
	0.12	4.56	0	2.52	0	4.86	0	12	mW

- Packaging
  - ✧ 10 × 10 BGA with 0.4 mm ball pitch
  - ✧ 5 × 5 mm^2

Note: Attention about ESD. This product is weak against ESD. Please handle it carefully.

3. External Pins

3.1. TC358770AXBG Pin Layout

The mapping of TC358770AXBG signals to the external pins is shown in the figure below.

A1 DSI0DM_0	A2 DSI0DP_0	A3 DSI1DM_3	A4 DSI1DM_2	A5 DSI1CM	A6 VDD_DSI12	A7 VSS_DSI	A8 DSI1DM_1	A9 DSI1DM_0	A10 TEST
B1 DSI0DM_1	B2 DSI0DP_1	B3 DSI1DP_3	B4 DSI1DP_2	B5 DSI1CP	B6 VSS_DSI	B7 VDD_DSI12	B8 DSI1DP_1	B9 DSI1DP_0	B10 VDDS
C1 VSS_DSI	C2 VDD_DSI12	C3 DIG_4	C4 DIG_3	C5 DIG_2	C6 DIG_1	C7 VSS_IO	C8 DIG_0	C9 RESX	C10 SPI_SCLK/ I2C_SCL
D1 DSI0CM	D2 DSI0CP	D3 VDDC	D4 VSSC	D5 VDDS	D6 SPI_SS	D7 SPI_MOSI/ I2C_SDA	D8 VPGM_1	D9 SPI_MISO	D10 I2S_OSCLK
E1 VDD_DSI12	E2 VSS_DSI	E3 SPI_I2C	E4 VSS_IO	E5 Disable_ ASSR	E6 DIG_5	E7 INT	E8 I2S_LRCLK	E9 I2S_BCLK	E10 I2S_DATA
F1 DSI0DM_2	F2 DSI0DP_2	F3 TM_CNT	F4 DIG_7	F5 DIG_8	F6 VSSC	F7 VDDC	F8 VPGM_0	F9 VSS_PLL9	F10 VDD_PLL912
G1 DSI0DM_3	G2 DSI0DP_3	G3 PREC_RES_0	G4 PREC_RES_1	G5 VSS_DP	G6 DIFF_SE	G7 HPD	G8 VSS_DP	G9 DPAUXP	G10 DPAUXM
H1 ATB_1	H2 VDD_PLL18	H3 VDD_PLL12	H4 VSS_PLL	H5 VDD_DP12	H6 VSS_DP	H7 VDD_DP12	H8 VDD_DP18	H9 VSS_DPA	H10 VDD_DPA18
J1 REFCLK	J2 VDD_DP12	J3 DPLNP_0	J4 VSS_DP	J5 DPLNP_1	J6 VDD_DP12	J7 DPLNP_2	J8 VSS_DP	J9 DPLNP_3	J10 VDD_DP18
K1 ATB_0	K2 VSS_DP	K3 DPLNM_0	K4 VDD_DP18	K5 DPLNM_1	K6 VSS_DP	K7 DPLNM_2	K8 VDD_DP18	K9 DPLNM_3	K10 VSS_DP

Figure 3.1 TC358770AXBG Chip Pin Layout (Top view)

3.2. TC358777XBG Pin Layout

The mapping of TC358777XBG signals to the external pins is shown in the figure below.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
DSI0DM_0	DSI0DP_0	VDD_DSI12	DSI1DM_3	DSI1DM_2	DSI1CM	VDD_DSI12	DSI1DM_1	DSI1DM_0	VDDIO
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
DSI0DM_1	DSI0DP_1	VSS	DSI1DP_3	DSI1DP_2	DSI1CP	VSS	DSI1DP_1	DSI1DP_0	RESX
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
DSI0CM	DSI0CP							SPI_SCLK	SPI_MISO
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
DSI0DM_2	DSI0DP_2		TEST5	TEST6	TEST7	TEST		SPI_SS	SPI_MOSI
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
DSI0DM_3	DSI0DP_3		VSS	TEST3	TEST4	VPGM		INT	I2S_OSCLK
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
VDDC	VSS		TEST9	VSS	TEST8	Disable ASSR		I2S_BCLK	I2S_DATA
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
PREC_RES_0	PREC_RES_1		DIFF_SE	TEST2	TEST10	VSS		SPI_I2C	I2S_LRCLK
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
VDDC	VSS							HPD	VDD_PLL912
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
VDD_DP12	VSS_DP	DPLNP_0	VSS_DP	DPLNP_1	VSS_DP	DPLNP_2	VSS_DP	DPLNP_3	DPAUXP
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
VDD_PLL18	REFCLK	DPLNM_0	VDD_DP18	DPLNM_1	VDD_DP12	DPLNM_2	VDD_DP18	DPLNM_3	DPAUXM

Figure 3.2 TC358777XBG Chip Pin Layout (Top view)

3.3. TC358770AXBG Pinout Description

The following table gives the signals of TC358770AXBG and their function.

Table 3.1 TC358770AXBG Functional Signal List

Group	Pin Name	I/O	Type	Function	Power Supply
System (6)	REFCLK	I	SCH	13, 19.2, 26 or 38.4 MHz Ref Clock	1.8 V
	DIFF_SE	I	Normal	1: Differential RefClkN is used 0: Singled end RefClk is used	1.8–3.3 V
	SPI_I2C	I	Normal	1: Activate SPI Slave Interface 0: Select I²C Slave Port	1.8–3.3 V
	RESX	I	SCH	System Reset – active Low	1.8–3.3 V
	DISABLE_ASSR	I	Normal	1: Disable ASSR, set when connecting to DP panel 0: Enable ASSR for eDP panel application	1.8–3.3 V
	INT	O	Normal	Interrupt Pin to Host	1.8–3.3 V
DSI0Rx (10)	DSI0CP	I	MIPI-PHY	MIPI-DSI0 Rx Clock Lane Positive	1.2 V
	DSI0CM	I	MIPI-PHY	MIPI-DSI0 Rx Clock Lane Negative	1.2 V
	DSI0DP[0]	I/O	MIPI-PHY	MIPI-DSI0 Rx Data Lane Positive	1.2 V
	DSI0DM[0]	I/O	MIPI-PHY	MIPI-DSI0 Rx Data Lane Negative	1.2 V
	DSI0DP[3:1]	I	MIPI-PHY	MIPI-DSI0 Rx Data Lane Positive	1.2 V
	DSI0DM[3:1]	I	MIPI-PHY	MIPI-DSI0 Rx Data Lane Negative	1.2 V
DSI1Rx (10)	DSI1CP	I	MIPI-PHY	MIPI-DSI1 Rx Clock Lane Positive	1.2 V
	DSI1CM	I	MIPI-PHY	MIPI-DSI1 Rx Clock Lane Negative	1.2 V
	DSI1DP[3:0]	I	MIPI-PHY	MIPI-DSI1 Rx Data Lane Positive	1.2 V
	DSI1DM[3:0]	I	MIPI-PHY	MIPI-DSI1 Rx Data Lane Negative	1.2 V
DPTx (15)	HPD	I/O	OD	DP Rx Interrupt/Detected	1.8–3.3 V
	DPLNP[3:0]	O	DP-PHY	DP Output Main Link Positive	1.8–3.3 V
	DPLNM[3:0]	O	DP-PHY	DP Output Main Link Negative	1.8–3 3 V
	DPAUXP	I/O	DP-PHY	DP Output AUX Channel Positive	1.8–3.3 V
	DPAUXM	I/O	DP-PHY	DP Output AUX Channel Positive	1.8–3.3 V
	ATB[0]	I/O	DP-PHY	Analog Test Bus Output REFCLKN input when DIFF_SE is asserted	1.8–3.3 V
	ATB[1]	O	DP-PHY	Analog Test Bus Output	1.8–3.3 V
	PREC_RES[1:0]	I	DP-PHY	Precision Resistance (3K @1%)	1.8–3.3 V
Audio (4)	I2S_OSCLK	I	Normal	512 times Audio Sample Clock	18–3.3 V
	I2S_BCLK	I	Normal	Audio Clock	1.8–3.3 V
	I2S_LRCLK	I	Normal	Audio Left/Right Selector	1.8–3.3 V
	I2S_DATA	I	Normal	Audio Data	1.8–3.3 V
SPI/I2C (4)	SPI_SCLK / I2C_SCL	I	OD	SPI Clock / I²C Clock	1.8–3.3 V
	SPI_MOSI / I2C_SDA	I/O	OD	SPI Input data / I²C SDA	1.8–3.3 V
	SPI_MISO	O	N	SPI Output data to Host	1.8–3.3 V
	SPI_SS_I2C_ADR_SEL	I	N	SPI Slave Select, I²C Slave Address Select	1.8–3.3 V
DFT (10)	TEST	I	N	Test Pin, active high	1.8–3.3 V
	TM_CNT	I	N	Test Pin, please tie to GND	1.8–3.3 V
	DIG[8:7], DIG[5:0]	I/O	N	Test Pin, please tie to GND	1.8–3.3 V
Power (22)	VDDS(2)	—	—	VDD for IO power supply	1.8–3.3 V
	VDD_DP18 (4)	—	—	VDD for DP PHY	1.8 V
	VDD_DPA18 (1)	—	—	VDD for DP Analog PHY	1.8 V
	VDD_PLL18 (1)	—	—	VDD for DP PLL	1.8 V
	VDD_PLL12 (1)	—	—	VDD for DP PLL	1.2 V
	VDD_DP12 (4)	—	—	VDD for DP PHY	1.2 V
	VDD_PLL912 (1)	—	—	VDD for Stream Clock PLL	1.2 V
	VDD_DSI12 (4)	—	—	VDD for MIPI-DSI PHY	1.2 V
	VDDC (2)	—	—	VDD for Internal Core	1.2 V
	VPGM (2)	—	—	eFuse Programming Voltage	1.8–3.3 V
Ground (19)	VSS_IO (2)	—	—	VSS for IO power supply	—
	VSS_DP (8)	—	—	VSS for DP PHY	—
	VSS_DPA (1)	—	—	VSS for DP PHY	—
	VSS_PLL (1)	—	—	VSS for DP PLL	—
	VSS_PLL9 (1)	—	—	VSS for Stream Clock PLL	—
	VSS_DSI12 (4)	—	—	VSS for MIPI-DSI PHY	—
	VSSC (2)	—	—	VSS for Internal Core	—

Normal: Normal IO (4 mA)
OD: Pseudo open-drain output, schmitt input
FS/SCH: Fail Safe schmitt input buffer
MIPI-PHY: Front-end analog IO for MIPI
DP-PHY: Front-end analog IO for DisplayPort™

Table 3.2 Pin Count Summary

Group Name	Pin Count
SYSTEM	6
DSI Rx	20
DisplayPort Tx	15
Audio	4
SPI/I2C	4
Test	10
POWER	22
GROUND	19
Total	**100**

3.4. TC358777XBG Pinout Description

The following table gives the signals of TC358777XBG and their function.

Table 3.3 TC358777XBG Functional Signal List

Group	Pin Name	I/O	Type	Function	Power Supply
System (6)	REFCLK	I	SCH	13, 19.2, 26 or 38.4 MHz Ref Clock	1.8 V
	DIFF_SE	I	Normal	1: Differential RefClkN is used 0: Singled end RefClk is used	1.8–3.3 V
	SPI_I2C	I	Normal	1: Activate SPI Slave Interface 0: Select I²C Slave Port	1.8–3.3 V
	DISABLE_ASSR	I	Normal	1: Disable ASSR, set when connecting to DP panel 0: Enable ASSR for eDP panel application	1.8–3.3 V
	RESX	I	SCH	System Reset – active Low	1.8–3.3 V
	INT	O	Normal	Interrupt Pin to Host	1.8–3.3 V
DSI0Rx (10)	DSI0CP	I	MIPI-PHY	MIPI-DSI0 Rx Clock Lane Positive	1.2 V
	DSI0CM	I	MIPI-PHY	MIPI-DSI0 Rx Clock Lane Negative	1.2 V
	DSI0DP[0]	I/O	MIPI-PHY	MIPI-DSI0 Rx Data Lane Positive	1.2 V
	DSI0DM[0]	I/O	MIPI-PHY	MIPI-DSI0 Rx Data Lane Negative	1.2 V
	DSI0DP[3:1]	I	MIPI-PHY	MIPI-DSI0 Rx Data Lane Positive	1.2 V
	DSI0DM[3:1]	I	MIPI-PHY	MIPI-DSI0 Rx Data Lane Negative	1.2 V
DSI1Rx (10)	DSI1CP	I	MIPI-PHY	MIPI-DSI1 Rx Clock Lane Positive	1.2 V
	DSI1CM	I	MIPI-PHY	MIPI-DSI1 Rx Clock Lane Negative	1.2 V
	DSI1DP[3:0]	I	MIPI-PHY	MIPI-DSI1 Rx Data Lane Positive	1.2 V
	DSI1DM[3:0]	I	MIPI-PHY	MIPI-DSI1 Rx Data Lane Negative	1.2 V
DPTx (13)	HPD	I/O	OD	DP Rx Interrupt/Detected	1.8–3.3 V
	DPLNP[3:0]	O	DP-PHY	DP Output Main Link Positive	1.8–3.3 V
	DPLNM[3:0]	O	DP-PHY	DP Output Main Link Negative	1.8–3.3 V
	DPAUXP	I/O	DP-PHY	DP Output AUX Channel Positive	1.8–3.3 V
	DPAUXM	I/O	DP-PHY	DP Output AUX Channel Positive	1.8–3.3 V
	PREC_RES[1:0]	I	DP-PHY	Precision Resistance (3K @1%)	1.8–3.3 V
Audio (4)	I2S_OSCLK	I	Normal	512 times Audio Sample Clock	1.8–3.3 V
	I2S_BCLK	I	Normal	Audio Clock	1.8–3.3 V
	I2S_LRCLK	I	Normal	Audio Left/Right Selector	1.8–3.3 V
	I2S_DATA	I	Normal	Audio Data	1.8–3.3 V
SPI/I2C (4)	SPI_SCLK / I2C_SCL	I	OD	SPI Clock / I²C Clock	1.8–3.3 V
	SPI_MOSI / I2C_SDA	I/O	OD	SPI Input data / I²C SDA	1.8–3.3 V
	SPI_MISO	O	N	SPI Output data to Host	1.8–3.3 V
	SPI_SS_I2C_ADR_SEL	I	N	SPI Slave Select, I²C Slave Address Select	1.8–3.3 V
DFT (10)	TEST	I	N	Test Pin, active high	1.8–3.3 V
	TEST[10:2]	I	N	Test Pin, please tie to GND	—
Power (12)	VDD_IO (1)	—	—	VDD for IO power supply	1.8–3.3 V
	VDD_DP18 (2)	—	—	VDD for DP PHY/Analog PHY	1.8 V
	VDD_PLL18 (1)	—	—	VDD for DP PLL	1.8 V
	VDD_DP12 (2)	—	—	VDD for DP PHY/PLL	1.2 V
	VDD_PLL912 (1)	—	—	VDD for Stream Clock PLL	1.2 V
	VDD_DSI12 (2)	—	—	VDD for MIPI-DSI PHY	1.2 V
	VDDC (2)	—	—	VDD for Internal Core	1.2 V
	VPGM (1)	—	—	eFuse Programming Voltage	1.8–3.3 V
Ground (11)	VSS_DP (4)	—	—	VSS for DP PHY/PLL	—
	VSS (7)	—	—	VSS for Internal Core/MIPI/IO	—

Normal: Normal IO (4 mA)
OD: Pseudo open-drain output, Schmitt input
FS/SCH: Fail Safe Schmitt input buffer
MIPI-PHY: Front-end analog IO for MIPI
DP-PHY: Front-end analog IO for Display Port

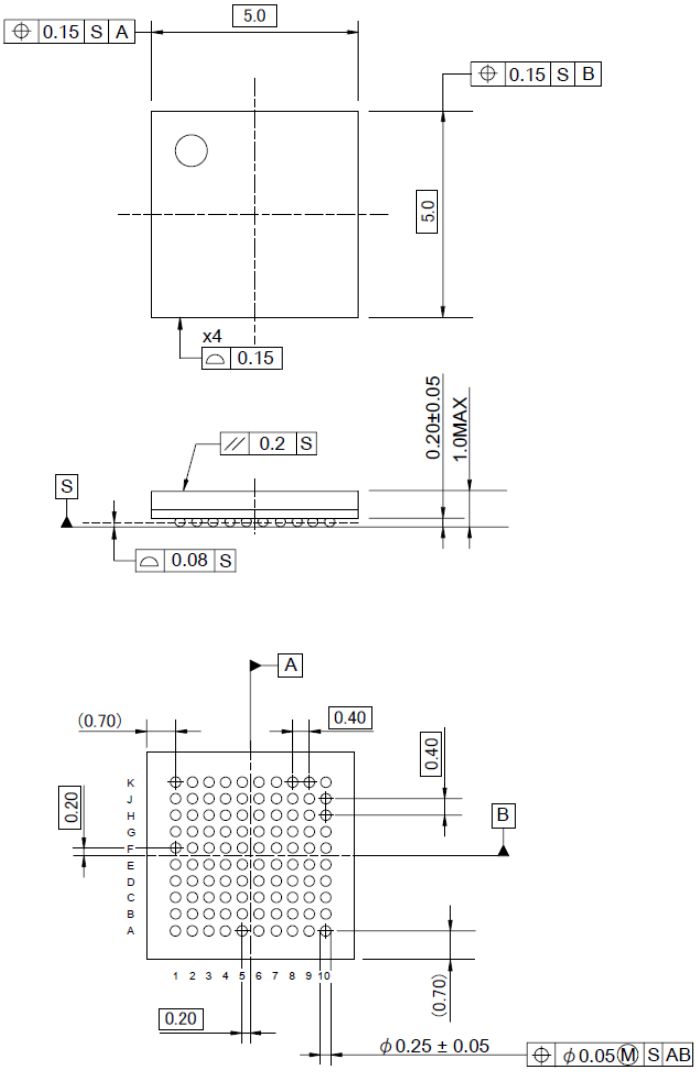
Table 3.4 Pin Count Summary

Group Name	Pin Count
SYSTEM	6
DSI Rx	20
DisplayPort Tx	13
I2S	4
SPI/I2C	4
Test	10
POWER	12
GROUND	11
Total	**80**

4. Package

TC358770AXBG housed in a 5.0 mm by 5.0 mm size package with 0.4 mm ball pitch. The detailed package drawing is shown below.

P-VFBGA100-0505-0.40-001 "Unit:mm"



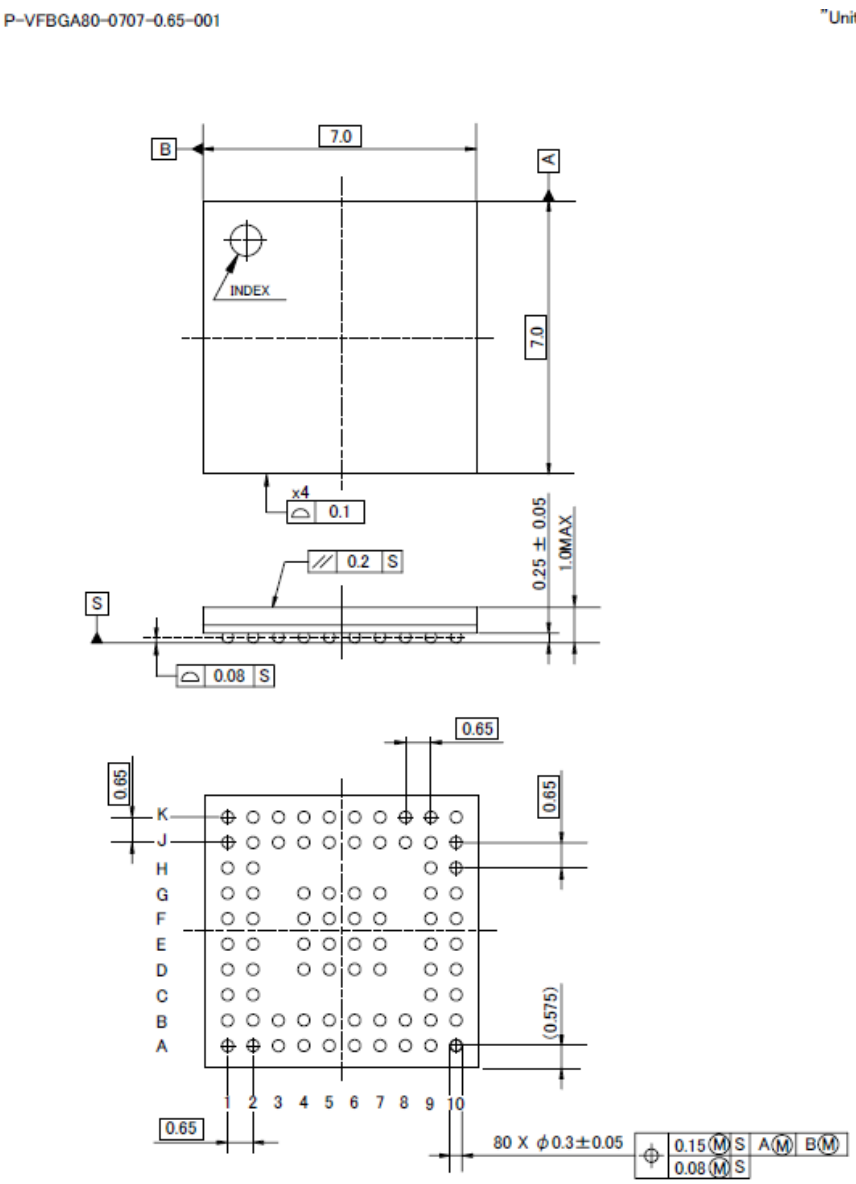
Weight: 40 mg (Typ.)

Figure 4.1 TC358770AXBG Package Dimension

Table 4.1 TC358770AXBG Package Details

Description	Normal
Body size (W, mm)	5
Body size (L, mm)	5
Overall thickness (t, mm)	1
Terminal pitch (mm)	0.4

TC358777XBG housed in a 7.0 mm by 7.0 mm size package with 0.65 mm ball pitch. The detailed package drawing is shown below.



Weight: 65 mg (Typ.)

Figure 4.2 TC358777XBG Package Dimension

Table 4.2 TC358777XBG Package Details

Description	Normal
Body size (W, mm)	7
Body size (L, mm)	7
Overall thickness (t, mm)	1
Terminal pitch (mm)	0.65

5. Electrical characteristics

5.1. Absolute Maximum Ratings

VSS = 0 V reference

VDD18 used for VDDIO as well as VDD-DP18; VDD12 used for VDDC as well as VDD-DSI12

Parameter	Symbol	Rating	Unit
Supply voltage (1.8 V)	VDD18	-0.3 to +3.5	V
Supply voltage (1.2 V)	VDD12	-0.3 to +2.0	V
Supply voltage (IO)	VDD18	-0.3 to +3.5	V
	VREF	-0.3 to +3.5	V
Input voltage	VIN	-0.3 to VDDIO+0.3	V
Output voltage	VOUT	-0.3 to VDDIO+0.3	V
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS = 0 V reference

VDD18 used for VDDIO as well as VDD-DP18; VDD12 used for VDDC as well as VDD-DSI12

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8 V)	VDD18	1.71	1.8	1.89	V
Supply voltage (1.2 V)	VDD12	1.14	1.2	1.26	V
Operating frequency (internal)	Fop	—	—	270	MHz
Operating temperature	Ta	-20	—	+70	°C

5.3. DC Electrical Specification

VSS = VSS_C = VSS_IO = VSS_DSI = VSS_DP = VSS_PLL = VSS_REG = 0 V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Input voltage High level CMOS input (Note1)	VIH	0.7 VDDIO	—	VDDIO	V
Input voltage Low level CMOS input (Note1)	VIL	0	—	0.3 VDDIO	V
Input voltage High level CMOS Schmitt Trigger (Note1)	VIHS	0.7 VDDIO	—	VDDIO	V
Input voltage Low level CMOS Schmitt Trigger (Note1)	VILS	0	—	0.3 VDDIO	V
Output voltage High level (Note1)(Note2)	VOH	0.8 VDDIO	—	VDDIO	V
Output voltage Low level (Note1)(Note2)	VOL	0	—	0.2 VDDIO	V
Input leak current High level	IIH1 (Note3)	-10	—	10	μA
Input leak current Low level	IIL1 (Note4)	-10	—	10	μA
	IIL2 (Note5)	-200	—	-10	μA

Note1: VDDIO within recommended operating condition.

Note2: Output current value is according to each IO buffer specification. Output voltage changes with output current value.

Note3: Normal pin, or Pull-up I/O pin applied VDD18_IO supply voltage to input pin.

Note4: Normal pin applied VSS (0 V) to input pin.

Note5: Pull-up I/O pin applied VSS (0 V) to input pin.

6. Revision History

Table 6.1 Revision History

Revision	Date	Description
1.0	2012-11-10	1. Start from 770XBG Rev 0.99D 2. Add ASSR support 3. Add Power consumption for each voltage rail
1.1	2013-01-15	1. Update MIPI copyright Footer: Change "Toshiba America Electronic Components, Inc." to "Toshiba Corporation and its affiliates." 2. Update VSDelay Calculation (assume DP data lane is either 2 or 4 lanes)
1.2	2013-10-25	1. Typo correction on register Tx_Rx_TA 2. Add Audio Functionality Description
1.3	2013-11-17	1. Update register field description for 0x0644[23:18]
1.4	2014-06-20	1. Add 777XBG package
1.41	2016-07-20	1. Typo Correction on DSI1DP[3:0]/DSI1DM[3:0]
1.42	2016-09-01	1. Modified duplicate DSI1CP/DSI1CM.
1.6	2017-10-23	Corrected typo. Changed header, footer and the last page. Changed corporate name.

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