TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

# **T2N7002AK**

#### High Speed Switching Applications

· ESD protected gate

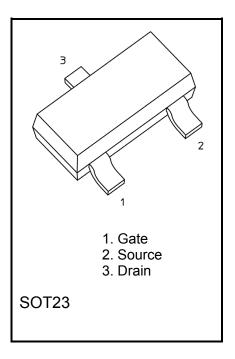
• Low ON-resistance  $R_{DS(on)} = 2.8 \Omega \text{ (typ.) } (@V_{GS} = 10 \text{ V})$ 

 $R_{DS(on)} = 3.1 \Omega \text{ (typ.) } (@V_{GS} = 5 \text{ V})$ 

 $R_{DS(on)} = 3.2 \Omega \text{ (typ.) } (@V_{GS} = 4.5 \text{ V})$ 

#### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristic		Symbol	Rating	Unit	
Drain-source voltage	$V_{DSS}$	60	٧		
Gate-source voltage	$V_{GSS}$	± 20	V		
Drain current (Note1)	DC	ID	200	mA	
Drain current (Note1)	Pulse	I <sub>DP</sub> (Note 2)	760		
Dower dissination	P <sub>D</sub> (Note 3)	320	mW		
Power dissipation		P <sub>D</sub> (Note 4)	1000		
Channel temperature	T <sub>ch</sub>	150	°C		
Storage temperature	T <sub>stg</sub> –55 to 150		°C		



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: The channel temperature should not exceed 150°C during use.

Note 2: Pulse width ≤ 10 µs, Duty ≤ 1%

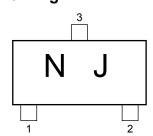
Note 3: Mounted on an FR4 board

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 0.42 \text{ mm}^2 \text{ x 3})$ 

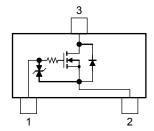
Note 4: Mounted on an FR4 board

(25.4 mm  $\times$  25.4 mm  $\times$  1.6 mm, Cu Pad: 645  $\text{mm}^2$  )

#### Marking



### **Equivalent Circuit (top view)**



Start of commercial production 2015-01



## **Electrical Characteristics (Ta = 25°C, Otherwise specified)**

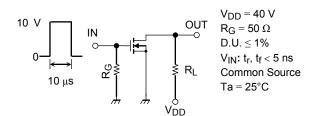
Ch	aracteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain-source b	oreakdown voltage	V (BR) DSS	$I_D = 250 \mu A, V_{GS} = 0 V$	60	_	_	V
Drain cutoff current	I <sub>DSS</sub>	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	_	_	1	μА	
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, Tj=150 ^{\circ}\text{C}$	_	_	200	μΑ	
		I <sub>GSS</sub>	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±2	μА
Gate leakage current	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±0.5		
	$V_{GS} = \pm 5 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±0.1		
Gate threshold	l voltage	V <sub>th</sub>	$I_D = 250 \mu A, V_{DS} = V_{GS}$	1.1	_	2.1	V
Forward transf	er admittance	Y <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_D = 200 \text{ mA}$ (Note 5)	_	450	_	mS
	R <sub>DS</sub> (ON) (Note 5)	$I_D = 100 \text{ mA}, V_{GS} = 10 \text{ V}$	_	2.8	3.9	Ω	
D : 011 : 1		I <sub>D</sub> = 100 mA, V <sub>GS</sub> = 10 V, Tj=150 °C	_	5.4	8.1		
Drain-source ON-resistance		I <sub>D</sub> = 100 mA, V <sub>GS</sub> = 5 V	_	3.1	4.4		
		I <sub>D</sub> = 100 mA, V <sub>GS</sub> = 4.5 V	_	3.2	4.7		
Total Gate Charge Gate-Source Charge Gate-Drain Charge		Q <sub>G(tot)</sub>	V 00 V 1 000 A	_	0.27	0.35	nC
		Q <sub>GS</sub>	$V_{DS} = 30 \text{ V, I}_{D} = 200 \text{ mA}$	_	0.08	_	
		$Q_{GD}$	V <sub>GS</sub> = 4.5 V	_	0.08	_	
Input capacitance		C <sub>iss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	11	17	pF
Output capacitance		Coss		_	3	_	
Reverse transfer capacitance		C <sub>rss</sub>		_	0.7	_	
Switching time	Turn-on delay time	t <sub>d(on)</sub>		_	2	4	- ns
	Rise time	t <sub>r</sub>	$V_{DD}$ = 40 V, $I_D$ = 160 mA $V_{GS}$ = 0 V to 10 V, $R_G$ = 50 $\Omega$	_	3	_	
	Turn-off delay time	t <sub>d(off)</sub>		_	7	14	
	Fall time	t <sub>f</sub>		_	24	_	
Drain-source forward voltage		V <sub>DSF</sub>	$I_D = -115 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note 5)	_	-0.87	-1.2	٧

Note 5: Pulse test

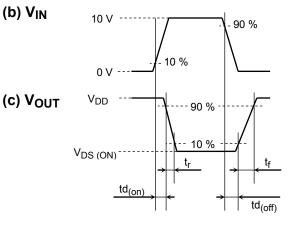
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#### **Switching Time Test Circuit**

#### (a) Test Circuit





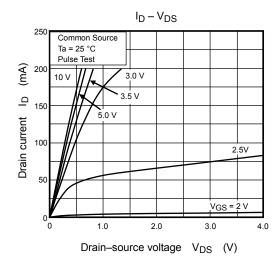


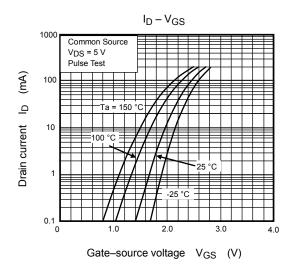
#### **Notice of Usage**

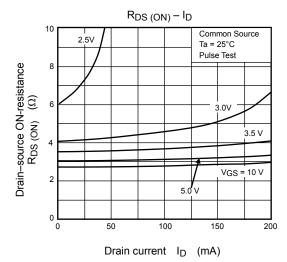
Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current (ID) to below (0.25 mA for this device). Then, for normal switching operation, VGS(ON) must be higher than Vth, and VGS(OFF) must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ . Take this into consideration when using the device.

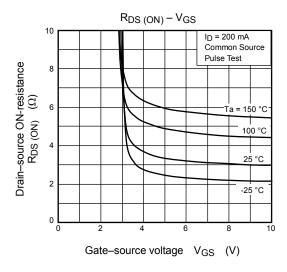
#### **Handling Precaution**

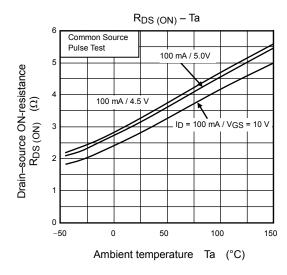
The MOSFETs in this device are sensitive to electrostatic discharge. When handling this device, the worktables, operators, soldering irons and other objects should be protected against anti-static discharge.

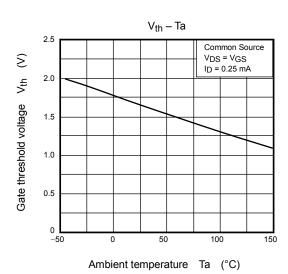


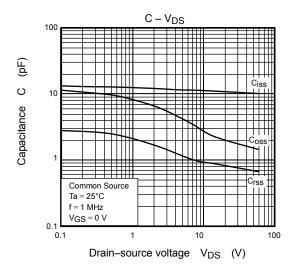


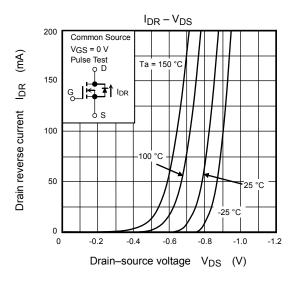


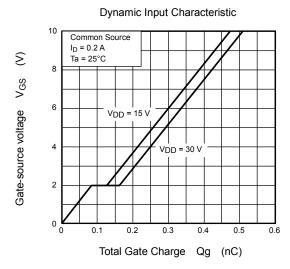


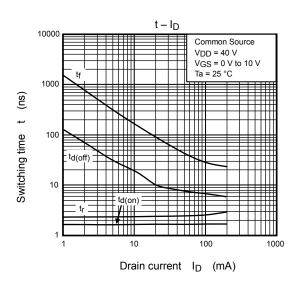


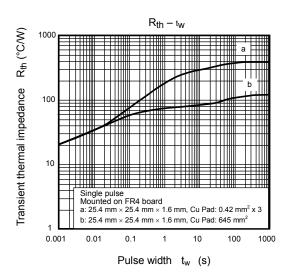


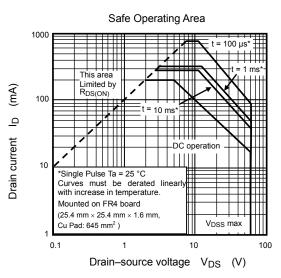












Note: The above characteristics curves are presented for reference only and not guaranteed by production test.



# **Package Dimensions**

Unit: mm SOT23 0.15 <del>+0.1</del> -0.05  $2.9 \pm 0.1$ Α 3 2.4 ±0.2 2 1 0.4 +0.1 -0.05 <del>ф</del>0.10 (М) А 0.95 0.95 1.9 0.05 ±0.05  $0.9 \pm 0.1$ 

Weight: 0.009g (typ.)

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