

TSF9N90M

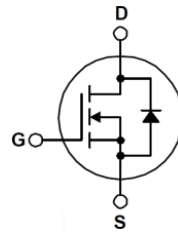
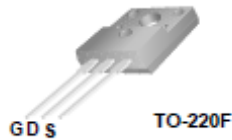
900V N-Channel MOSFET

General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

- 9A,900V,Max. $R_{DS(on)}=1.4\ \Omega$ @ $V_{GS}=10V$
- Low gate charge(typical 52nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	900	V
V_{GS}	Gate-Source Voltage	± 30	V
I_D	Drain Current	$T_C = 25^\circ\text{C}$	9*
		$T_C = 100^\circ\text{C}$	5.7*
I_{DM}	Pulsed Drain Current	36*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	900	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.8	mJ
I_{AR}	Repetitive avalanche current (Note 1)	9	A
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	48	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Resistance Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.6	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C/W}$

Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 4.5\ \text{A}$	--	1.2	1.4	Ω
g_{fs}	Forward transfer conductance(note 3)	$V_{DS} = 10\ \text{V}, I_D = 4.5\ \text{A}$	--	9.2	--	S

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	900	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 900\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	μA
		$V_{DS} = 720\ \text{V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	-100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	2100	--	pF
C_{oss}	Output Capacitance		--	175	--	pF
C_{riss}	Reverse Transfer Capacitance		--	14	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 450\ \text{V}, I_D = 9\ \text{A},$ $R_G = 25\ \Omega$ (Note 3,4)	--	50	--	ns
t_r	Turn-On Rise Time		--	120	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	100	--	ns
t_f	Turn-Off Fall Time		--	75	--	ns
Q_g	Total Gate Charge	$V_{DS} = 720\ \text{V}, I_D = 9\ \text{A},$ $V_{GS} = 10\ \text{V}$ (Note 3,4)	--	52	68	nC
Q_{gs}	Gate-Source Charge		--	16	--	nC
Q_{gd}	Gate-Drain Charge		--	20	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	9	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	36		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 9\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$I_S = 9\ \text{A}, V_{GS} = 0\ \text{V}$	--	550	--	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\ \text{A}/\mu\text{s}$ (Note 4)	--	6.5	--	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=21\text{mH}, I_{AS}=9\text{A}, V_{DD}=50\text{V}, R_G=25\Omega,$ Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Typical Characteristics

Fig. 1 $I_D - V_{DS}$

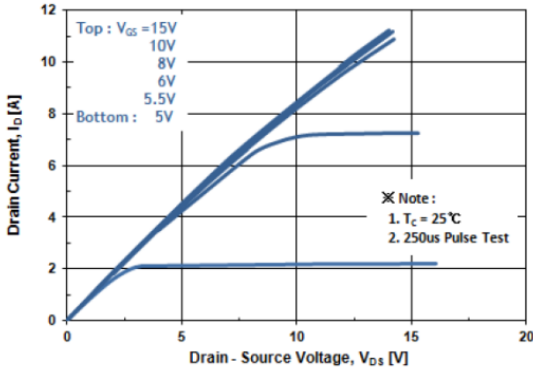


Fig. 2 $I_D - V_{GS}$

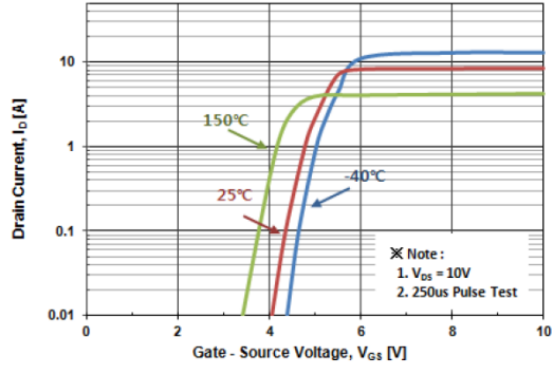


Fig. 3 $R_{DS(ON)} - I_D$

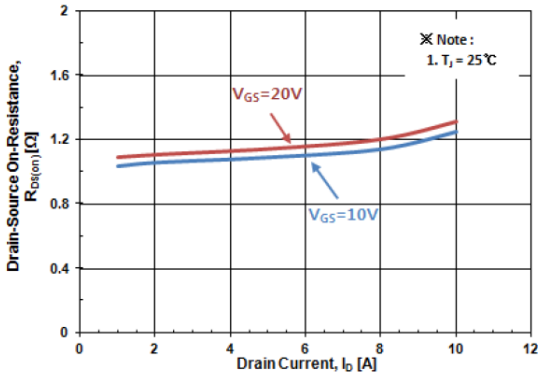


Fig. 4 $I_S - V_{SD}$

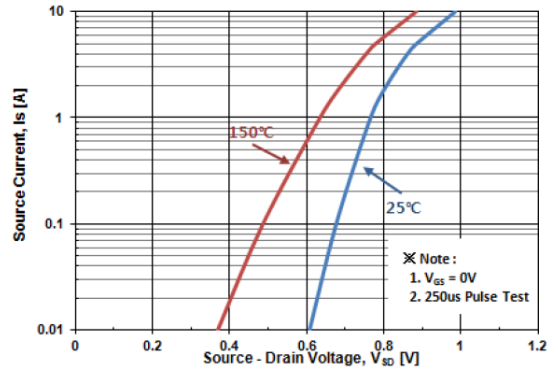


Fig. 5 Capacitance - V_{DS}

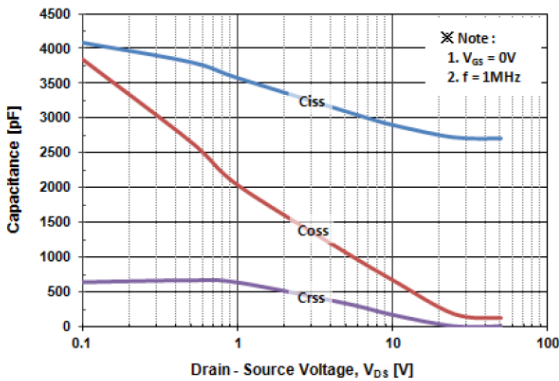
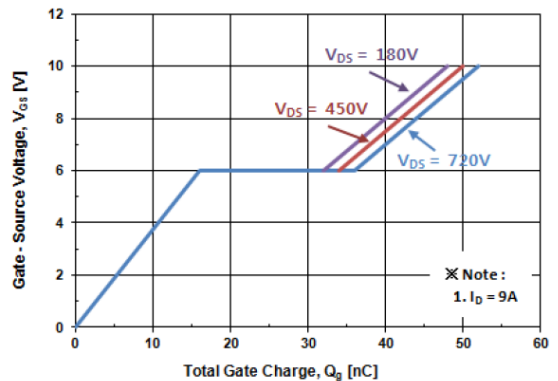


Fig. 6 $V_{GS} - Q_G$



Typical Characteristics

Fig. 7 $BV_{DSS} - T_J$

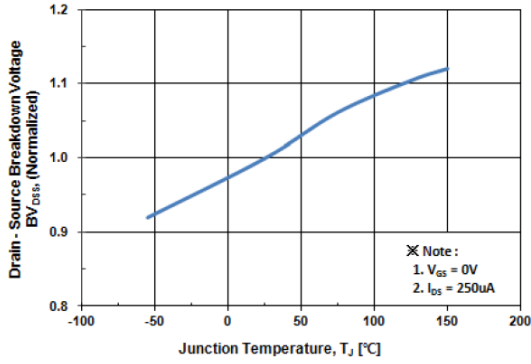


Fig. 8 $R_{DS(ON)} - T_J$

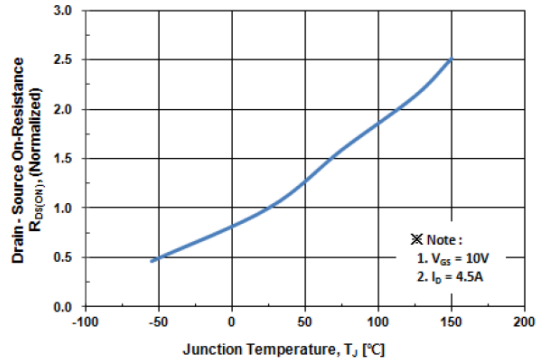


Fig. 9 $I_D - T_C$

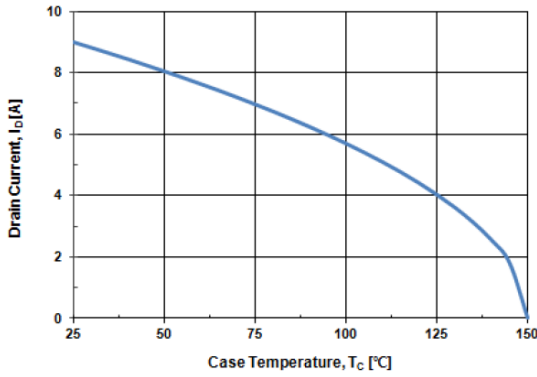


Fig. 10 Safe Operating Area

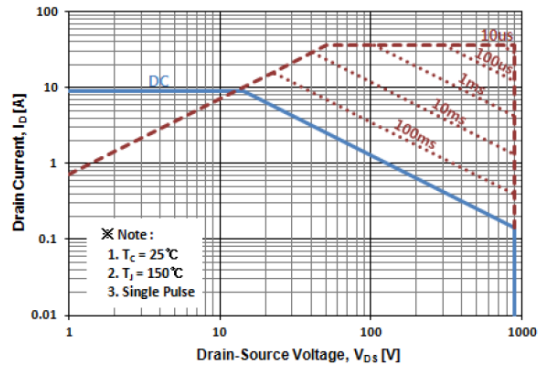


Fig. 11 Transient Thermal Impedance

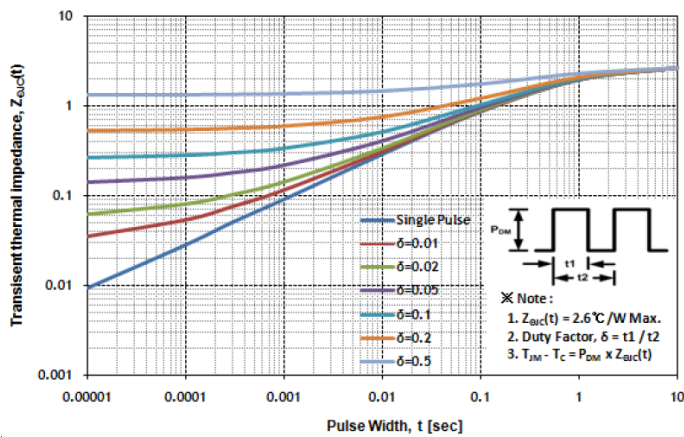


Fig 12. Gate Charge Test Circuit & Waveform

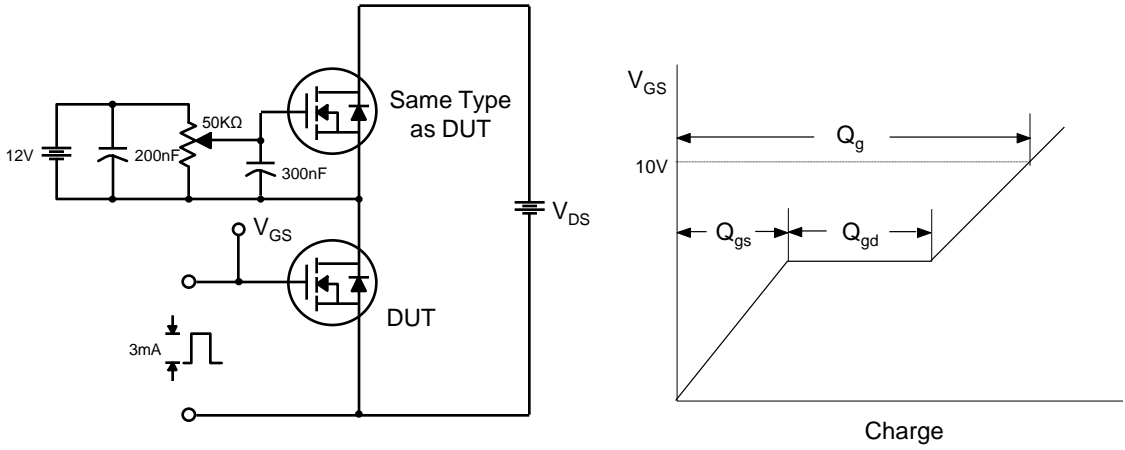


Fig 13. Resistive Switching Test Circuit & Waveforms

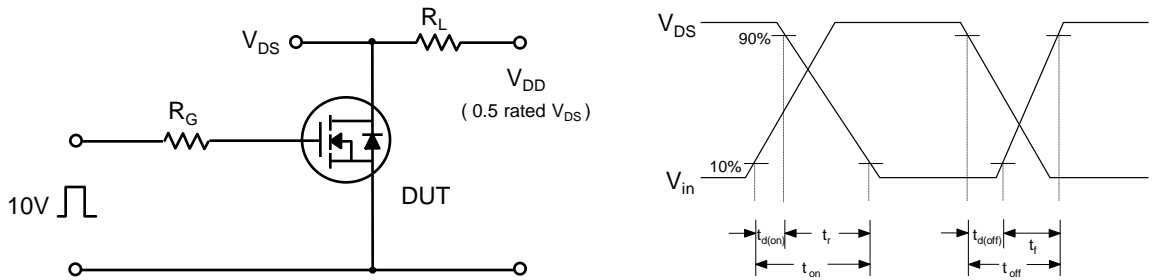


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

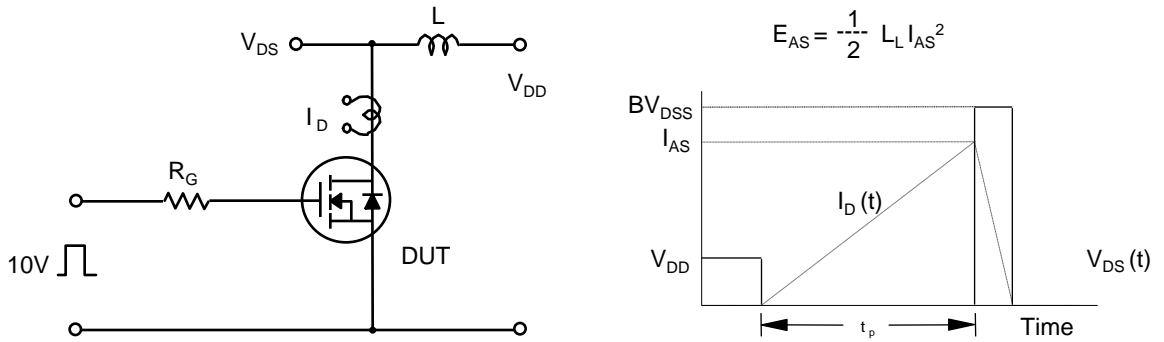
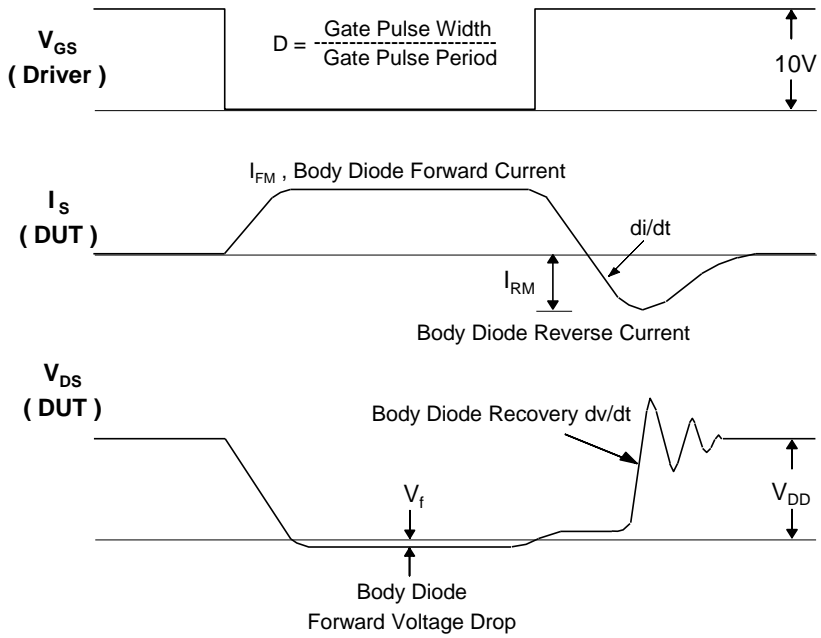
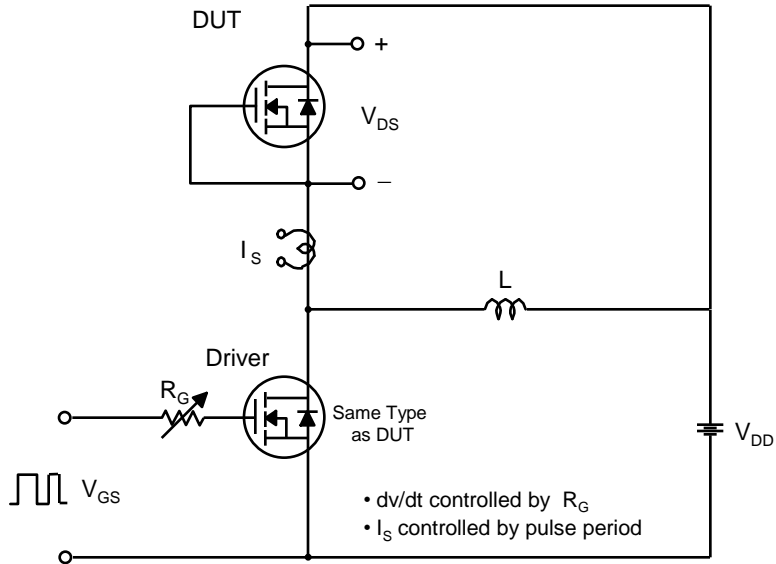


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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