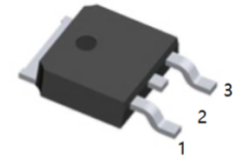


General Description

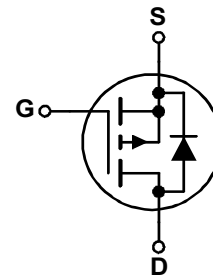
This P-Channel MOSFET has been produced using technology to deliver low $r_{DS(on)}$ and good switching characteristic offering superior performance in application.



1.G 2.D 3.S
TO-252(DPAK) top view

Features

- $V_{DS}(V) = -40V$
- $I_D = -8.4A$ ($V_{GS} = -10V$)
- $R_{DS(ON)} < 27m\Omega$ ($V_{GS} = -10V$)
- $R_{DS(ON)} < 35m\Omega$ ($V_{GS} = -4.5V$)
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS Compliant



Application

- Inverter
- Power Supplies

MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Conditions	Rated Values	Units
V_{DS}	Drain to Source Voltage		-40	V
V_{GS}	Gate to Source Voltage		± 20	V
I_D	Drain Current -Continuous(Package Limited)	$T_C = 25^\circ C$	-32	A
	-Continuous(Silicon Limited)	$T_C = 25^\circ C$ (Note 1)	-40	
	-Continuous	$T_A = 25^\circ C$ (Note 1a)	-8.4	
	-Pulsed		-100	
E_{AS}	Drain-Source Avalanche Energy	(Note 3)	121	mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	69	W
	Power Dissipation	(Note 1a)	3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.8	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	40	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-33		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -32\text{V}, V_{GS} = 0\text{V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		4.9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -8.4\text{A}$		23	27	m Ω
		$V_{GS} = -4.5\text{V}, I_D = -7\text{A}$		30	35	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{V}, I_D = -8.4\text{A}$		23		S
C_{iss}	Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1790	2380	pF
C_{oss}	Output Capacitance		260	345	pF	
C_{rss}	Reverse Transfer Capacitance		140	205	pF	
R_g	Gate Resistance	$f = 1\text{MHz}$		4		Ω
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\text{V}, I_D = -8.4\text{A}, V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		8	16	ns
t_r	Rise Time		15	27	ns	
$t_{d(off)}$	Turn-Off Delay Time		34	55	ns	
t_f	Fall Time		14	26	ns	
$Q_{g(TOT)}$	Total Gate Charge	$V_{DD} = -20\text{V}, I_D = -8.4\text{A}$		19	27	nC
Q_{gs}	Gate to Source Gate Charge	$V_{GS} = -5\text{V}$		5.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			6.1		nC
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -8.4\text{A}$ (Note 2)		-0.85	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -8.4\text{A}, di/dt = 100\text{A}/\mu\text{s}$		30	45	ns
Q_{rr}	Reverse Recovery Charge		31	47	nC	

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

- a. $40^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper
- b. $96^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

2: Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3: Starting $T_J = 25^\circ\text{C}$, $L = 3\text{mH}$, $I_{AS} = 9\text{A}$, $V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

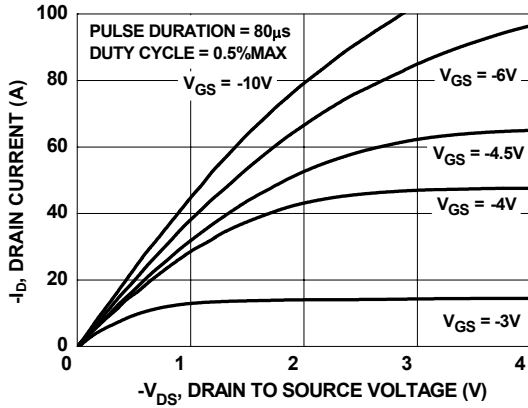


Figure 1. On Region Characteristics

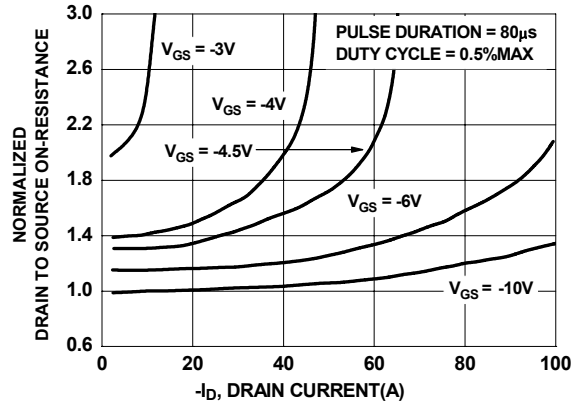


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

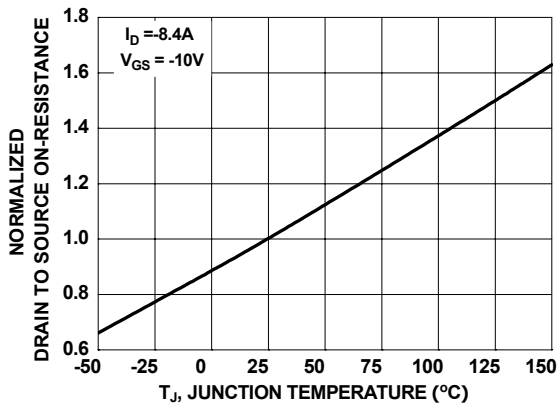


Figure 3. Normalized On Resistance vs Junction Temperature

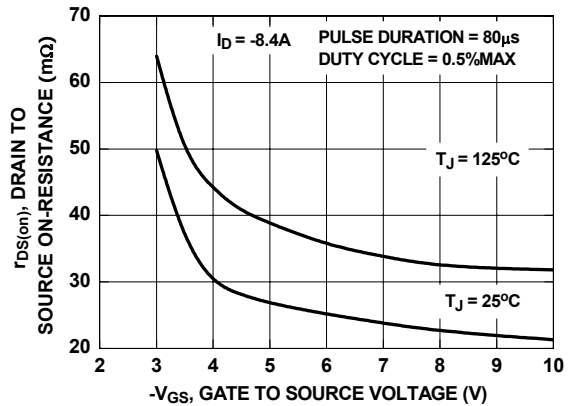


Figure 4. On-Resistance vs Gate to Source Voltage

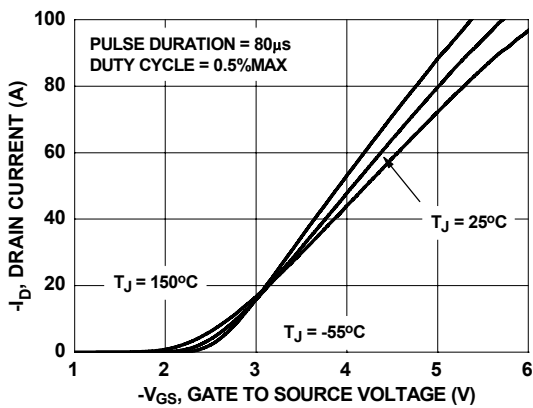


Figure 5. Transfer Characteristics

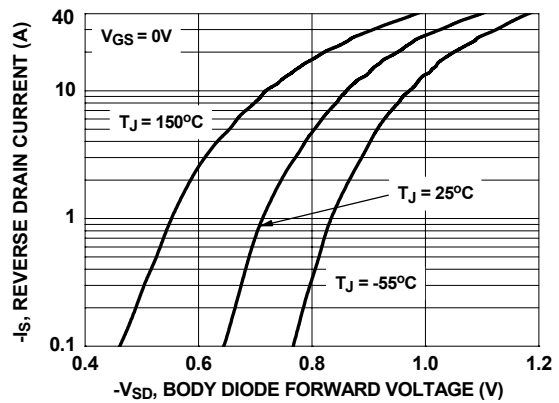


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

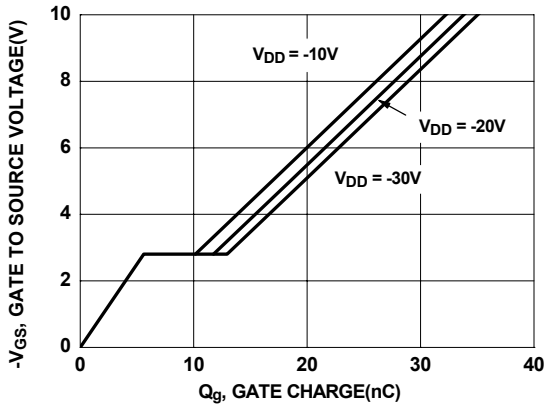


Figure 7. Gate Charge Characteristics

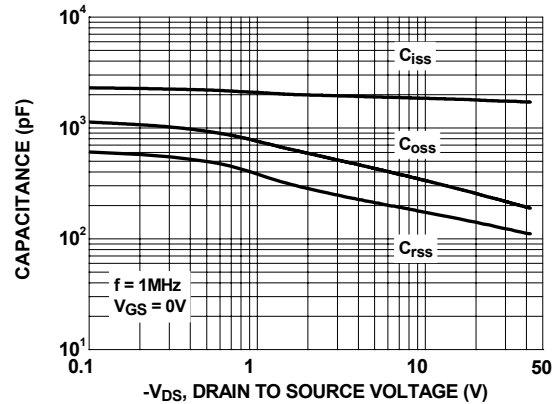


Figure 8. Capacitance vs Drain to Source Voltage

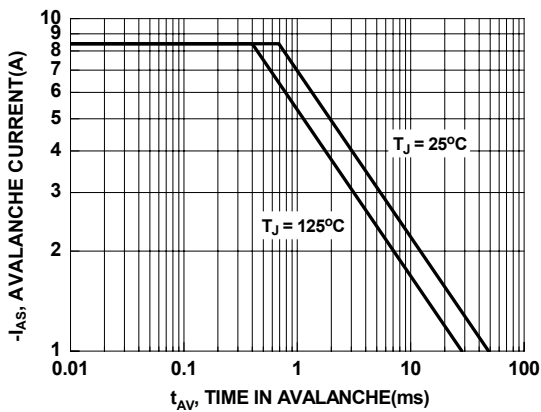


Figure 9. Unclamped Inductive Switching Capability

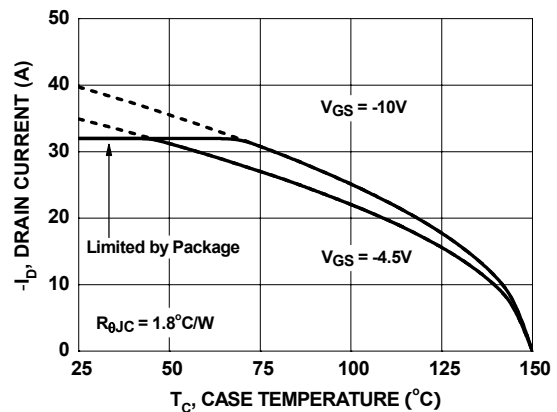


Figure 10. Maximum Continuous Drain Current vs Case Temperature

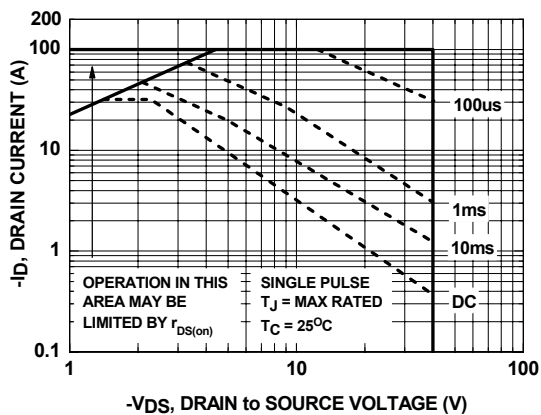


Figure 11. Forward Bias Safe Operating Area

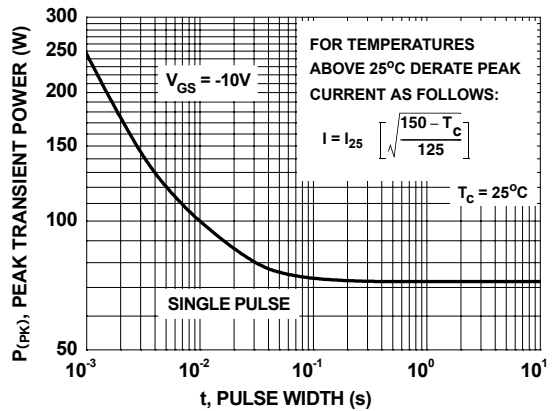


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

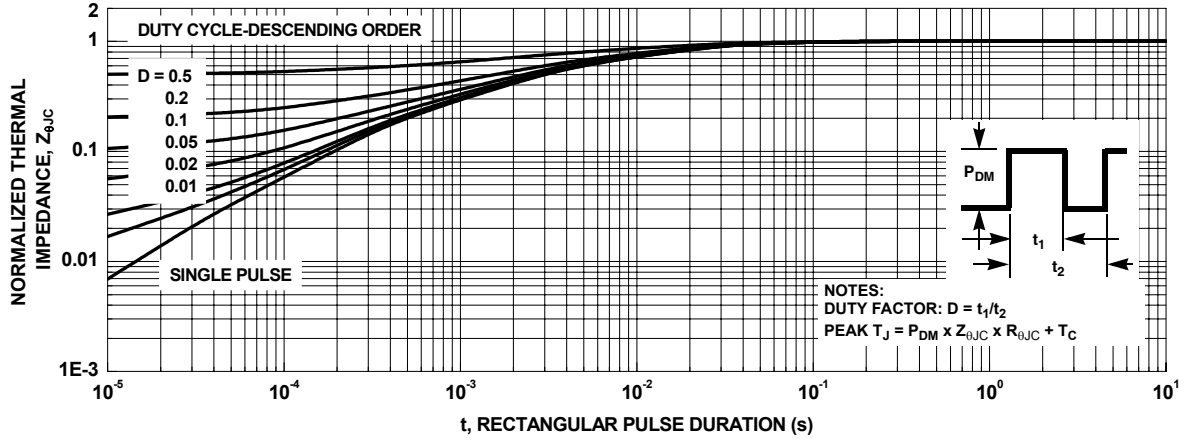
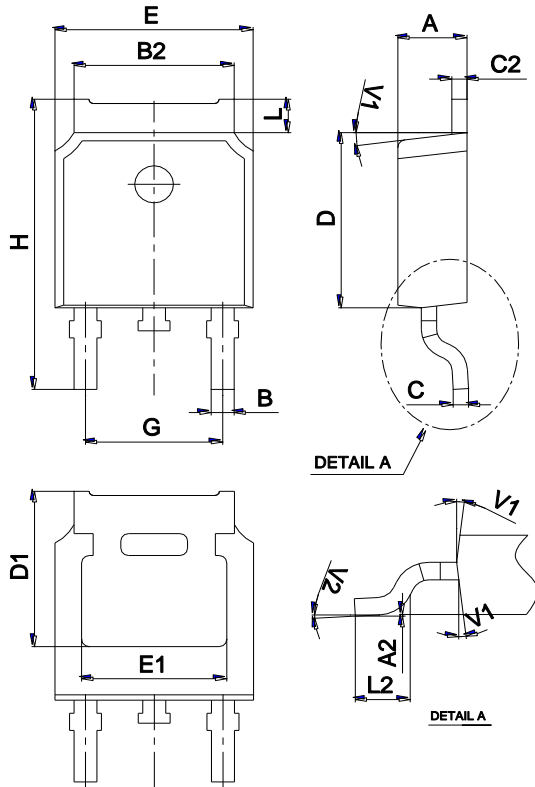


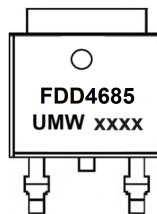
Figure 13. Transient Thermal Response Curve

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDD4685	TO-252	2500	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

[>>UMW\(友台半导体\)](#)