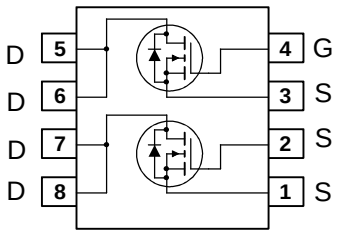
General Description

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



Features

- $V_{DS\ (V)}$ = 30V
- I_D = 6A (V_{GS} = 10V)
- $R_{DS(ON)}$ < 28mΩ (V_{GS}=10V)
- $R_{DS(ON)}$ < 35 mΩ (V_{GS}=4.5V)
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current – Continuous	(Note 1a)	6	A
	– Pulsed		20	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.6	W
		(Note 1b)	1.0	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

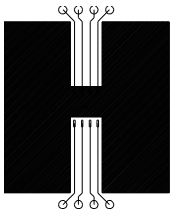
Electrical Characteristics

T_A = 25°C unless otherwise noted

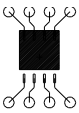
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = 24 V, V_{GS} = 0 V, T_J = 55°C			1 10	µA
I_{GSS}	Gate–Source Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–4.5		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 6 A V_{GS} = 4.5 V, I_D = 5 A		19 24	28 35	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 6 A		25		S
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		575		pF
C_{oss}	Output Capacitance			145		pF
C_{rss}	Reverse Transfer Capacitance			65		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		2.1		Ω
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	16	ns
t_r	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			23	37	ns
t_f	Turn–Off Fall Time			3	6	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 6 A, V_{GS} = 5 V		5.8	8.1	nC
Q_{gs}	Gate–Source Charge			1.7		nC
Q_{gd}	Gate–Drain Charge			2.1		nC
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.75	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 6 A, d_{iF}/d_t = 100 A/µs		20		nS
Q_{rr}	Diode Reverse Recovery Charge			10		nC

Notes:

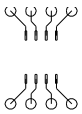
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

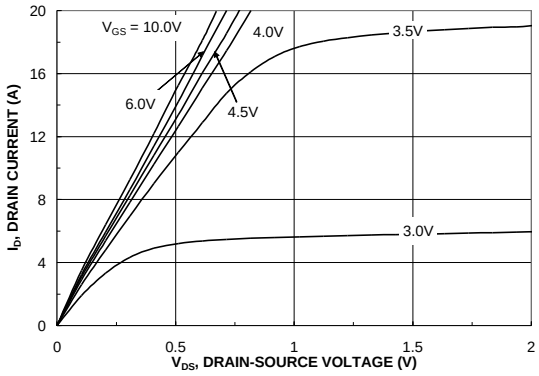


Figure 1. On-Region Characteristics.

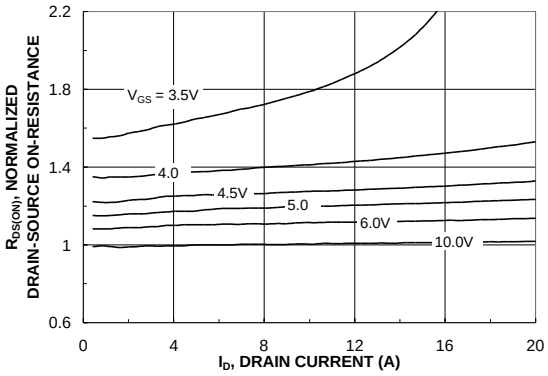


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

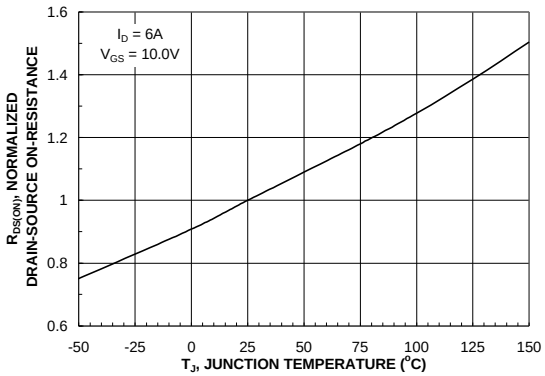


Figure 3. On-Resistance Variation with Temperature.

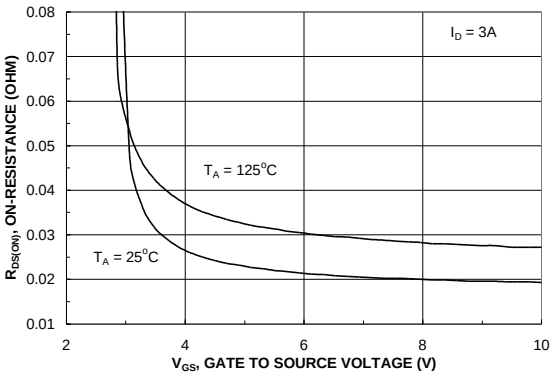


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

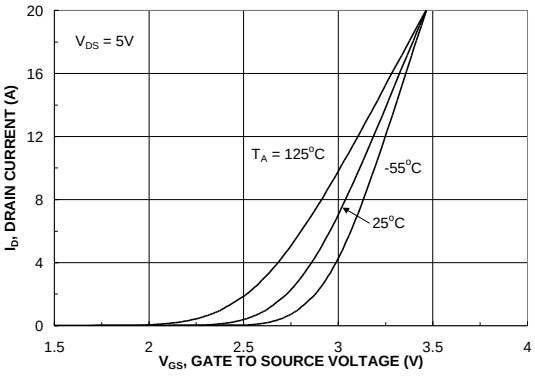


Figure 5. Transfer Characteristics.

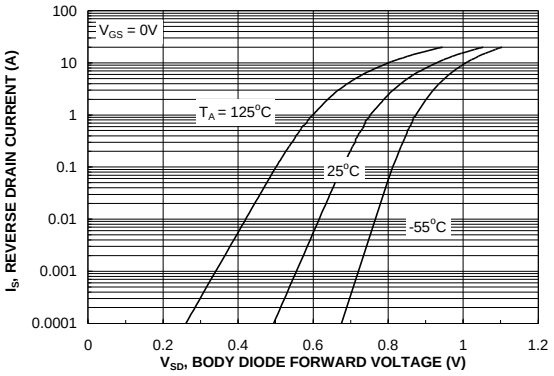


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

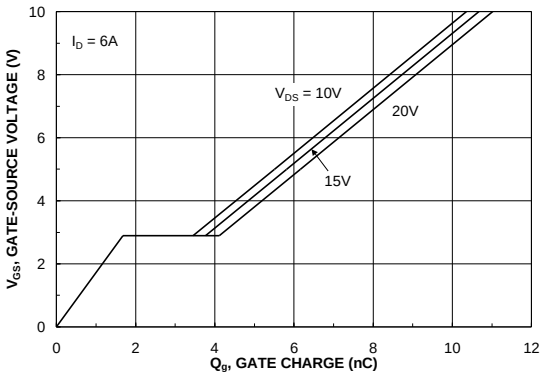


Figure 7. Gate Charge Characteristics.

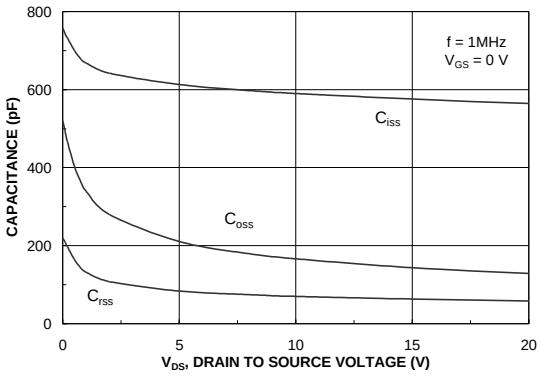


Figure 8. Capacitance Characteristics.

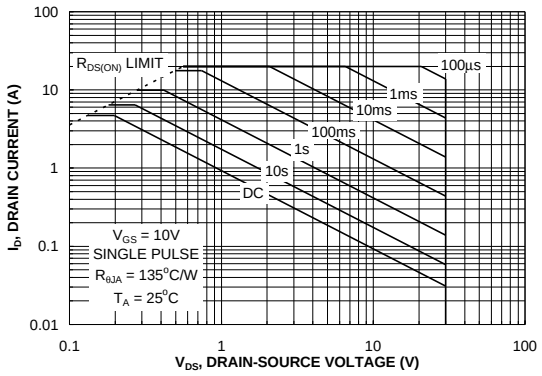


Figure 9. Maximum Safe Operating Area.

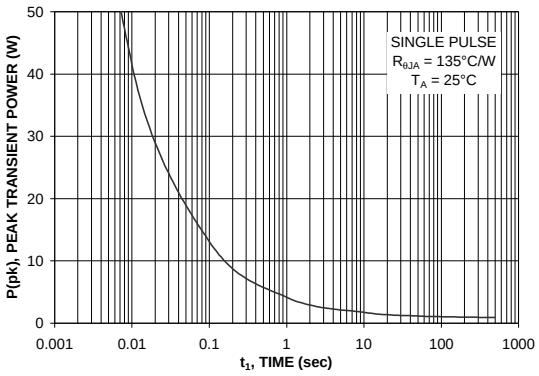


Figure 10. Single Pulse Maximum Power Dissipation.

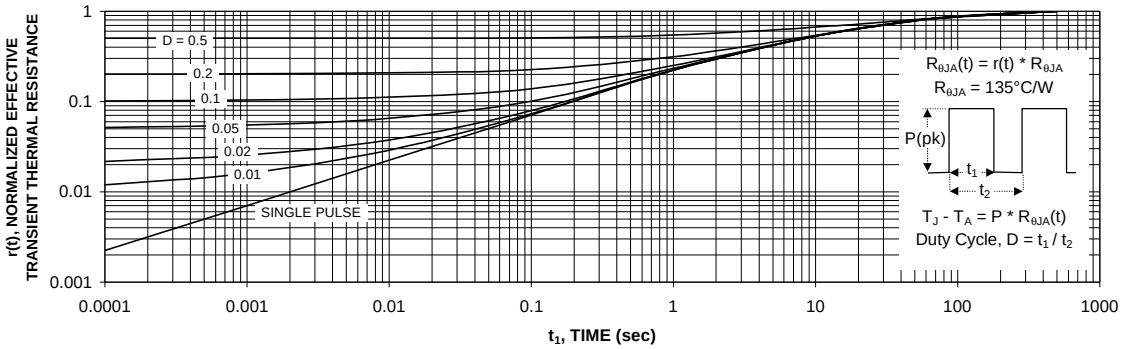
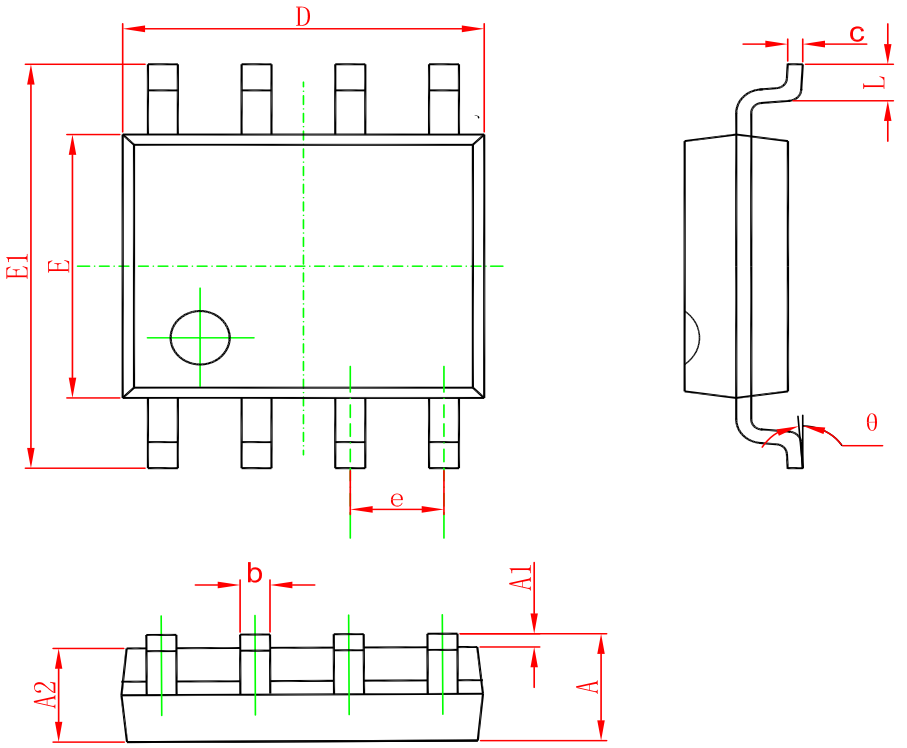


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

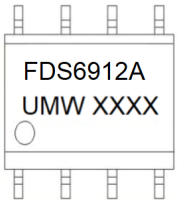
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDS6912A	SOP-8	3000	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)