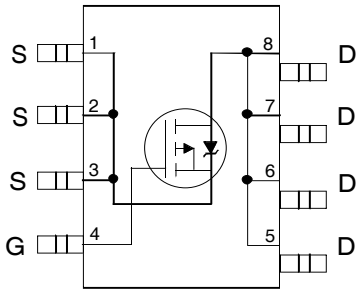
Features

- $V_{DS\ (V)}$=-55V
- $R_{DS(ON)}$ < 20 mΩ (V_{GS} =-4.5V)
- $R_{DS(ON)}$ < 60 mΩ (V_{GS} =-2.7V)
- Generation V Technology
- Ultra Low On-Resistance
- Surface Mount
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free



SOP-8

Description

The SOP-8 has been modified through a customi-zed eadframe for enhanced thermal characteristics and multiple-die capabilitv making it ideal in a varietyof powerapplications.Withthese improve-ments.multiple devices can be used in an appli-cation with dramatically reduced board space. The package is desianed fon vapor phase. inra rea. or wave so gerina technigues Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

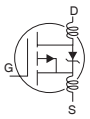
Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_A = 25°C	10 Sec. Pulsed Drain Current, V_{GS} @ -4.5V	-7.7	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ -4.5V	-6.7	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ -4.5V	-5.4	
I_{DM}	Pulsed Drain Current ①	-27	
P_D @T_A = 25°C	Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	℃

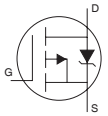
Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④		50	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20			V	V_{GS} = 0V, ID = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		-0.012		V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance			40	mΩ	V_{GS} = -4.5V, I_D = -3.2A ③
				60		V_{GS} = -2.7V, I_D = -2.7A ③
$V_{GS(th)}$	Gate Threshold Voltage	-0.70			V	V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	6.8			S	V_{DS} = -15V, I_D = -3.2A
I_{DSS}	Drain-to-Source Leakage Current			-1.0	μA	V_{DS} = -16V, V_{GS} = 0V
				-25		V_{DS} = -16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage			-100	nA	V_{GS} = -12V
	Gate-to-Source Reverse Leakage			100		V_{GS} = 12V
Q_g	Total Gate Charge			50	nC	I_D = -3.2A
Q_{gs}	Gate-to-Source Charge			5.5		V_{DS} = -16V
Q_{gd}	Gate-to-Drain ("Miller") Charge			21		V_{GS} = -4.5V, See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time		14		ns	V_{DD} = -10V
t_r	Rise Time		32			I_D = -3.2A
$t_{d(off)}$	Turn-Off Delay Time		100			R_G = 6.0Ω
t	Fall Time		65			R_D = 3.1Ω, See Fig. 10 ③
L_D	Internal Drain Inductance		2.5		nH	Between lead tip and center of die contact 
L_S	Internal Source Inductance		4.0			
C_{iss}	Input Capacitance		1500		pF	V_{GS} = 0V
C_{oss}	Output Capacitance		730			V_{DS} = -15V
C_{rss}	Reverse Transfer Capacitance		340			f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)			-3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①			-27		
V_{SD}	Diode Forward Voltage			-1.0	V	T_J = 25°C, I_S = -2.0A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time		69	100	ns	T_J = 25°C, I_F = -3.2A
Q_{rr}	Reverse RecoveryCharge		71	110	μC	di/dt = 100A/μs ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② I_{SD} ≤ -3.2A, di/dt ≤ -65A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t ≤ 10sec.

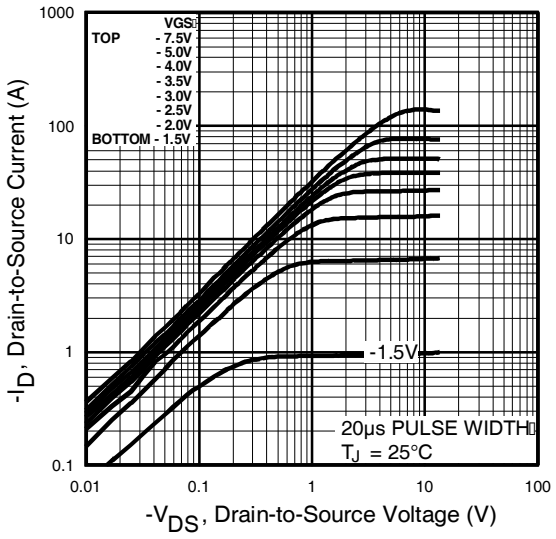


Fig 1. Typical Output Characteristics

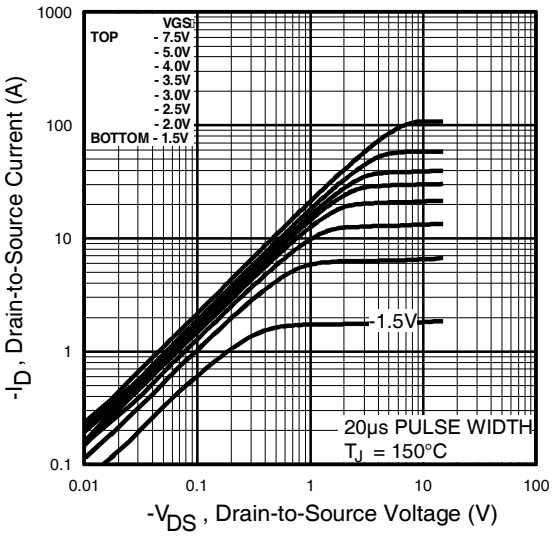


Fig 2. Typical Output Characteristics

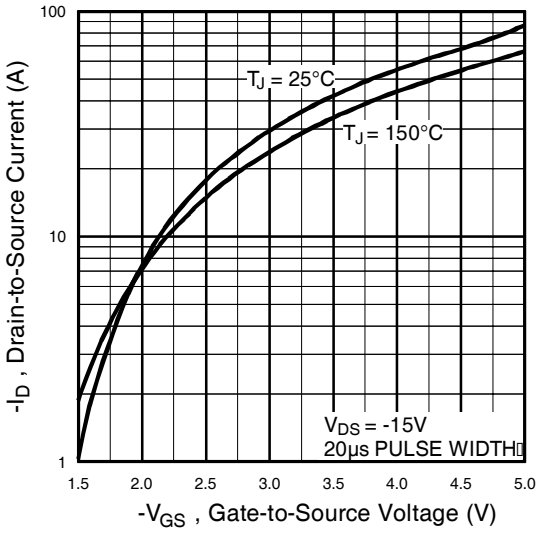


Fig 3. Typical Transfer Characteristics

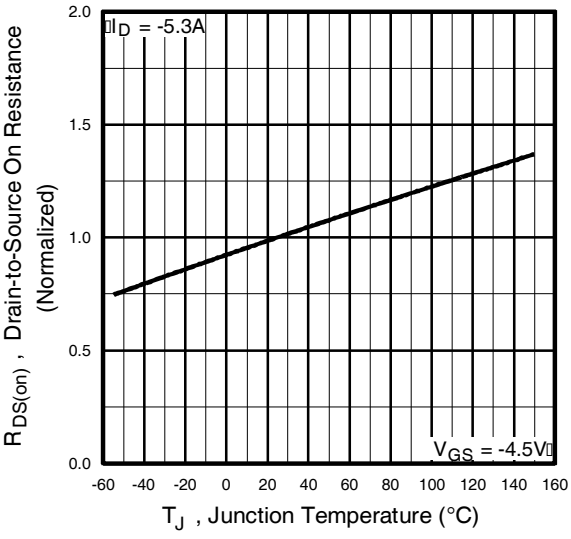


Fig 4. Normalized On-Resistance Vs. Temperature

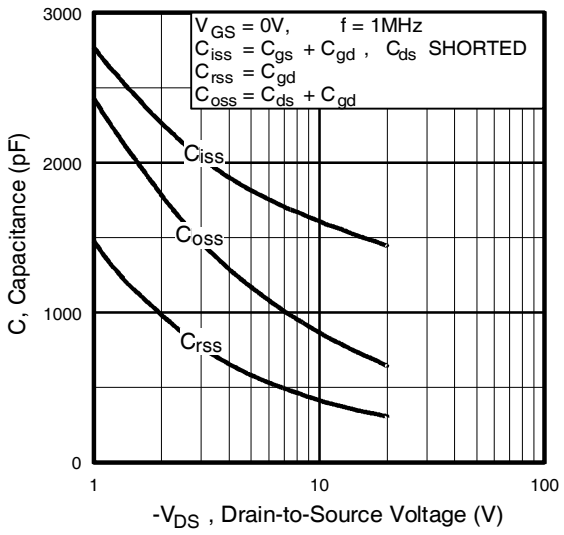


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

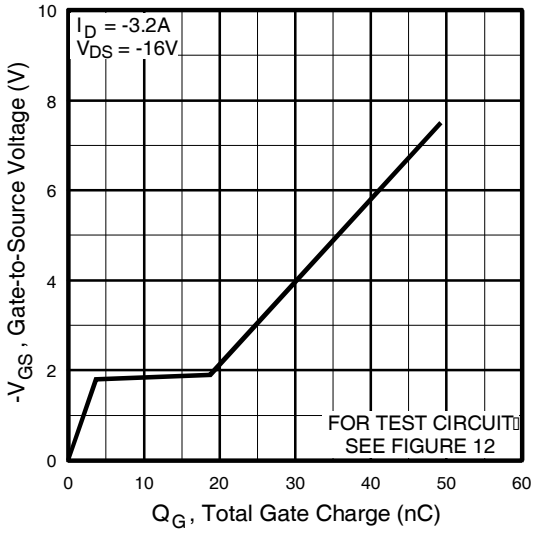


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

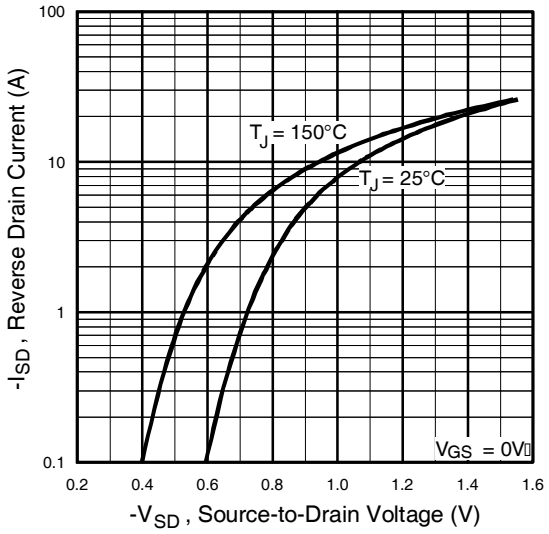


Fig 7. Typical Source-Drain Diode Forward Voltage

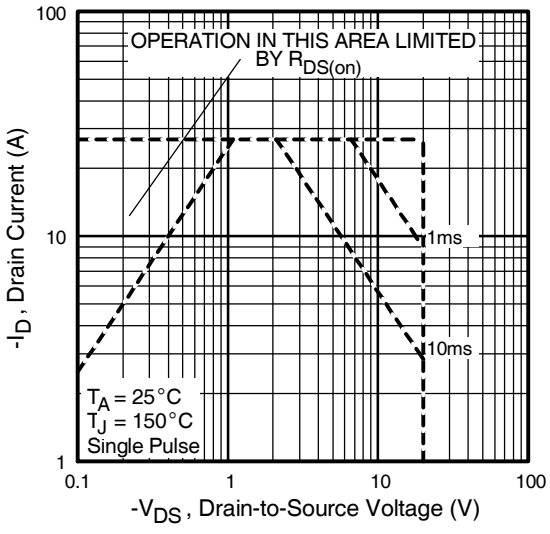


Fig 8. Maximum Safe Operating Area

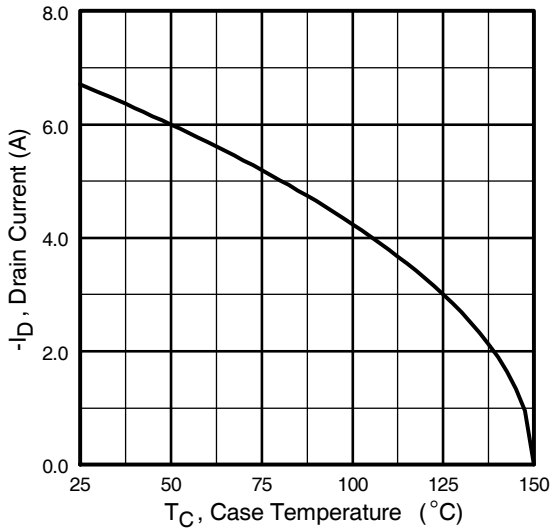


Fig 9. Maximum Drain Current Vs. Ambient Temperature

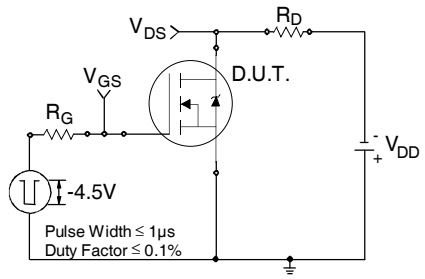


Fig 10a. Switching Time Test Circuit

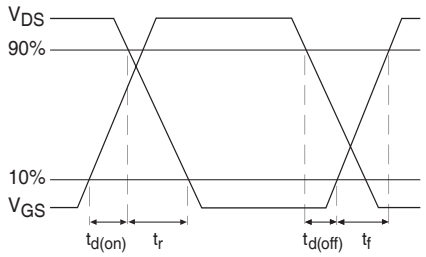


Fig 10b. Switching Time Waveforms

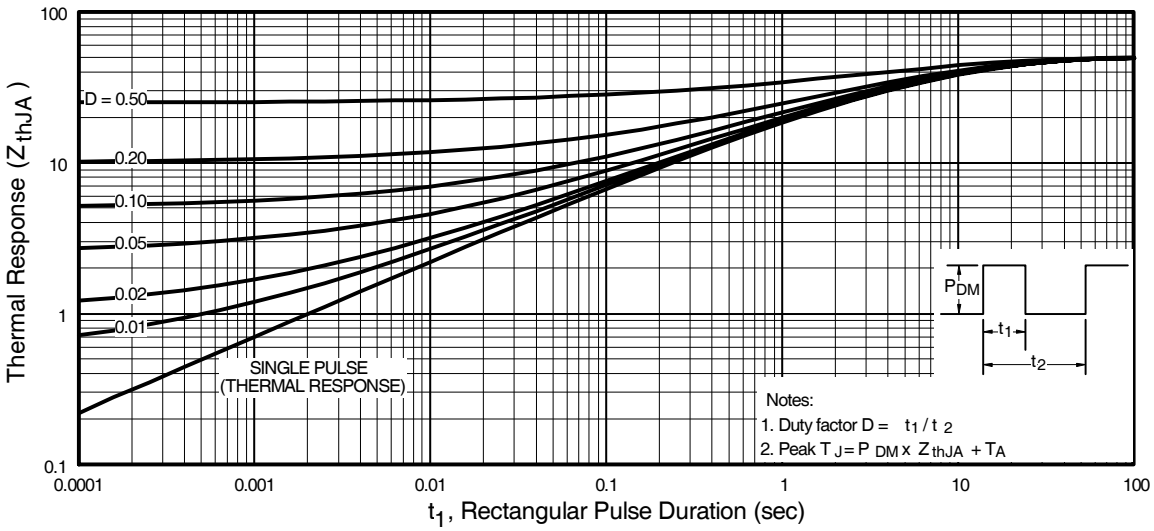


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

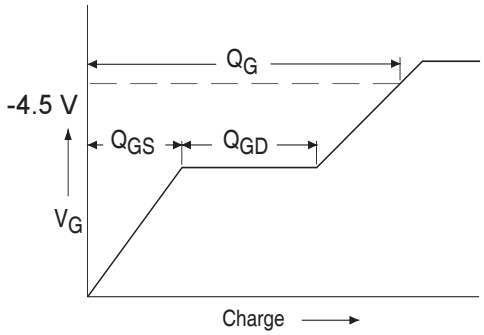


Fig 12a. Basic Gate Charge Waveform

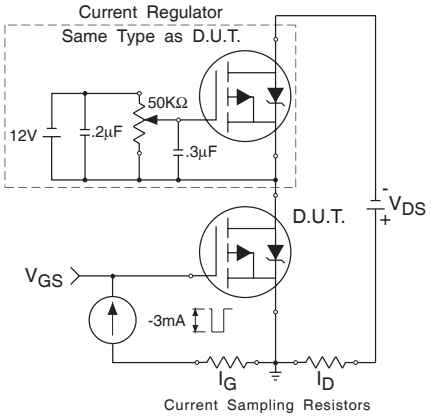
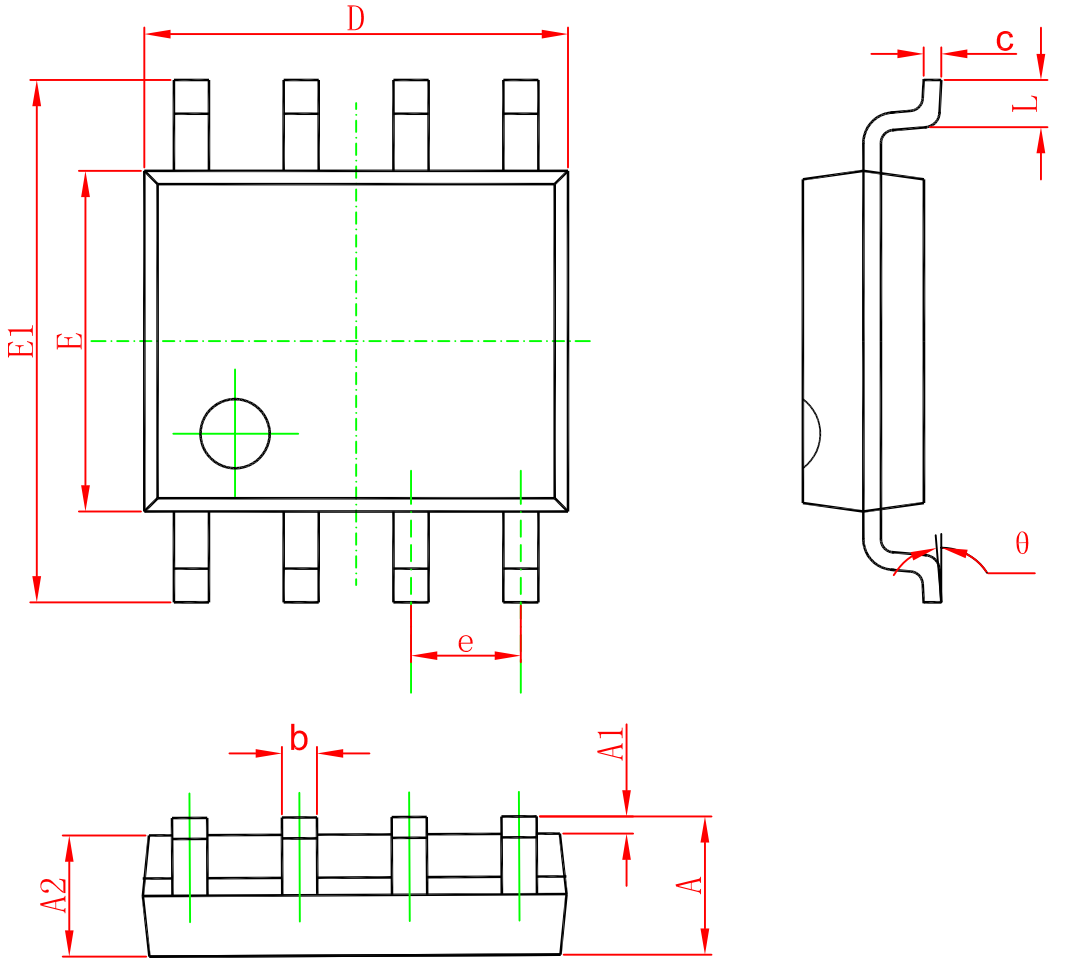


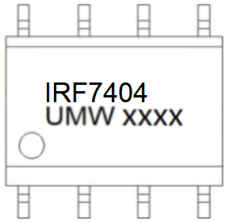
Fig 12b. Gate Charge Test Circuit

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRF7404TR	SOP-8	3000	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)