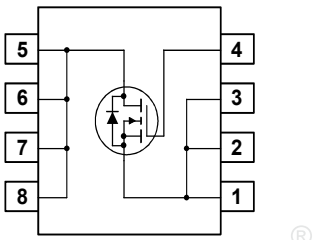
General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.



SOP-8

Applications

- DC/DC converters

Features

- $V_{DS\,(V)}$ =30V
- I_D= 10.2A (V_{GS} = 10V)
- $R_{DS(ON)}$ ＜14mΩ (V_{GS}=10V)
- $R_{DS(ON)}$ ＜17 mΩ (V_{GS}=4.5V)
- High performance trench technology for extremely low $r_{DS(on)}$
- Low gate charge
- High power and current handling capability
- RoHS Compliant

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 50°C/W)	10.2	A
	Continuous (T_A = 25°C, V_{GS} = 4.5V, $R_{\theta JA}$ = 50°C/W)	9.3	A
	Pulsed	80	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	57	mJ
P_D	Power dissipation	2.5	W
	Derate above 25°C	20	mW/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2b)	125	°C/W

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	μA
		V_{DS} = 24V, V_{GS} = 0V, T_J = 150°C			250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V			±100	nA
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.2		2.5	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 10.2A, V_{GS} = 10V		11.0	14.0	mΩ
		I_D = 9.3A, V_{GS} = 4.5V		13.8	17.0	mΩ
		I_D = 10.2A, V_{GS} = 10V, T_J = 150°C		17.5	22.7	mΩ
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		897		pF
C_{OSS}	Output Capacitance			190		pF
C_{RSS}	Reverse Transfer Capacitance			111		pF
R_G	Gate Resistance	V_{GS} = 0.5V, f = 1MHz	0.7	2.9	5.0	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V, V_{DD} = 15V, I_D = 10.2A, I_g = 1.0mA		17	26	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V, V_{DD} = 15V, I_D = 10.2A, I_g = 1.0mA		9	14	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V, V_{DD} = 15V, I_D = 10.2A, I_g = 1.0mA		0.9	1.4	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 15V, I_D = 10.2A, I_g = 1.0mA		2.5		nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 15V, I_D = 10.2A, I_g = 1.0mA		1.7		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 15V, I_D = 10.2A, I_g = 1.0mA		3.3		nC
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 10.2A, V_{GS} = 10V, R_{GS} = 16Ω			54	ns
$t_{d(ON)}$	Turn-On Delay Time			7		ns
t_r	Rise Time			29		ns
$t_{d(OFF)}$	Turn-Off Delay Time			45		ns
t_f	Fall Time			18		ns
t_{OFF}	Turn-Off Time				94	ns
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 10.2A			1.25	V
		I_{SD} = 2.1A			1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 10.2A, dI_{SD}/dt = 100A/μs			19	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 10.2A, dI_{SD}/dt = 100A/μs			9.5	nC

Notes:
1: Starting T_J = 25°C, L = 1mH, I_{AS} = 10.7A, V_{DD} = 30V, V_{GS} = 10V.
2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
a) 50°C/W when mounted on a $1in^2$ pad of 2 oz copper.
b) 125°C/W when mounted on a minimum pad.

Typical Characteristics T_J = 25°C unless otherwise noted

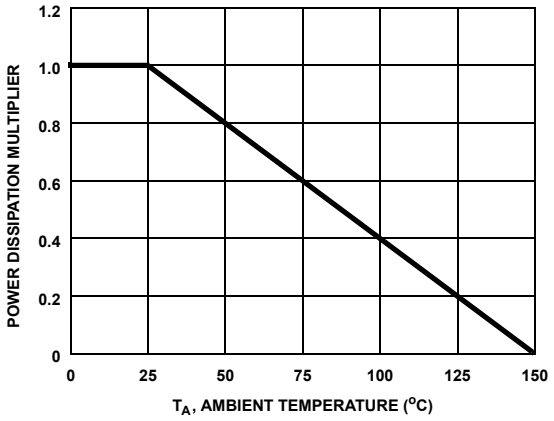


Figure 1. Normalized Power Dissipation vs Ambient Temperature

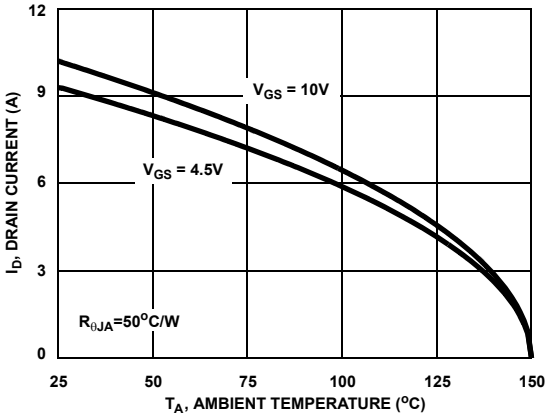


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

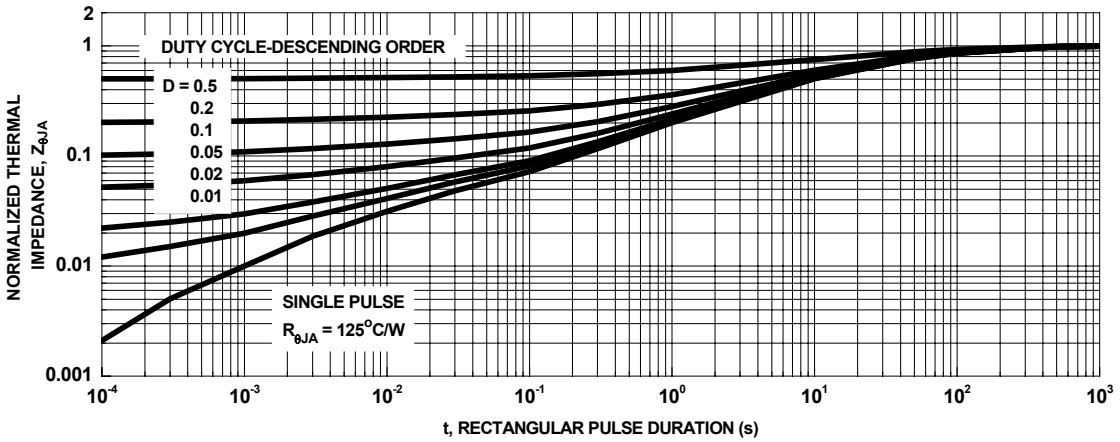


Figure 3. Normalized Maximum Transient Thermal Impedance

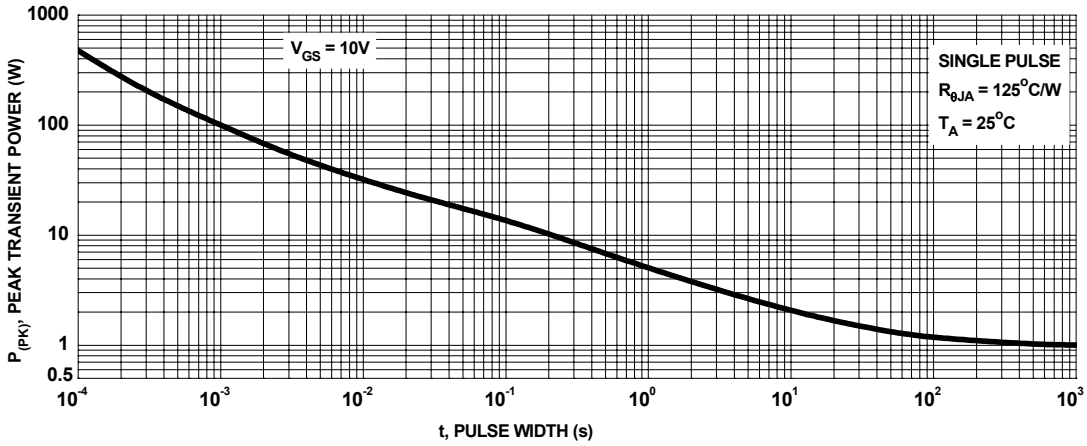


Figure 4. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

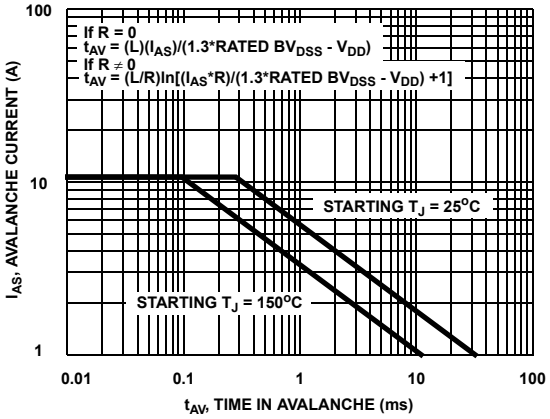


Figure 5. Unclamped Inductive Switching Capability

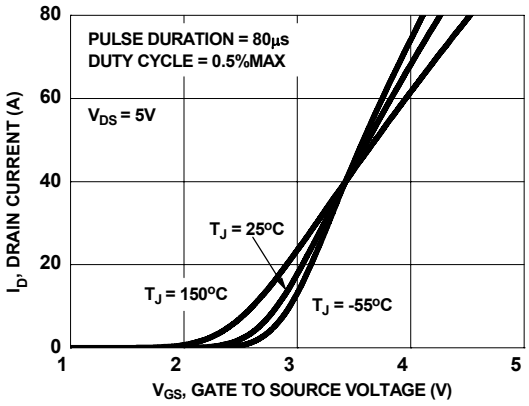


Figure 6. Transfer Characteristics

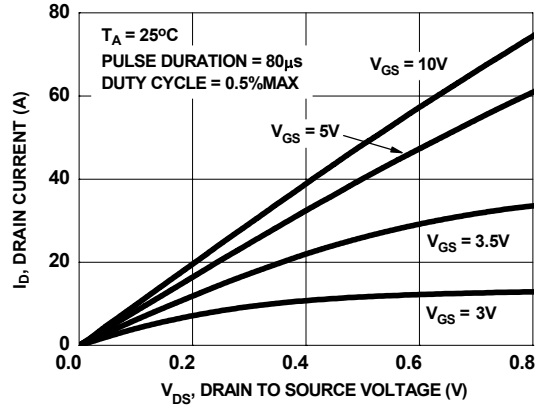


Figure 7. Saturation Characteristics

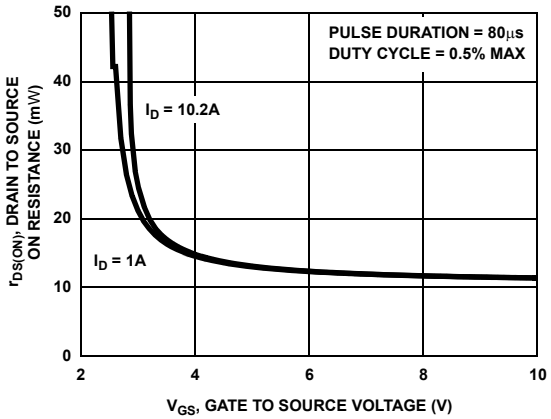


Figure 8. Drain to Source On Resistance vs Gate Voltage and Drain Current

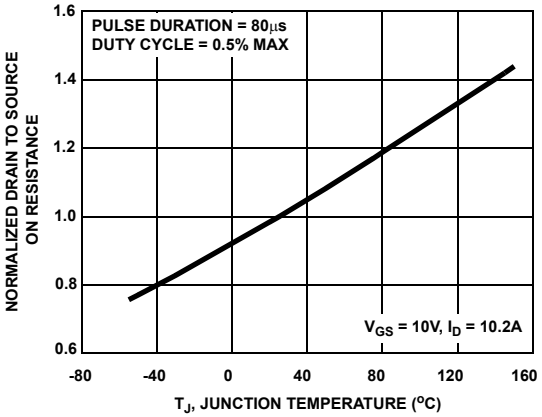


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

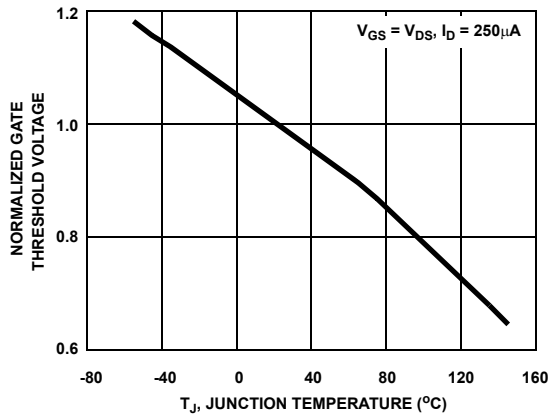


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics T_J = 25°C unless otherwise noted

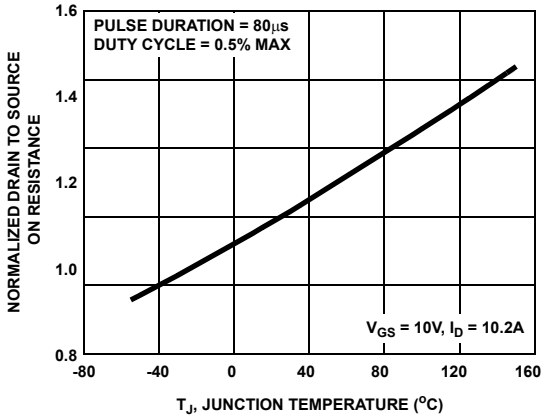


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

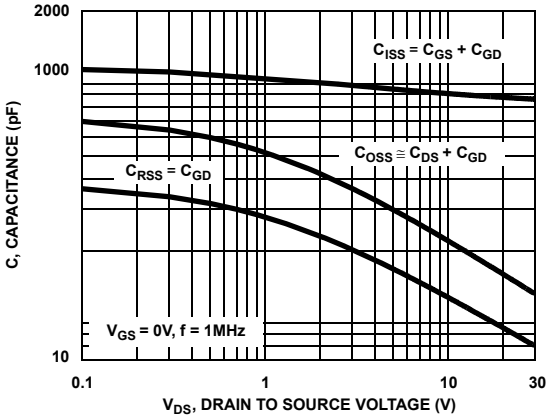


Figure 12. Capacitance vs Drain to Source Voltage

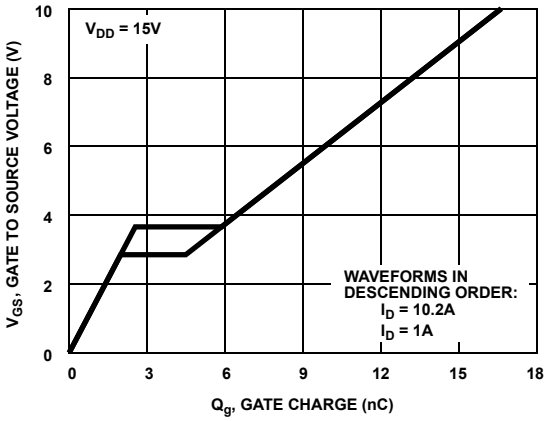


Figure 13. Gate Charge Waveforms for Constant Gate Currents

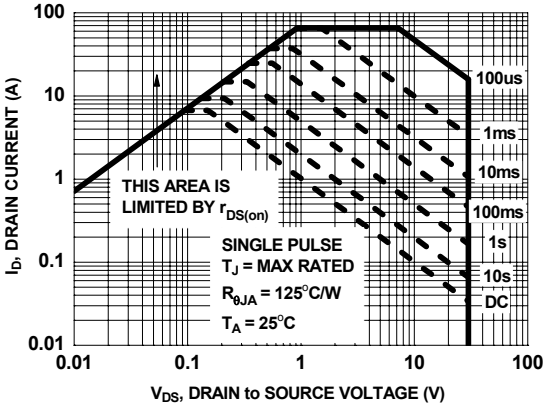


Figure 14. Forward Bias Safe Operating Area

Test Circuits and Waveforms

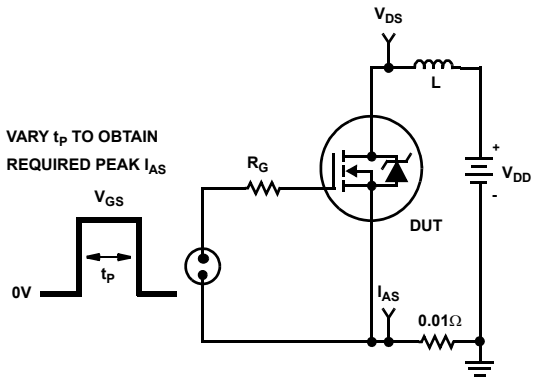


Figure 15. Unclamped Energy Test Circuit

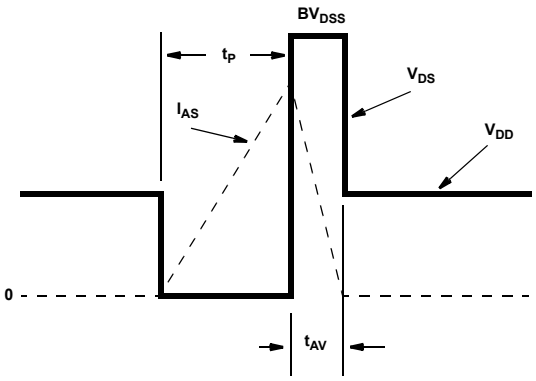


Figure 16. Unclamped Energy Waveforms

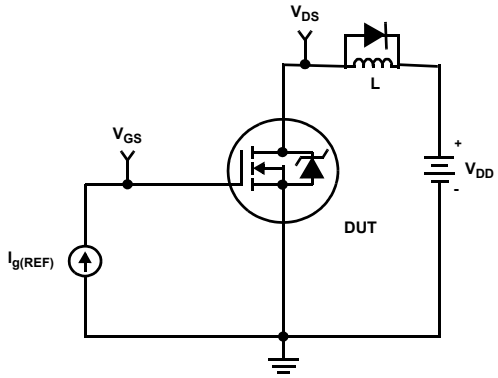


Figure 17. Gate Charge Test Circuit

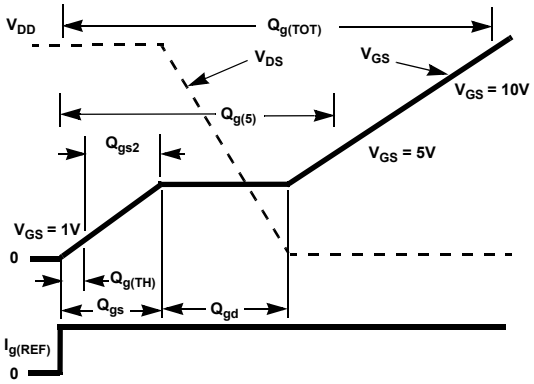


Figure 18. Gate Charge Waveforms

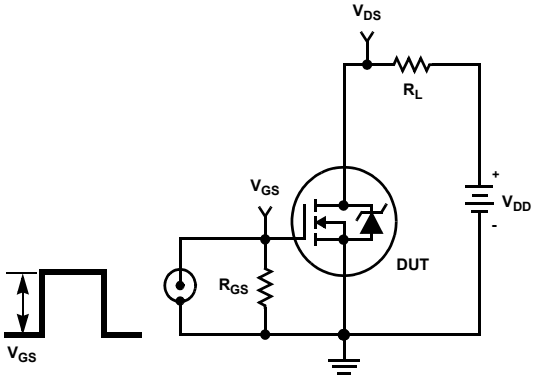


Figure 19. Switching Time Test Circuit

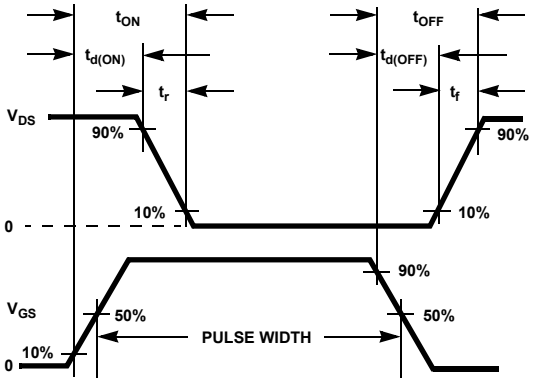
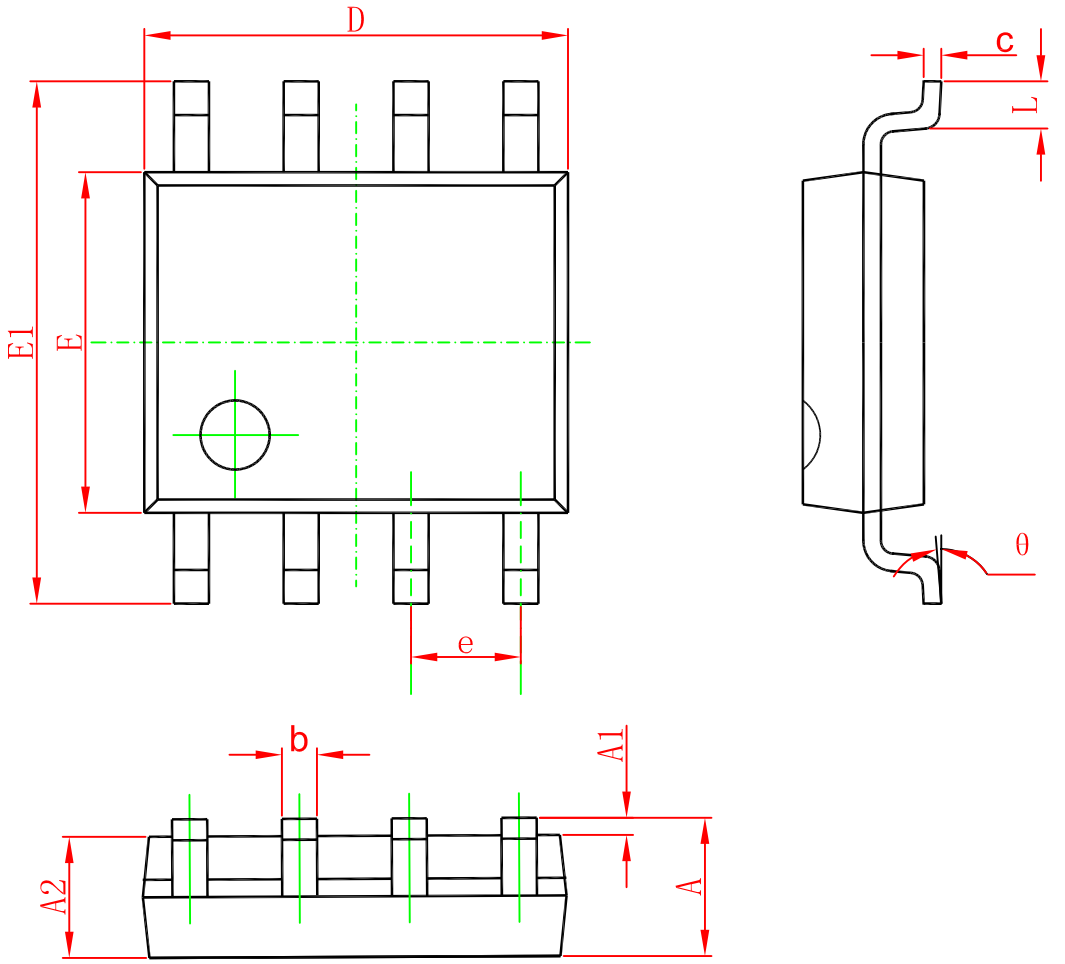


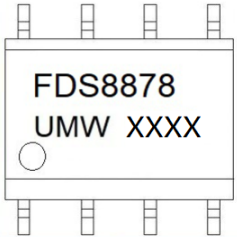
Figure 20. Switching Time Waveforms

Package Mechanical Data SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDS8878	SOP-8	3000	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)