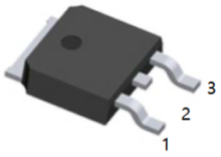
60V N-Channel MOSFET

Features

- Deal for high frequency switching
- Optimized technology for DC / DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$

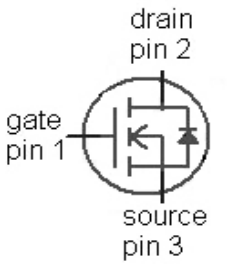


1.G 2.D 3.S

TO-252(DPAK) top view

Product Summary

- V_{DS}(V) = 60V
- I_D = 50A (V_{GS}= 10V)
- $R_{DS(ON)}$ < 8.8mΩ (V_{GS} = 10V)



MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2)]	50	A
		T_C=100 °C	47	
Pulsed drain current[3)]	$I_{D,pulse}$	T_C=25 °C	200	
Avalanche energy, single pulse[4)]	E_{AS}	I_D=50 A, R_{GS}=25 Ω	43	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	71	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1)] J-STD20 and JESD22

[2)] Current is limited by bondwire; with an R_{thJC}=2.1 K/W the chip is able to carry 67 A.

[3)] See figure 3 for more detailed information

[4)] See figure 13 for more detailed information

Electrical characteristics, at T_j=25°C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}				2.1	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint			62	
		6 cm² cooling area[4)]			40	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	60			
V Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=34 µA	2	3	4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C		0.1	1	µA
		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C		10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V		1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=50 A		7.1	8.8	mΩ
Gate resistance	R_G			0.9		Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	29	57		S

[4)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

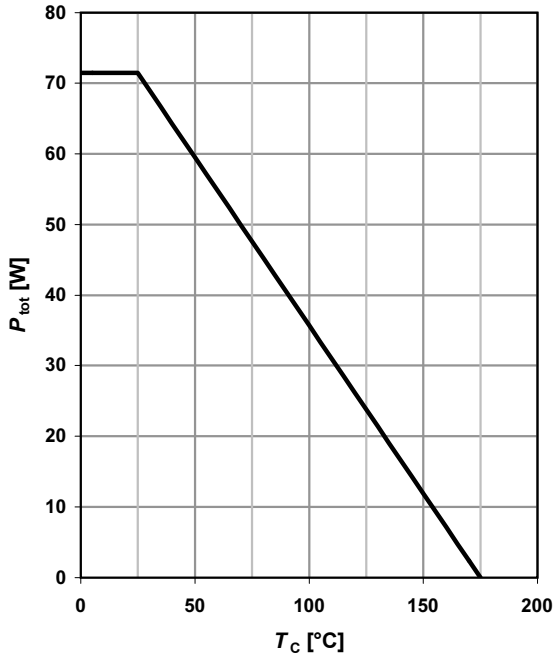
Dynamic characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz		2900	3900	pF
Output capacitance	C_{oss}			640	850	
Reverse transfer capacitance	C_{rss}			23		
Turn-on delay time	$t_{d(on)}$	V_{DD}=30 V, V_{GS}=10 V, I_D=45 A, R_G=3.5 Ω		15		ns
Rise time	t_r			40		
Turn-off delay time	$t_{d(off)}$			20		
Fall time	t_f			5		
Gate to source charge	Q_{gs}	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 10 V		16		nC
Gate to drain charge	Q_{gd}			3		
Switching charge	Q_{sw}			11		
Gate charge total	Q_g			36	48	
Gate plateau voltage	$V_{plateau}$			5.6		V
Output charge	Q_{oss}	V_{DD}=30 V, V_{GS}=0 V		29	38	nC
Diode continous forward current	I_S	T_C=25 °C			50	A
Diode pulse current	$I_{S,pulse}$				200	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C		1.0	1.2	V
Reverse recovery time	t_{rr}	V_R=30 V, I_F=45A, di_F/dt=100 A/µs		45		ns
Reverse recovery charge	Q_{rr}			40		nC

[5] See figure 16 for gate charge parameter definition

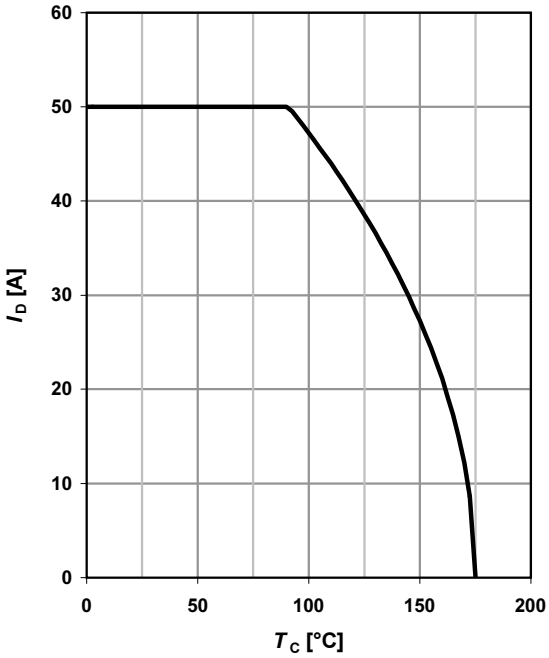
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

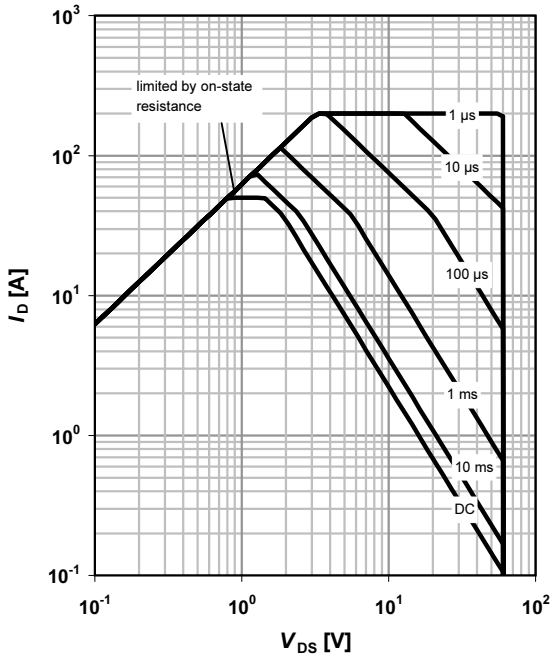
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

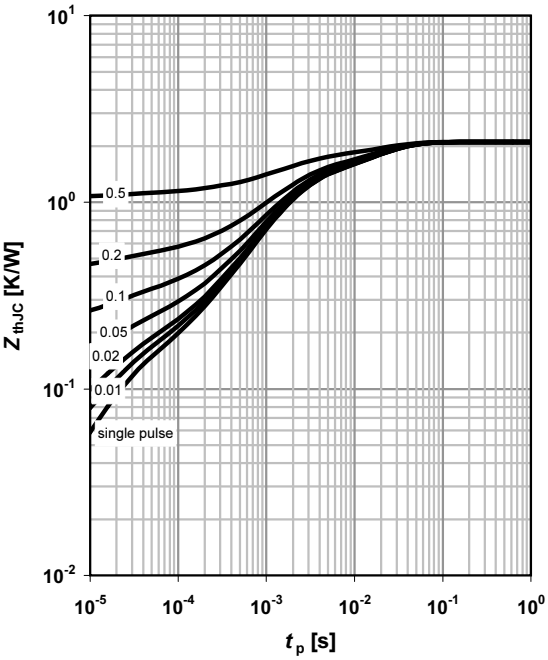
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

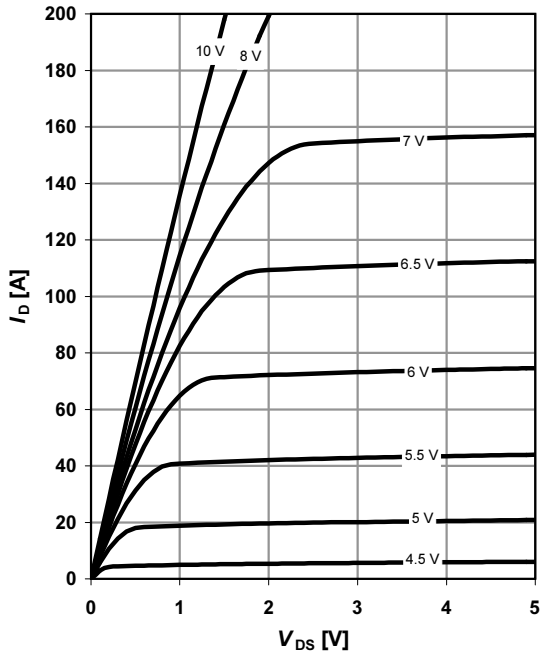
parameter: $D=t_p/T$



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

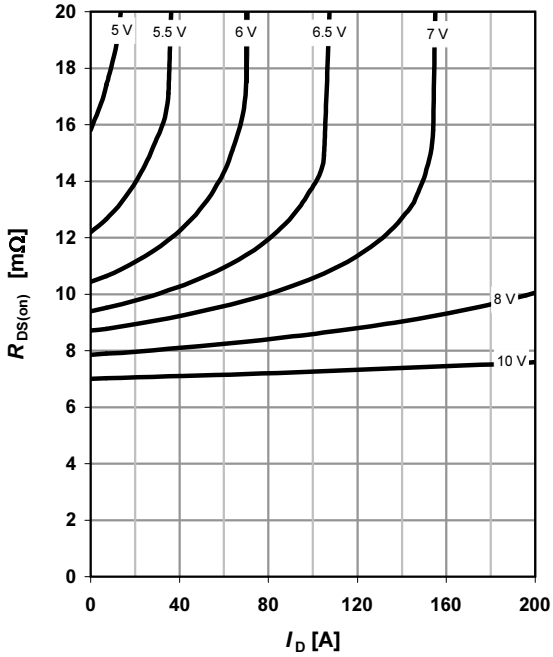
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

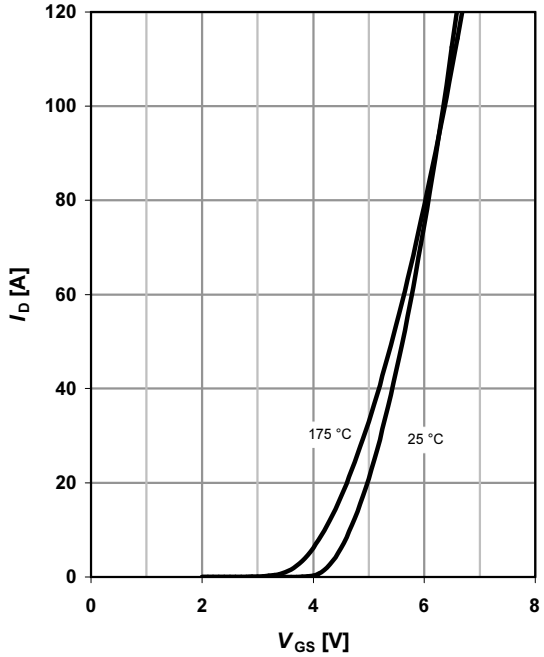
parameter: V_{GS}



7 Typ. transfer characteristics

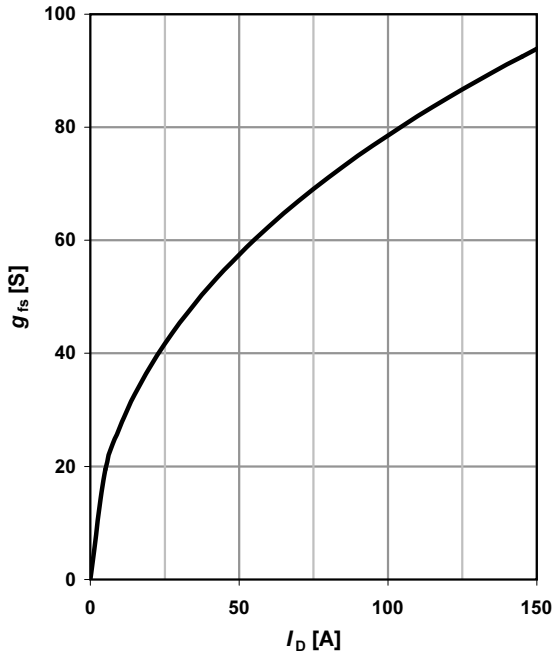
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$

parameter: T_j



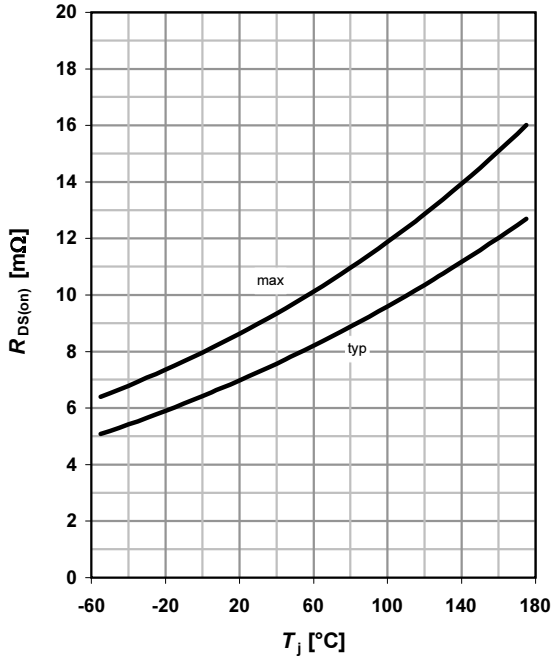
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



9 Drain-source on-state resistance

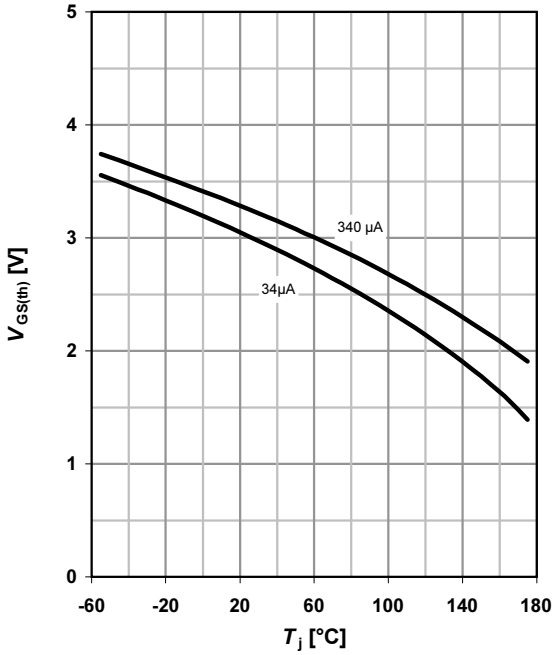
$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V



10 Typ. gate threshold voltage

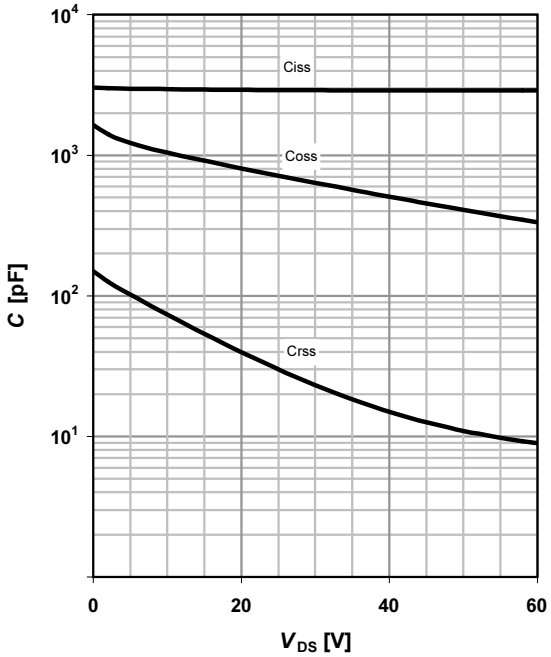
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

parameter: I_D



11 Typ. capacitances

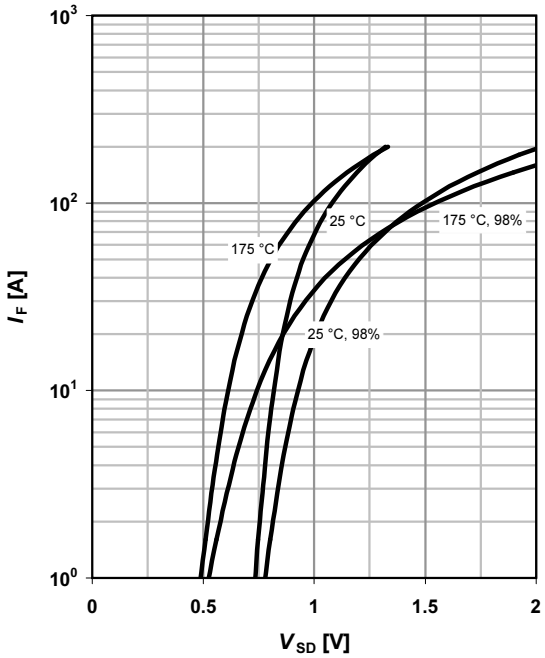
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

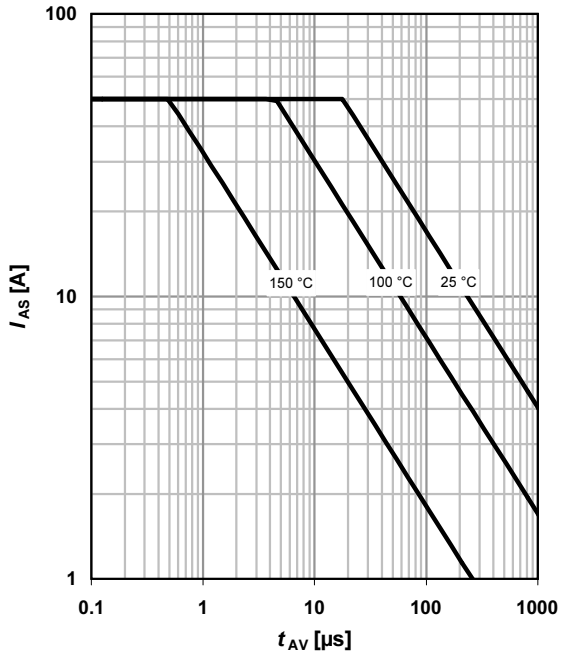
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

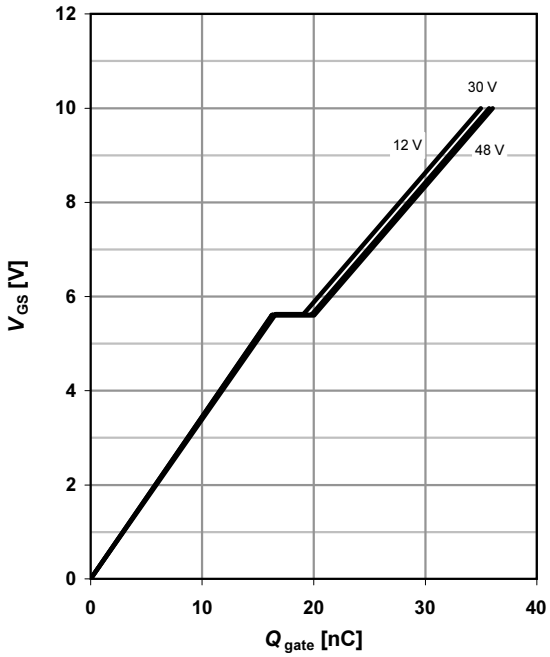
parameter: $T_{j(start)}$



14 Typ. gate charge

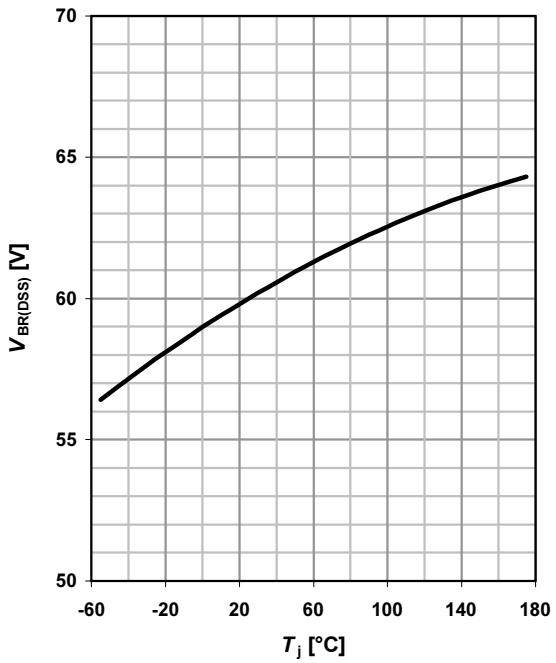
V_{GS}=f(Q_{gate}); I_D=50 A pulsed

parameter: V_{DD}

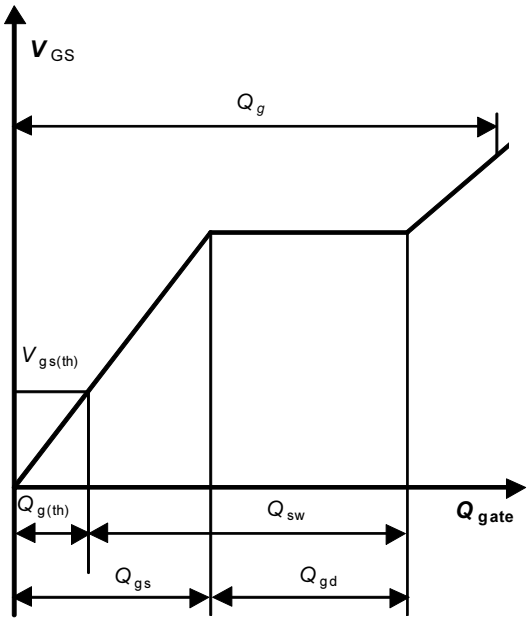


15 Drain-source breakdown voltage

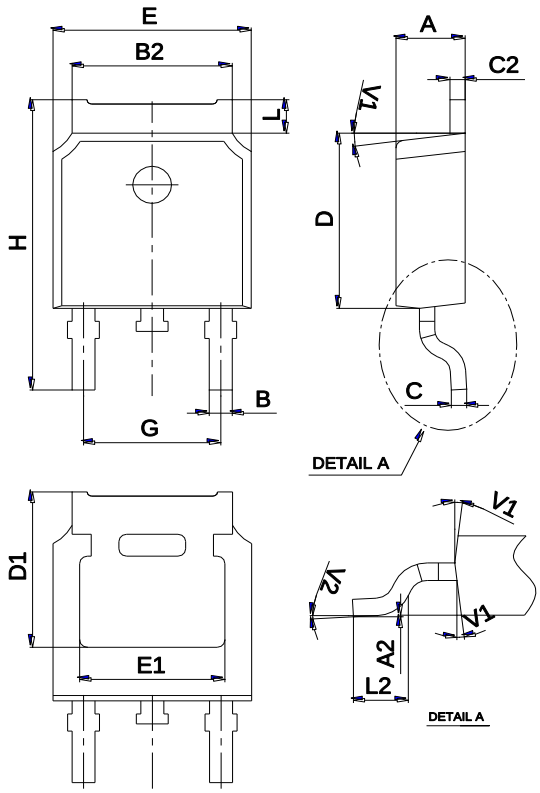
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IPD088N06N3G	TO-252	2500	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)