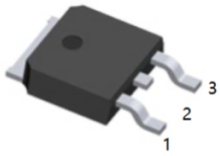
60V N-Channel MOSFET

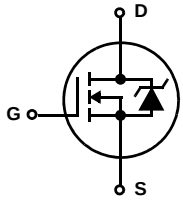
Features

- V_{DS} (V) = 60V
- $R_{DS(ON)}$ <100mΩ（V_{GS}= 5V）
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- 175℃ Operating Temperature



1.G 2.D 3.S

TO-252(DPAK) top view



Absolute Maximum Ratings

T_C = 25℃, Unless Otherwise Specified

Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	14	A
Pulsed Drain Current (Note 3)	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating.	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	48	W
Derate above 25^{o}C		0.32	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^{o}C

NOTE:

1. T_J = 25^{o}C to 150^{o}C.

Electrical Specifications T_C = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V, Figure 13		60			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA, Figure12		1		2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V				1	μA
		V_{DS} = 40V, V_{GS} = 0V, T_C = 150°C				50	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V				±100	nA
Drain to Source On Resistance (Note 2)	$R_{DS(ON)}$	I_D = 14A, V_{GS}= 5V, Figures 9, 11				100	mΩ
Turn-On Time	$t_{(ON)}$	V_{DD} = 25V, I_D = 7A, R_L = 3.57Ω, V_{GS} = 5V, R_{GS} = 0.6Ω				60	ns
Turn-On Delay Time	$t_{d(ON)}$				13		ns
Rise Time	t_r				24		ns
Turn-Off Delay Time	$t_{d(OFF)}$				42		ns
Fall Time	t_f				16		ns
Turn-Off Time	$t_{(OFF)}$					100	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 40V, I_D = 14A, R_L = 2.86Ω Figures 20, 21			40	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0V to 5V				25	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V				1.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz Figure 14			670		pF
Output Capacitance	C_{OSS}				185		pF
Reverse Transfer Capacitance	C_{RSS}				50		pF
Thermal Resistance Junction to Case	$R_{\theta JC}$					3.125	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-252				100	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 14A			1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 14A, dI_{SD}/dt = 100A/μs			125	ns

NOTES:

2. Pulse Test: Pulse Width ≤300ms, Duty Cycle ≤2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature. See Transient Thermal Impedance Curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves Unless Otherwise Specified

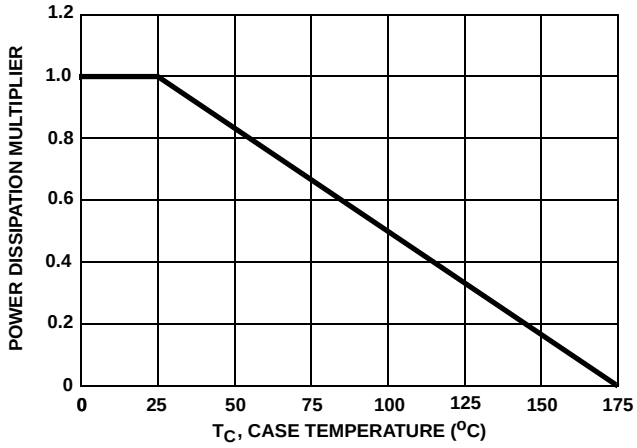


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

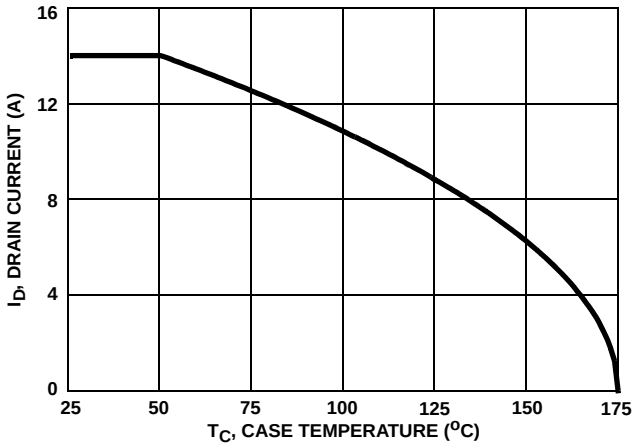


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

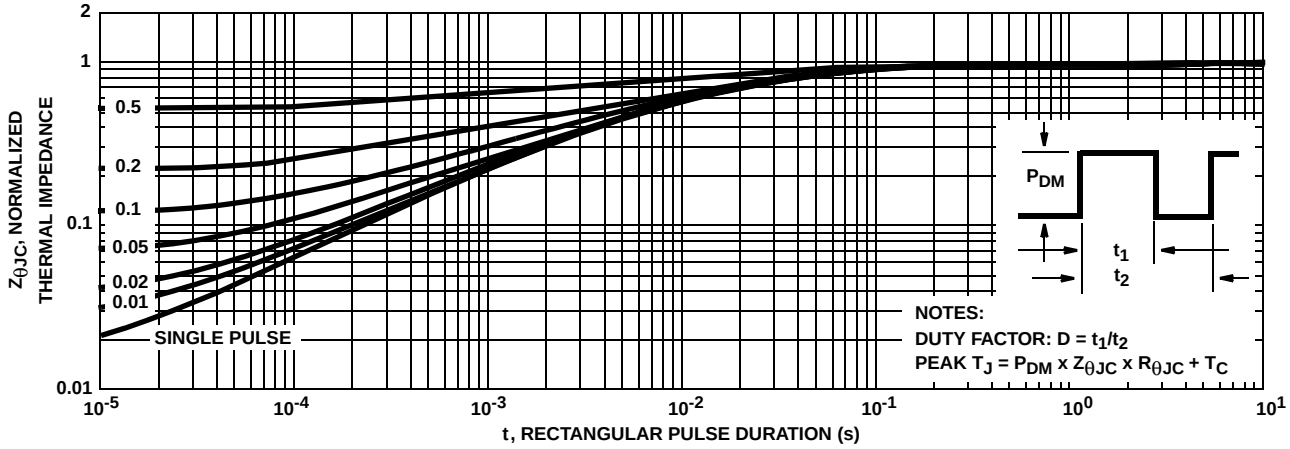


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

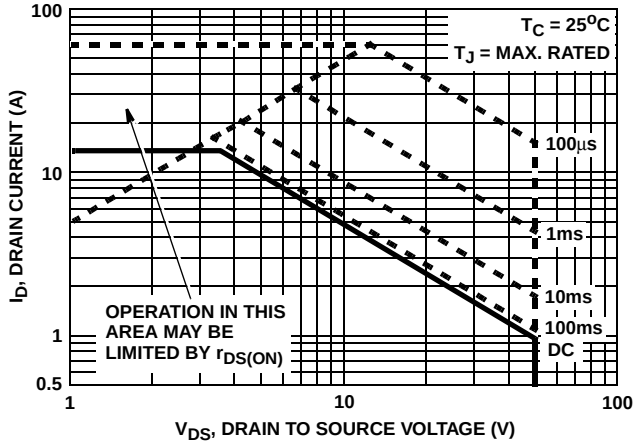


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

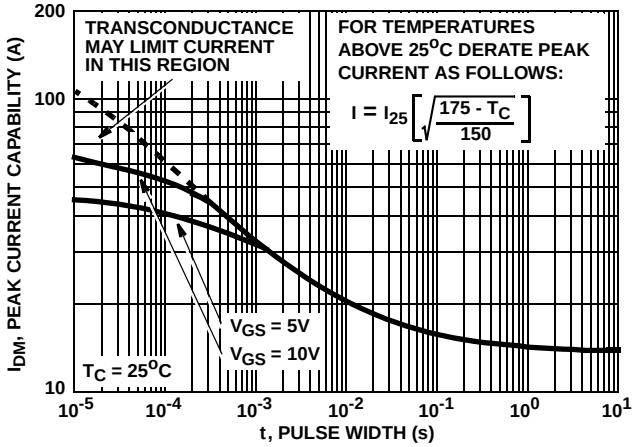


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified

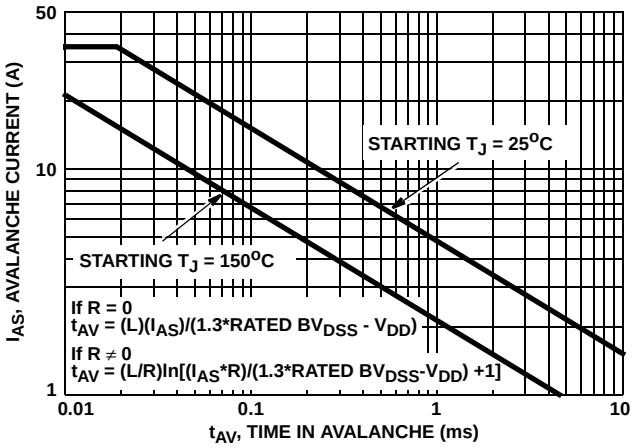


FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

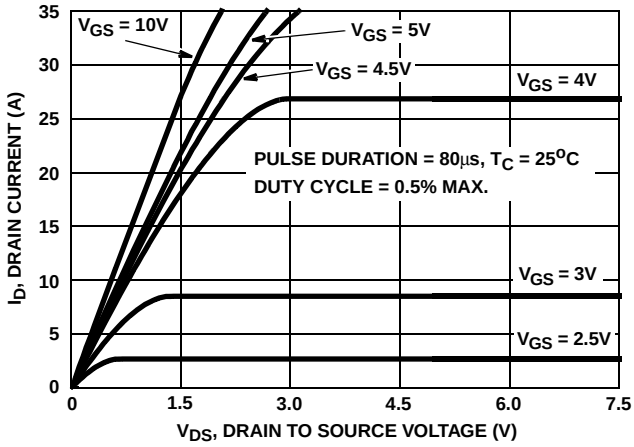


FIGURE 7. SATURATION CHARACTERISTICS

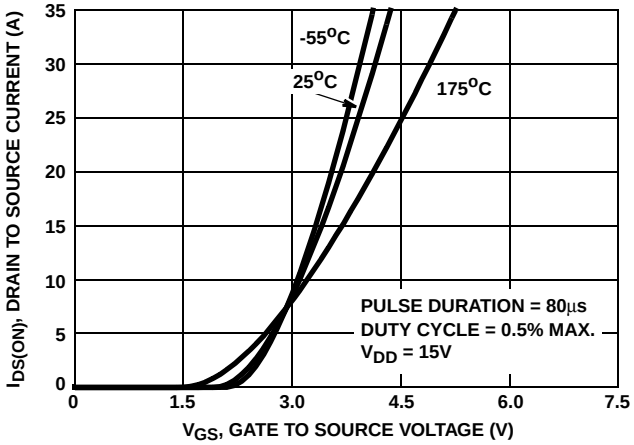


FIGURE 8. TRANSFER CHARACTERISTICS

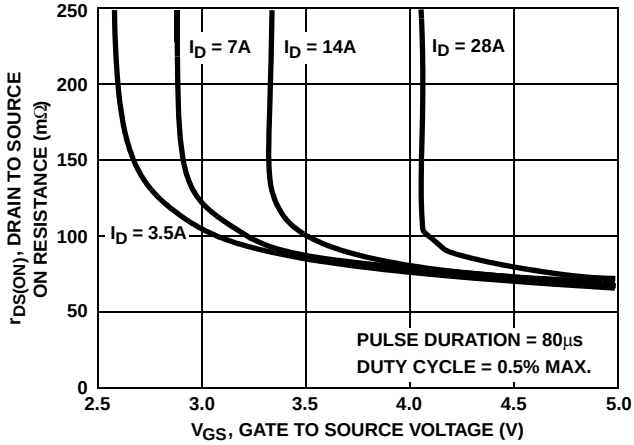


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

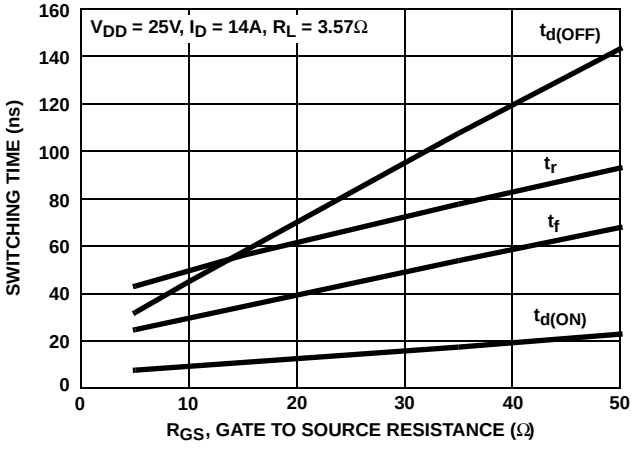


FIGURE 10. SWITCHING TIME vs GATE RESISTANCE

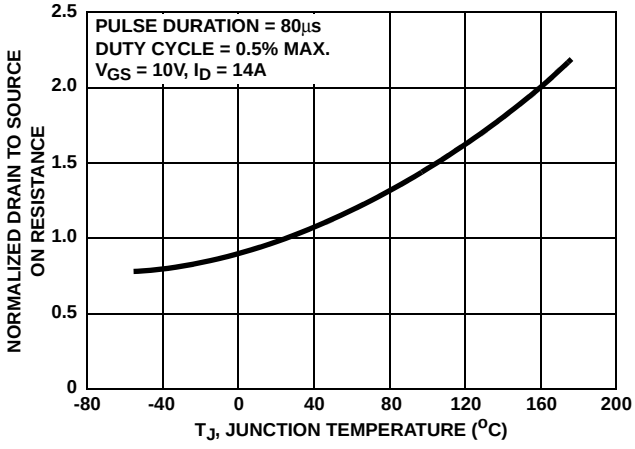


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified

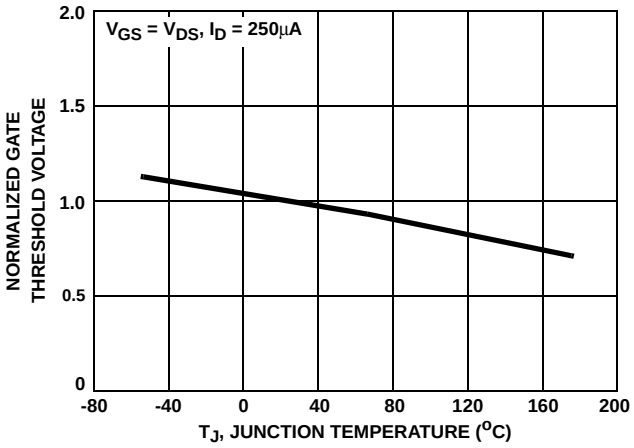


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

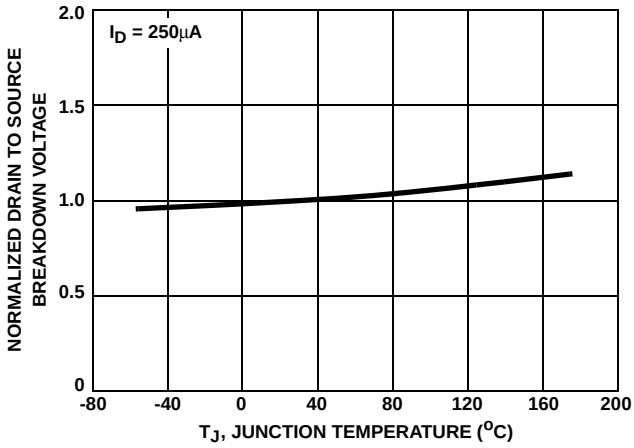


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

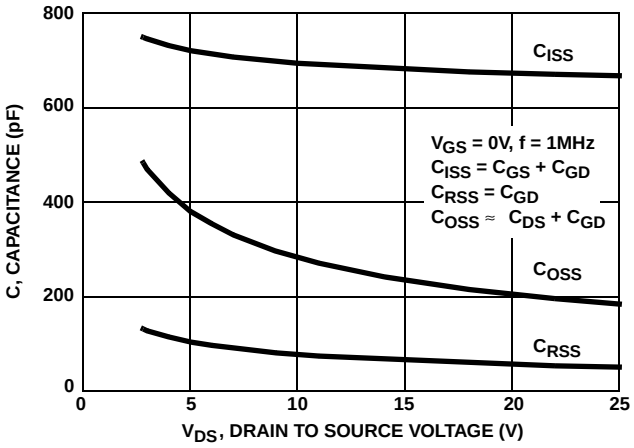


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

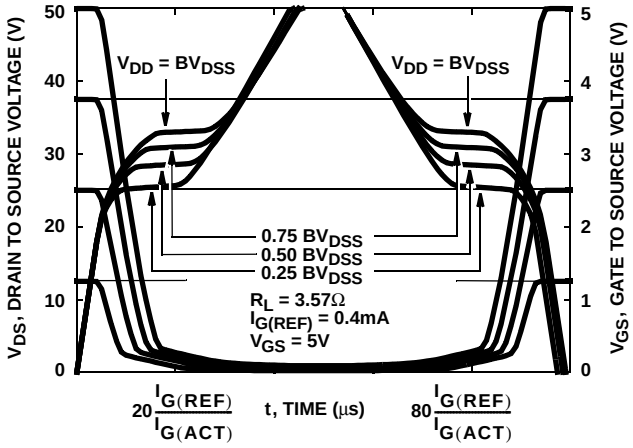


FIGURE 15. TRANSCONDUCTANCE vs DRAIN CURRENT

Test Circuits and Waveforms

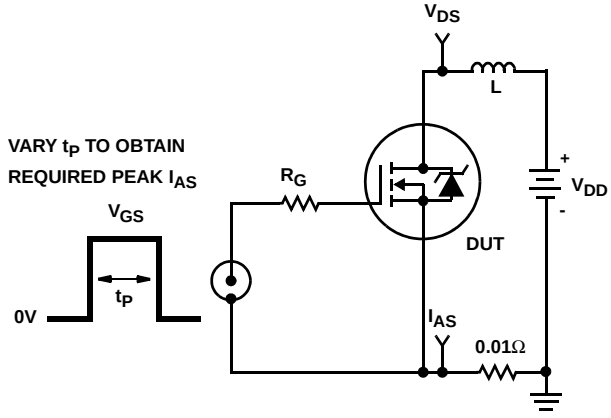


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

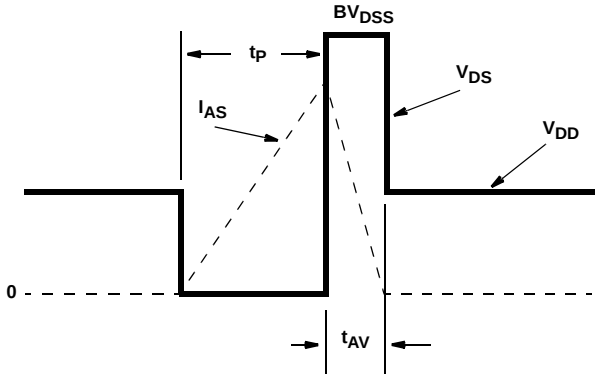


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms

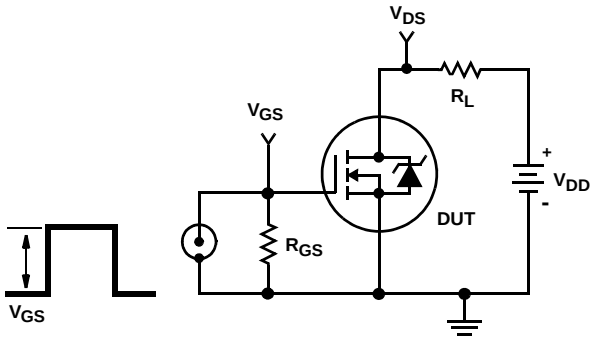


FIGURE 18. SWITCHING TIME TEST CIRCUIT

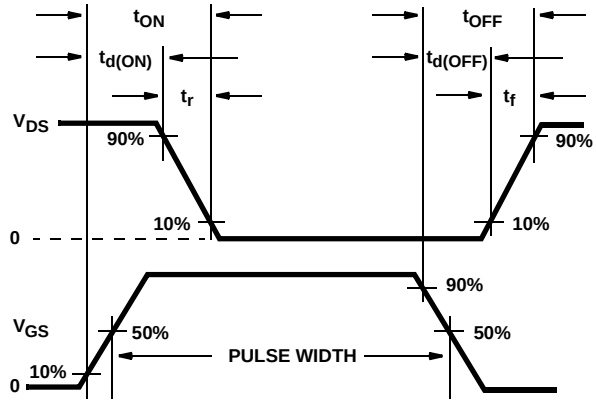


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

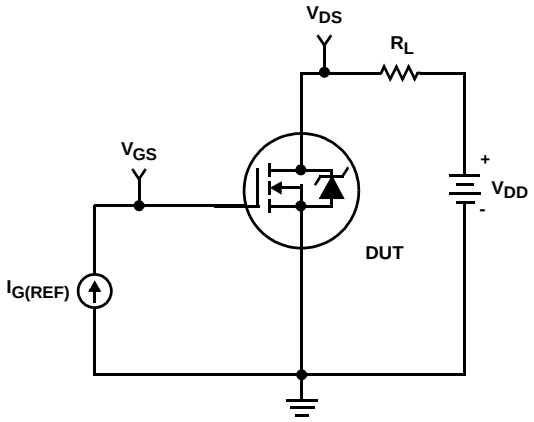


FIGURE 20. GATE CHARGE TEST CIRCUIT

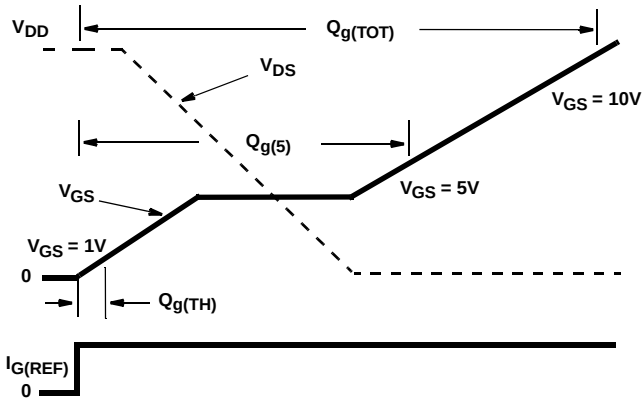
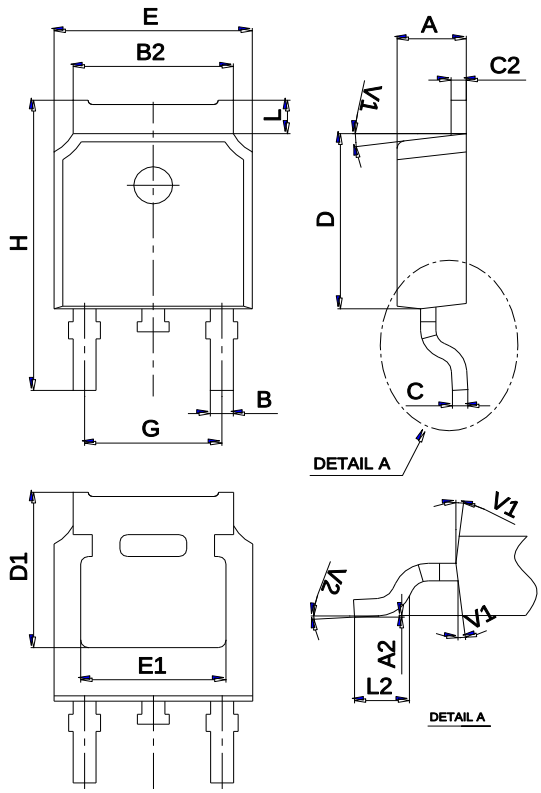


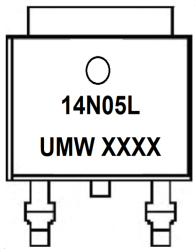
FIGURE 21. GATE CHARGE WAVEFORMS

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW RFD14N05LSM	TO-252	2500	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)