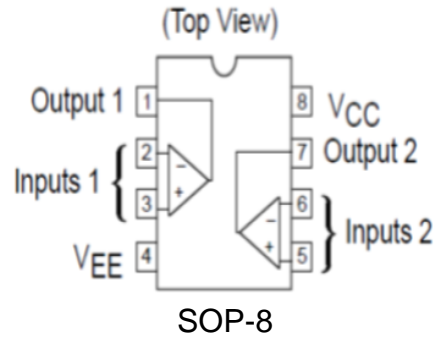


Summary

This type of J-FET input operational amplifier is specially designed for low-power applications, which are characterized by high input impedance, low input bias current and low input offset current.

Advanced design technology ensures higher conversion rate, gain bandwidth product and output swing. Commercial and vehicle equipment can be packaged in plastic dipline SOP.

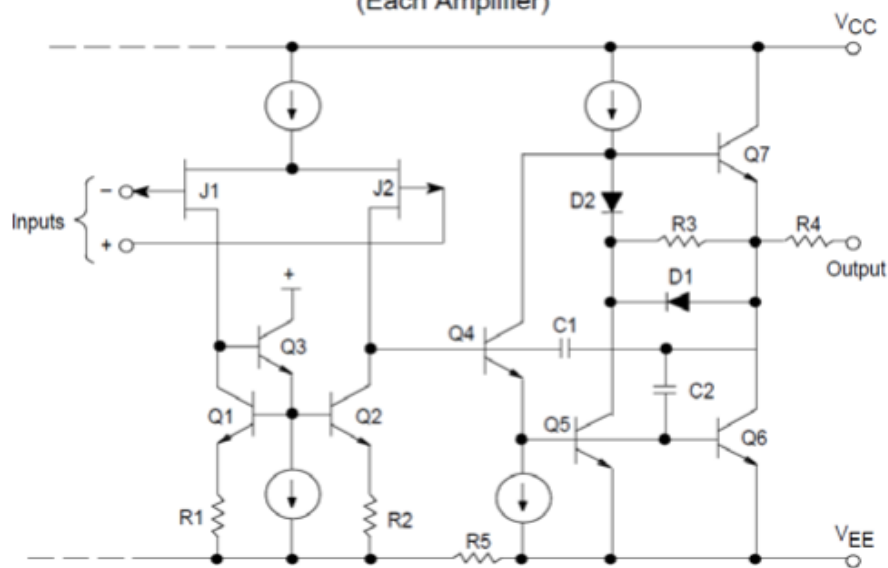
PIN CONNECTIONS



Main feature

- Low power supply current: 200uA/Amplifier
- Low input bias current: 5.0pA
- High gain bandwidth: 2.0MHz
- High conversion rate: 6.0V/uS
- High input impedance: 10¹²Ω
- Large output voltage swing: ±14V
- Output short circuit protection

Representative Schematic Diagram
(Each Amplifier)



Low power J - FET input operational amplifier
Maximum rating

category	symbol	value	unit
Power supply (from VCC to VEE)	VS	+36	V
Input differential voltage range (Note 1)	V_{DR}	± 30	V
Input voltage range (Note 1 and Note2)	V_{IR}	± 15	V
Output Short Circuit Duration (Note 3)	tsc	need to be decided or settled	sec
operating junction temperature range	T_J	+125	°C
Storage temperature range	T_{stg}	- 60 to +150	°C

- Note: 1. The differential voltage is located at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must not exceed the amplitude of the supply voltage of 15 volts, whichever is smaller.
3. Power consumption must be considered to ensure that the maximum junction temperature is not exceeded.

Electrical characteristics (Vcc=20V, T_{amp}=25°C shall be specified separately)

parameter	symbol	TL062C			unit
		Min	Typ	Max	
Input offset voltage (RS =50Ω, VO = 0V) TA=25°C TA=0°C to +70°C	V_{io}		3.0	15 20	mV
Average temperature coefficient of offset voltage (RS=50Ω VO=0V)	$\Delta V_{io} / \Delta T$		10		uV/°C
Input offset current (VCM=0V, VO=0V) TA=25°C TA=0°C to +70°C	I_{io}		0.5	200 2	pA nA
Input bias current (VCM=0V, VO=0V) TA=25°C TA=0°C to +70°C	I_{IB}		3	200 10	pA nA
Input common- mode voltage range TA=25°C	V_{ICR}	- 11	+14.5 - 12	+11	V
Large signal voltage gain (RL = 10kΩ, VO = ±10V0) TA=25°C TA=0°C to +70°C	A_{VOL}	3.0 3.0	58		V/mV
Output voltage amplitude (RL=10KΩ, VID=10 V0) TA=25°C TA=0°C to +70°C	V_{o+} V_{o-} V_{o+} V_{o-}	+10 +10	+14 - 14	- 10 - 10	V
common mode rejection ratio RS=50Ω VCM=VICR min, VO=0V, TA=25°C	CMR	70	84		dB

Low power J - FET input operational amplifier

common mode rejection ratio (RS=50Ω, VCM=0V, VO=0V, TA=25°C)	PSR	70	86		dB
Supply current (per independent op amp) (No load, VO=0V, TA=25°C)	I _D		200	250	uA
Total power consumption (per independent operational amplifier) (No load, VO=0V, TA=25°C)	P _D		6.0	7.5	mW

Ac electrical characteristics (VCC=+15V, VEE= - 15V, TA= +25°C unless otherwise specified).

parameter	symbol	Min	Typ	Max	unit
Conversion rate (vin =- 10V to+10V, RL = 10KΩ, CL = 100PF, AV=+1.0)	SR	2.0	5.0		V/uS
Rise time (Vin = 20mV, RL = 10kΩ, CL = 100pf, AV =+1.0).	Tr		0.1		uS
Deviation value (vin = 20mv, rl = 10kΩ, cl = 100pf, av =+1.0).	OS		10		%
setting time (VCC=+15V, VEE= - 15V, AV=+1.0, RL=10kΩ, VO=0V to +10V step)	t _s		1.5 2.2		uS
Gain bandwidth product (f=200KHz)	GBW		2.0		MHz
Equivalent input noise (RS=100Ω, f=1.0KHz)	e _n		47		nV/sqrt(Hz)
Input resistance	R _i		10 ¹²		W
Channel separation (f=10KHz)	CS		120		dB

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

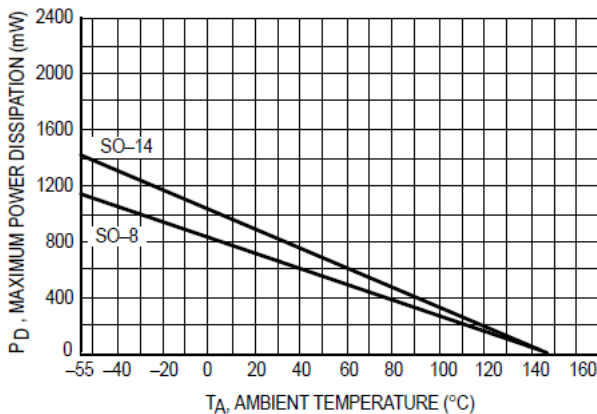
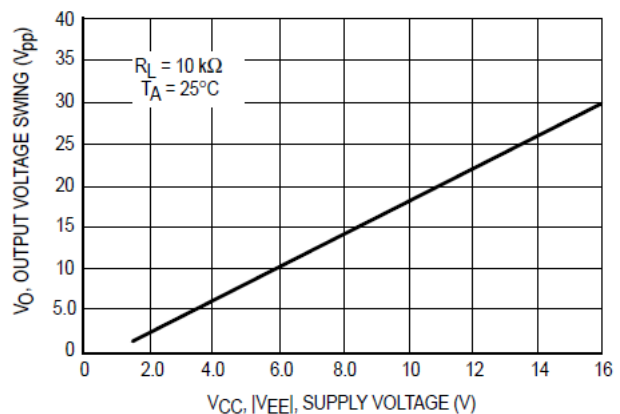


Figure 2. Output Voltage Swing versus Supply Voltage



Low power J - FET input operational amplifier

Figure 3. Output Voltage Swing versus Temperature

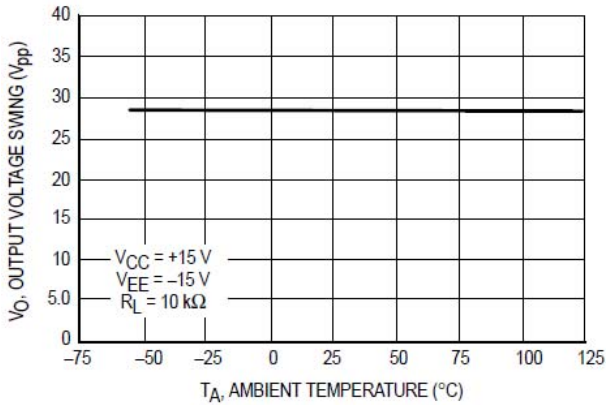


Figure 4. Output Voltage Swing versus Load Resistance

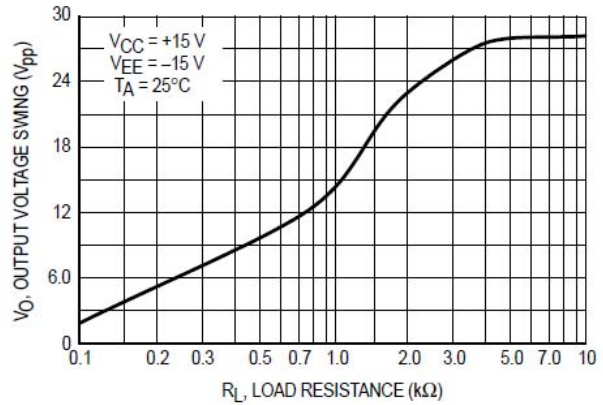


Figure 5. Output Voltage Swing versus Frequency

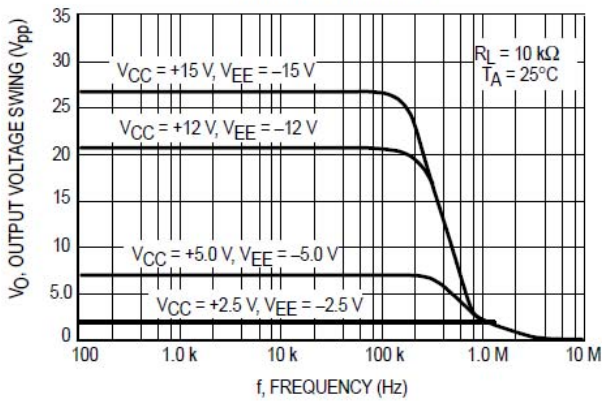


Figure 6. Large Signal Voltage Gain versus Temperature

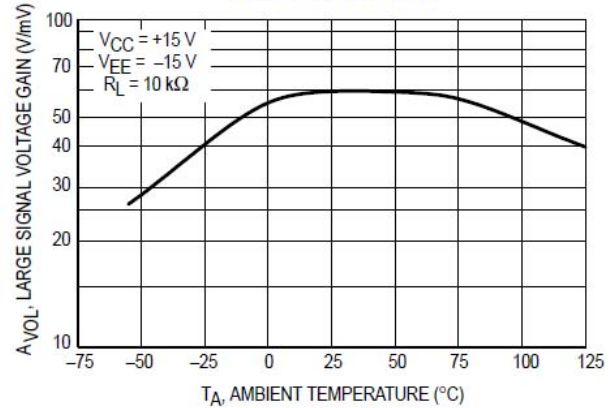


Figure 7. Open Loop Voltage Gain and Phase versus Frequency

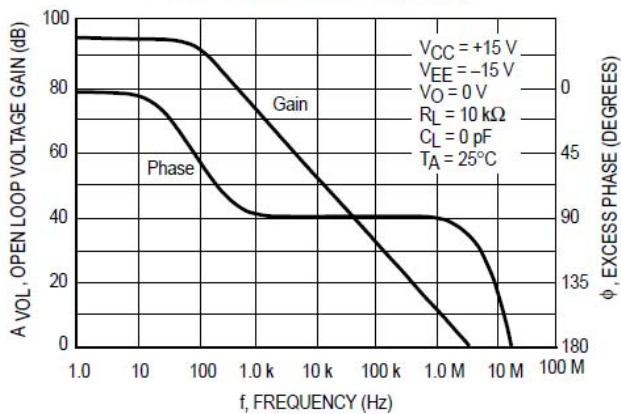
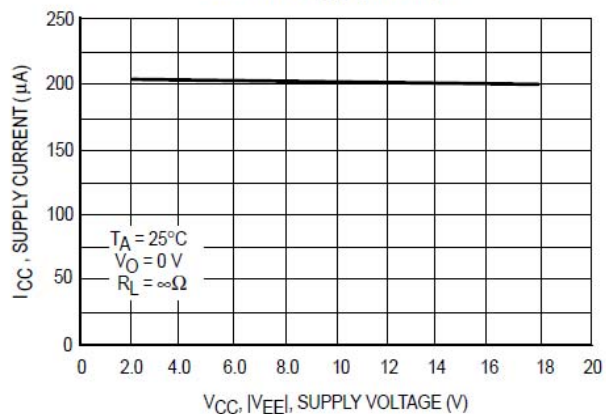


Figure 8. Supply Current per Amplifier versus Supply Voltage



Low power J - FET input operational amplifier

Figure 9. Supply Current per Amplifier versus Temperature

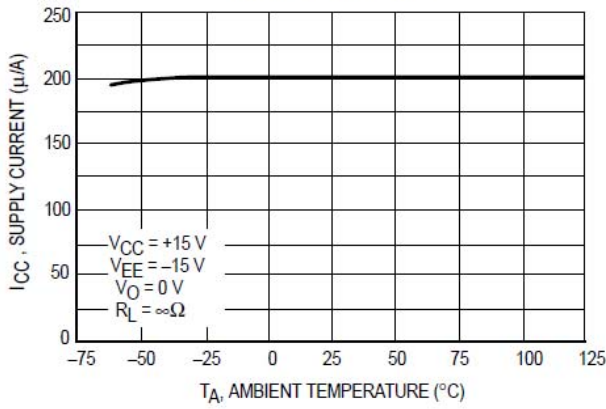


Figure 10. Total Power Dissipation versus Temperature

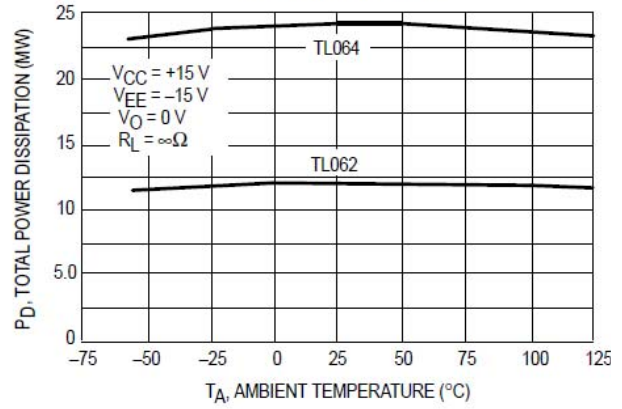


Figure 11. Common Mode Rejection versus Temperature

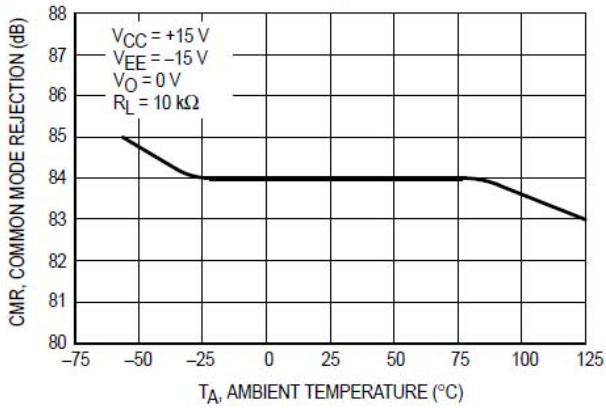


Figure 12. Common Mode Rejection versus Frequency

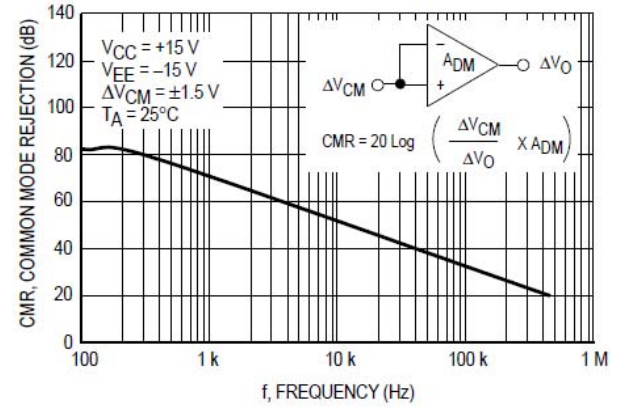


Figure 13. Power Supply Rejection versus Frequency

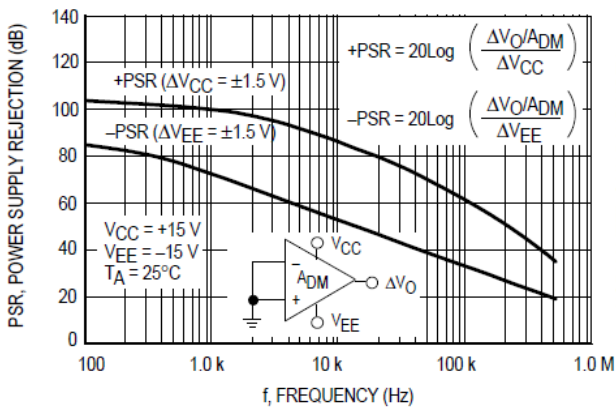
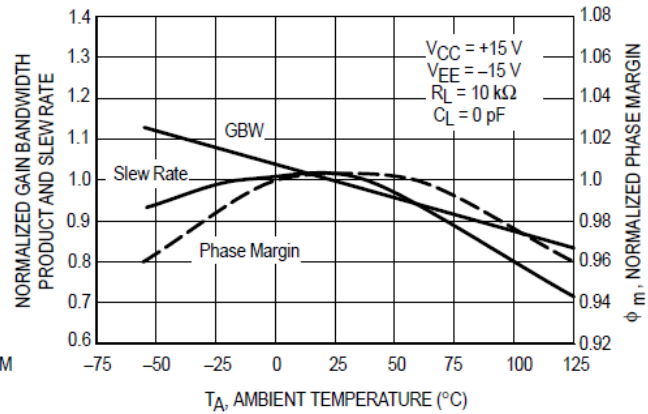


Figure 14. Normalized Gain Bandwidth Product, Slew Rate and Phase Margin versus Temperature



Low power J - FET input operational amplifier

Figure 15. Input Bias Current versus Temperature

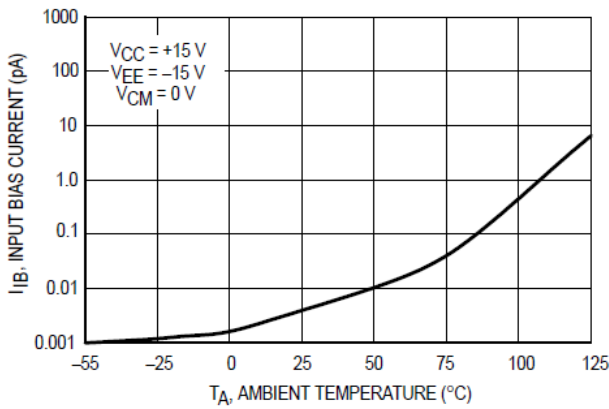


Figure 16. Input Noise Voltage versus Frequency

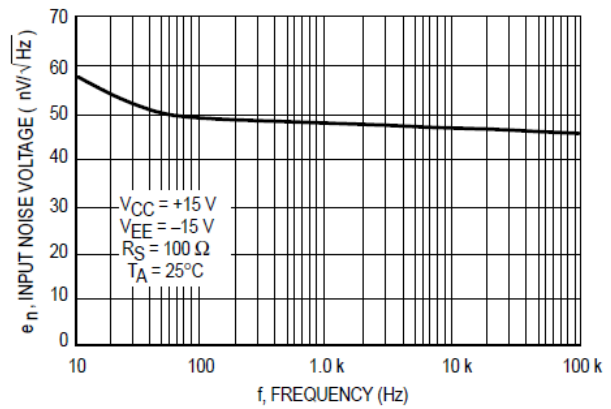


Figure 17. Small Signal Response

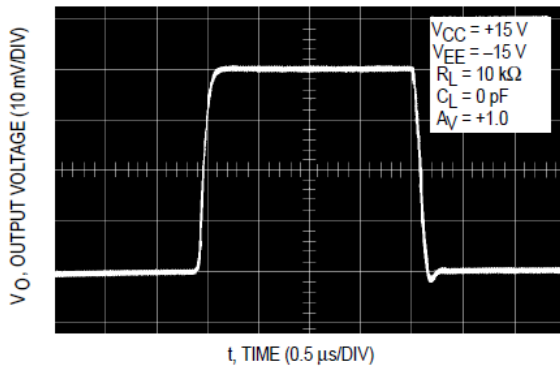


Figure 18. Large Signal Response

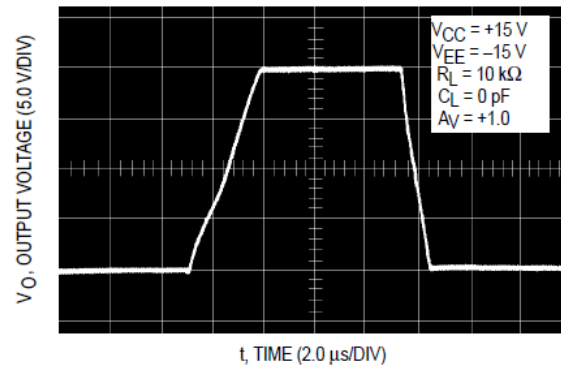


Figure 19. AC Amplifier

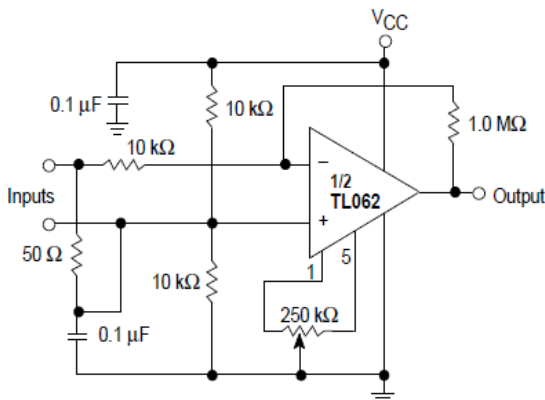


Figure 20. High-Q Notch Filter

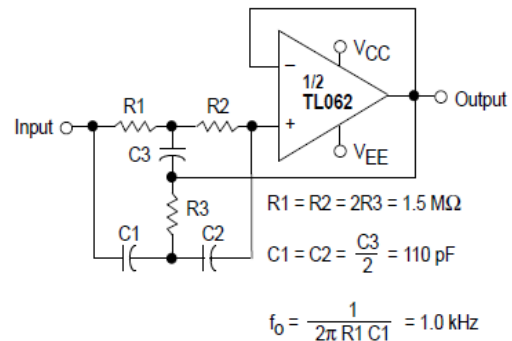


Figure 21. Instrumentation Amplifier

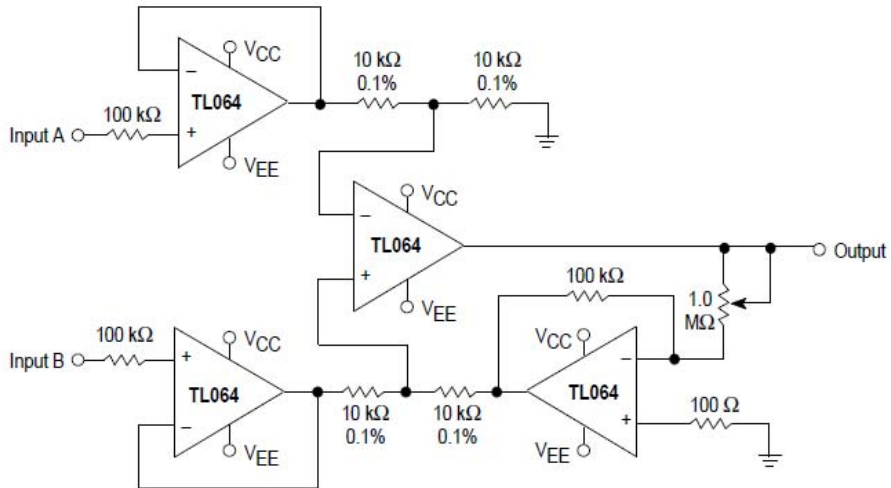


Figure 22. 0.5 Hz Square-Wave Oscillator

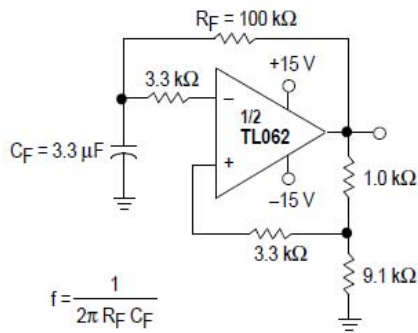
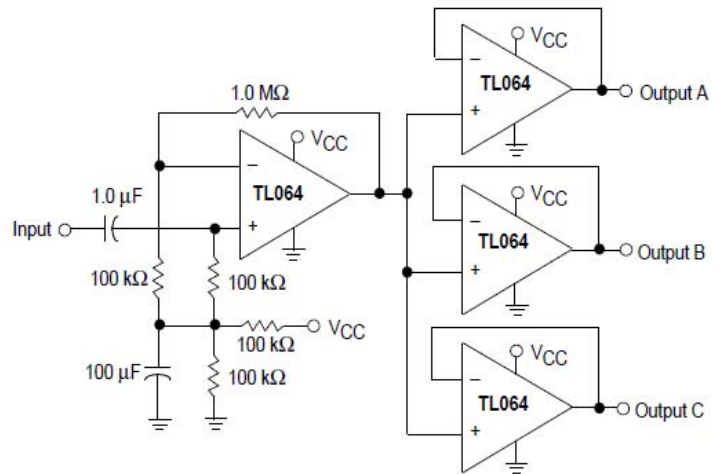
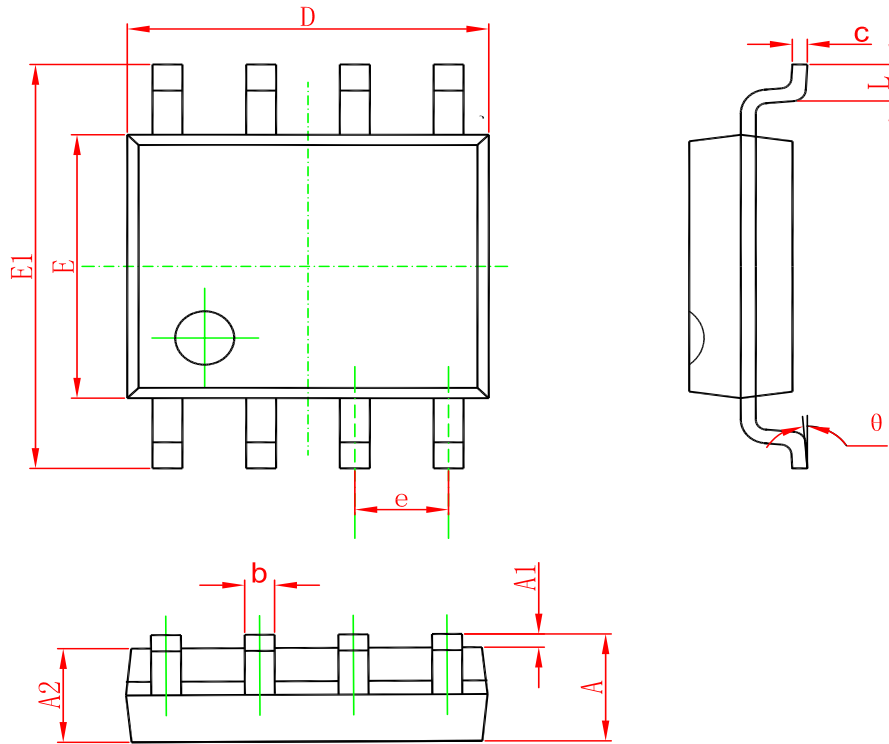


Figure 23. Audio Distribution Amplifier



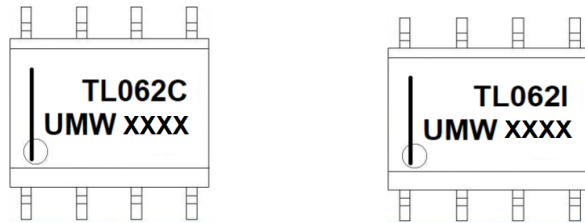
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW TL062IDR	SOP-8	2500	Tape and reel
UMW TL062CDR	SOP-8	2500	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

[>>UMW\(友台半导体\)](#)