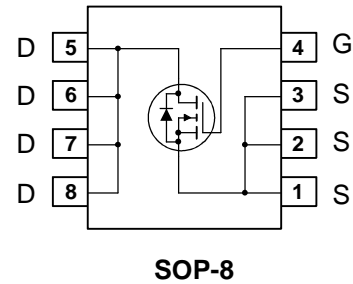


### General Description

This N-Channel Logic Level MOSFET is produced using the advanced Power Trench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.



### Features

- $V_{DS} (V) = 30V$
- $I_D = 12 A (V_{GS} = 10V)$
- $R_{DS(ON)} < 9.5m\Omega (V_{GS}=10V)$
- $R_{DS(ON)} < 13 m\Omega (V_{GS}=4.5V)$
- Ultra-low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability

### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	12.5	A
		50	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2.5	W
		1.2	
		1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

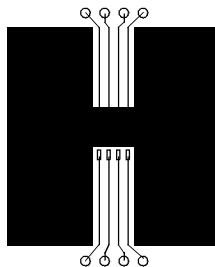
$R_{\theta JA}$	Thermal Resistance, Junction-to-Case (Note 1a)	50	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	

### Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

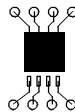
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units	
<b>Off Characteristics</b>							
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		25		mV/ $^\circ\text{C}$	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$	
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	$\mu\text{A}$	
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA	
<b>On Characteristics (Note 2)</b>							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2	3	V	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-4.9		mV/ $^\circ\text{C}$	
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 12.5\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 10.5\text{ A}$		7.8 9.9	9.5 13	m $\Omega$	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	25			A	
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 12.5\text{ A}$		64		S	
<b>Dynamic Characteristics</b>							
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1620		pF	
$C_{oss}$	Output Capacitance				380		pF
$C_{rss}$	Reverse Transfer Capacitance				160		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.3		$\Omega$	
<b>Switching Characteristics (Note 2)</b>							
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		10	19	ns	
$t_r$	Turn–On Rise Time			5	10	ns	
$t_{d(off)}$	Turn–Off Delay Time			27	43	ns	
$t_f$	Turn–Off Fall Time			15	27	ns	
$Q_g$	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 12.5\text{ A},$ $V_{GS} = 5\text{ V}$		16	23	nC	
$Q_{gs}$	Gate–Source Charge			5		nC	
$Q_{gd}$	Gate–Drain Charge			5.8		nC	
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				2.1	A	
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.73	1.2	V	
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 12.5\text{ A}, d_F/d_t = 100\text{ A}/\mu\text{s}$		28		ns	
$Q_{rr}$	Diode Reverse Recovery Charge			18		nC	

**Notes:**

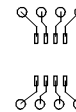
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $105^\circ\text{C}/\text{W}$  when mounted on a  $.04\text{ in}^2$  pad of 2 oz copper



c)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty Cycle < 2.0%

Typical Characteristics

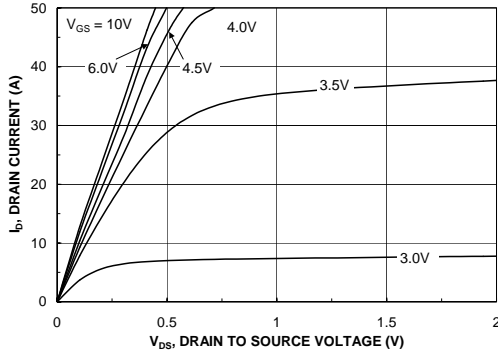


Figure 1. On-Region Characteristics.

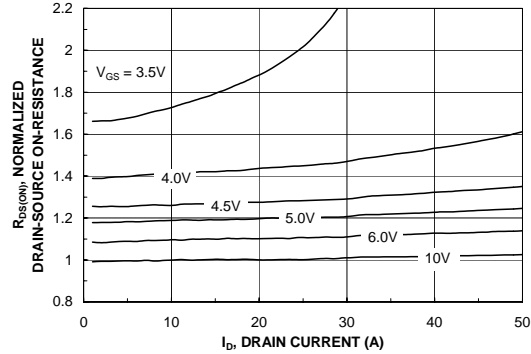


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

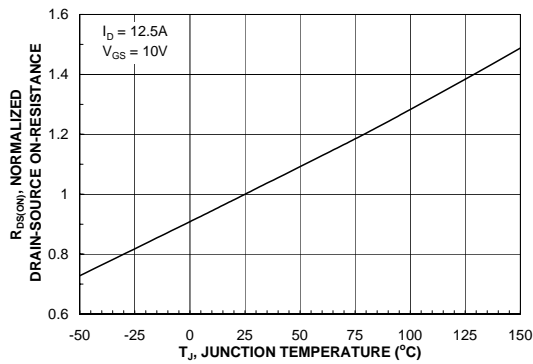


Figure 3. On-Resistance Variation with Temperature.

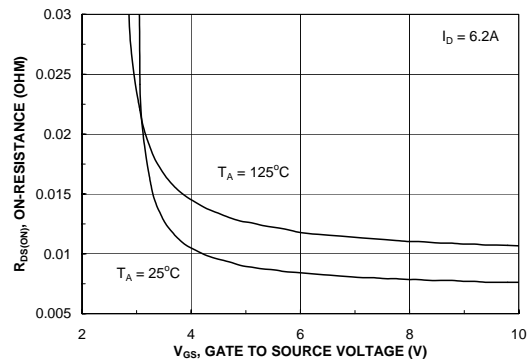


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

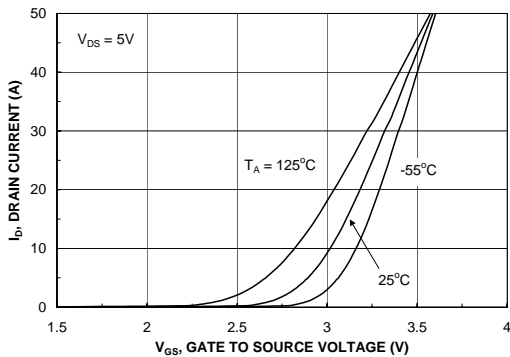


Figure 5. Transfer Characteristics.

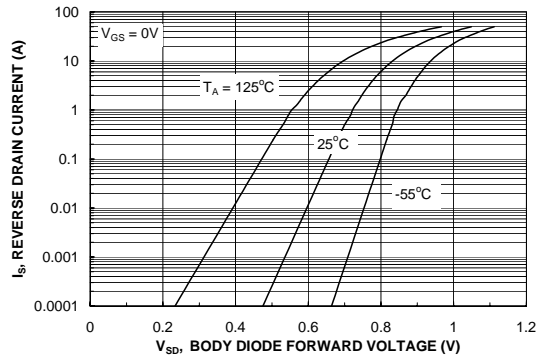


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

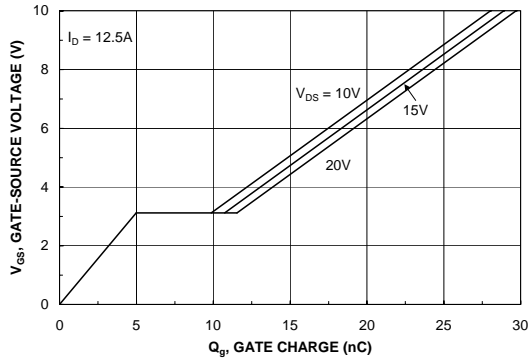


Figure 7. Gate Charge Characteristics.

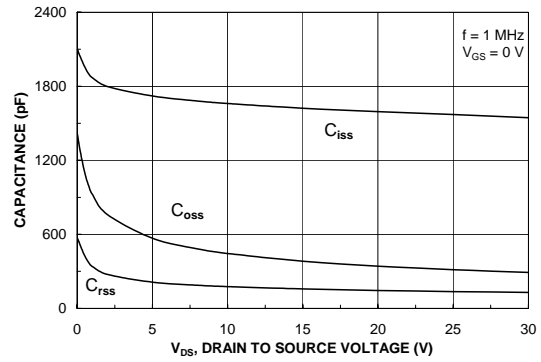


Figure 8. Capacitance Characteristics.

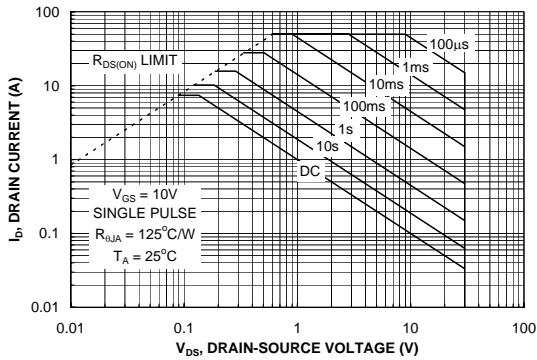


Figure 9. Maximum Safe Operating Area.

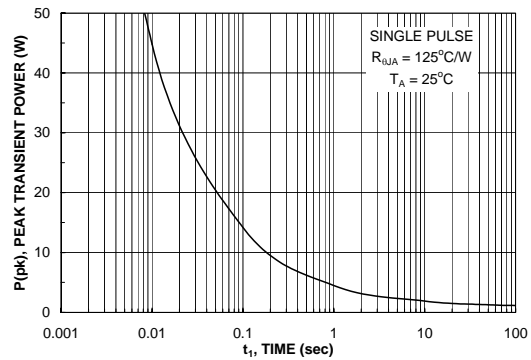


Figure 10. Single Pulse Maximum Power Dissipation.

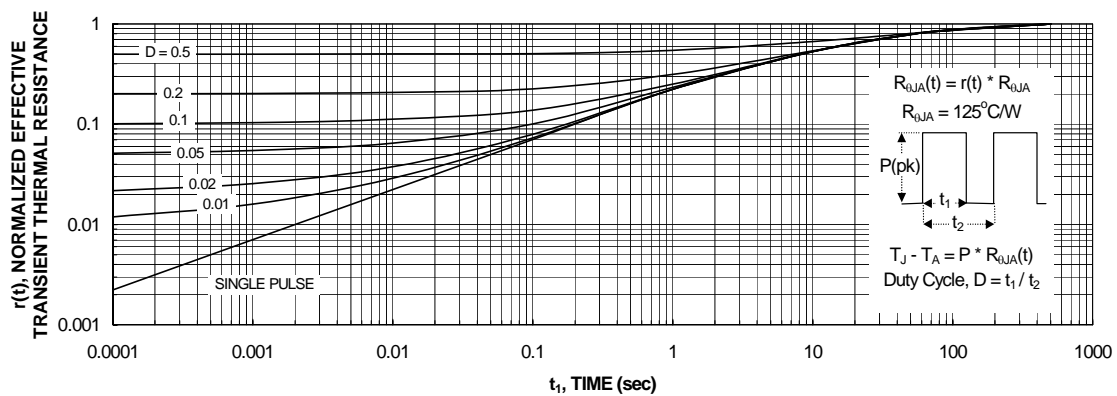
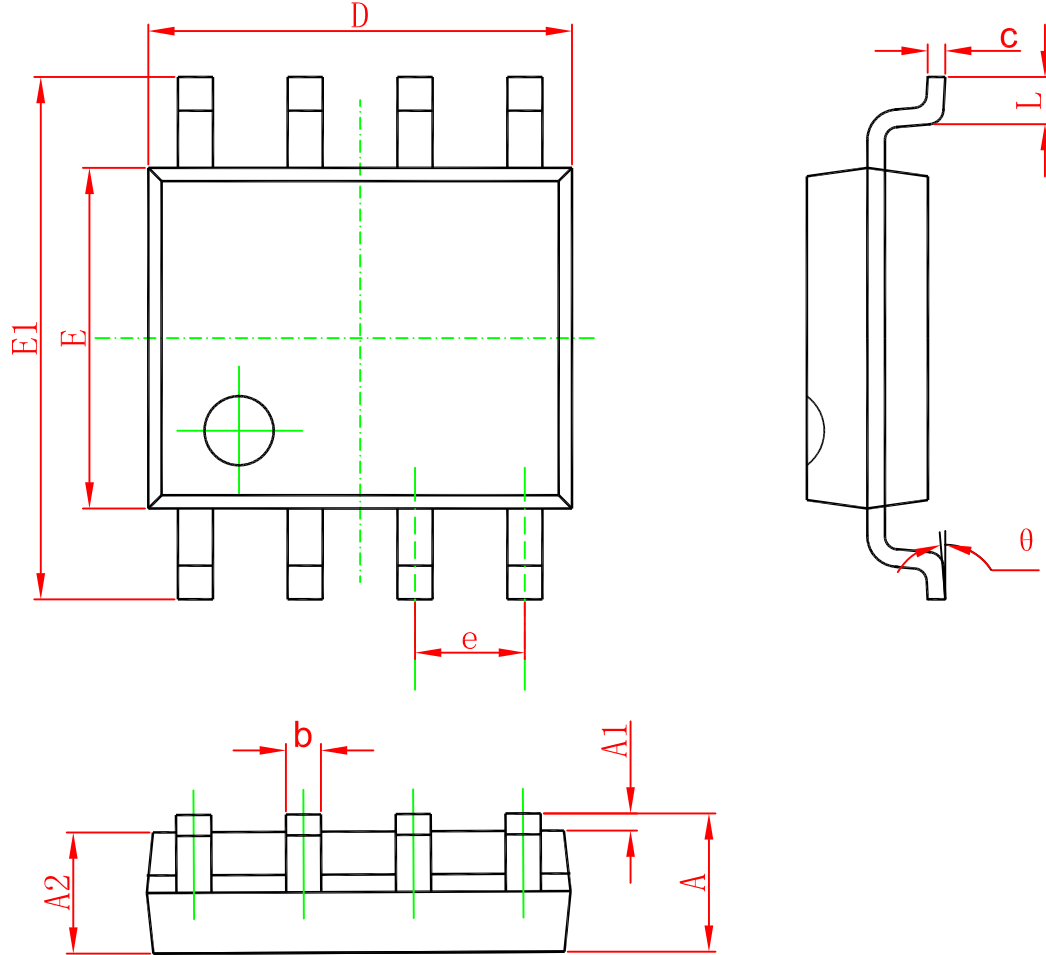


Figure 11. Transient Thermal Response Curve.

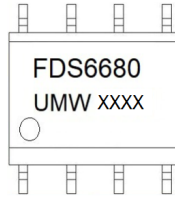
Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

Package Mechanical Data SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

**Marking**



**Ordering information**

Order code	Package	Baseqty	Deliverymode
UMW FDS6680A	SOP-8	3000	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

[>>UMW\(友台半导体\)](#)