Features

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up to 200 mA

Applications

- Fingerprint Biometrics
- Iris Biometrics
- RFID Reader

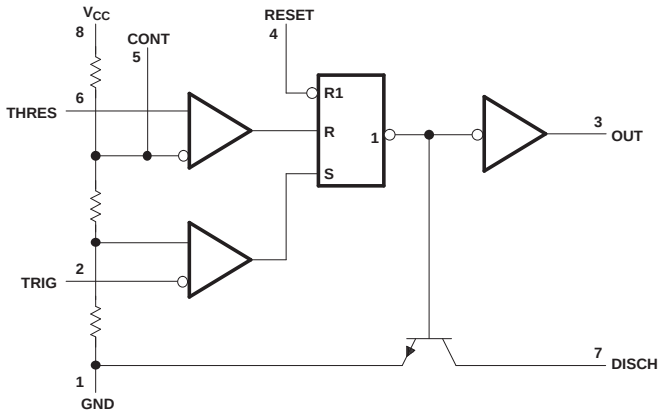
Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

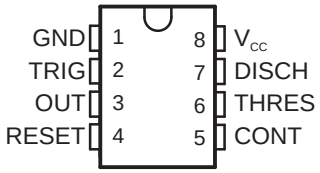
The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

Simplified Schematic

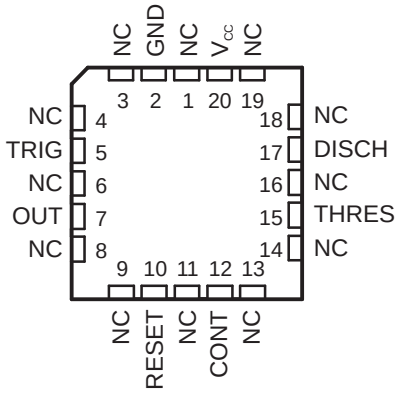


Pin Configuration and Functions

NA555...D OR P PACKAGE
NE555...D, P, PS, OR PW PACKAGE
SA555...D OR P PACKAGE
SE555...D, JG, OR P PACKAGE
(TOP VIEW)



SE555...FK PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	D, P, PS, PW, JG	FK		
	NO.			
CONT	5	12	I/O	Controls comparator thresholds, Outputs 2/3 VCC, allows bypass capacitor connection
DISCH	7	17	O	Open collector output to discharge timing capacitor
GND	1	2	–	Ground
NC		1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	–	No internal connection
OUT	3	7	O	High current timer output signal
RESET	4	10	I	Active low reset input forces output and discharge low.
THRES	6	15	I	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	5	I	Start of timing input. TRIG < ½ CONT sets output high and discharge open
V_{CC}	8	20	–	Input supply voltage, 4.5 V to 16 V. (SA555 maximum is 18 V)

Specifications

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)			18	V
V_I	Input voltage	CONT, RESET, THRES, TRIG		V_{CC}	V
I_O	Output current			±225	mA
θ_{JA}	Package thermal impedance(3)(4)	D package		97	°C/W
		P package		85	
		PS package		95	
		PW package		149	
θ_{JC}	Package thermal impedance(5)(6)	FK package		5.61	°C/W
		JG package		14.5	
T_J	Operating virtual junction temperature			150	°C
	Case temperature for 60 s	FK package		260	°C
	Lead temperature 1,6 mm (1/16 in) from case for 60 s	JG package		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C) / \theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with MIL-STD-883.

Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	NA555, NE555, SA555	4.5	16	V
		SE555	4.5	18	
V_I	Input voltage	CONT, RESET, THRES, and TRIG		V_{CC}	V
I_O	Output current			±200	mA
T_A	Operating free-air temperature	NA555	–40	105	°C
		NE555	0	70	
		SA555	–40	85	
		SE555	–55	125	

Electrical Characteristics

V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	V_{CC} = 15 V		9.4	10	10.6	8.8	10	11.2	V
	V_{CC} = 5 V		2.7	3.3	4	2.4	3.3	4.2	
THRES current(1)				30	250		30	250	nA
TRIG voltage level	V_{CC} = 15 V		4.8	5	5.2	4.5	5	5.6	V
		T_A = –55°C to 125°C	3		6				
	V_{CC} = 5 V		1.45	1.67	1.9	1.1	1.67	2.2	
		T_A = –55°C to 125°C			1.9				
TRIG current	TRIG at 0 V			0.5	0.9		0.5	2	µA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	T_A = –55°C to 125°C				1.1				
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0 V			–0.4	–1		–0.4	–1.5	
DISCH switch off-state current				20	100		20	100	nA
DISCH switch on-state voltage	V_{CC} = 5 V, I_O = 8 mA						0.15	0.4	V
CONT voltage (open circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
		T_A = –55°C to 125°C	9.6		10.4				
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
		T_A = –55°C to 125°C	2.9		3.8				
Low-level output voltage	V_{CC} = 15 V, I_{OL} = 10 mA			0.1	0.15		0.1	0.25	V
		T_A = –55°C to 125°C			0.2				
	V_{CC} = 15 V, I_{OL} = 50 mA			0.4	0.5		0.4	0.75	
		T_A = –55°C to 125°C			1				
	V_{CC} = 15 V, I_{OL} = 100 mA			2	2.2		2	2.5	
		T_A = –55°C to 125°C			2.7				
	V_{CC} = 15 V, I_{OL} = 200 mA			2.5			2.5		
	V_{CC} = 5 V, I_{OL} = 3.5 mA	T_A = –55°C to 125°C			0.35				
	V_{CC} = 5 V, I_{OL} = 5 mA			0.1	0.2		0.1	0.35	
		T_A = –55°C to 125°C			0.8				
	V_{CC} = 5 V, I_{OL} = 8 mA			0.15	0.25		0.15	0.4	
High-level output voltage	V_{CC} = 15 V, I_{OH} = –100 mA		13	13.3		12.75	13.3		V
		T_A = –55°C to 125°C	12						
	V_{CC} = 15 V, I_{OH} = –200 mA			12.5			12.5		
	V_{CC} = 5 V, I_{OH} = –100 mA		3	3.3		2.75	3.3		
		T_A = –55°C to 125°C	2						
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	10		9	13	
		V_{CC} = 5 V		2	4		2	5	

(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when V_{CC} = 5 V, the maximum value is $R = R_A + R_B \neq 3.4$ MΩ, and for V_{CC} = 15 V, the maximum value is 10 MΩ.

Operating Characteristics

V_{CC} = 5 V to 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval(2)	Each timer, monostable(3)	T_A = 25°C		0.5	1.5(4)		1	3	%
	Each timer, astable(5)			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable(3)	T_A = MIN to MAX		30	100(4)		50		ppm/°C
	Each timer, astable(5)			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable(3)	T_A = 25°C		0.05	0.2(4)		0.1	0.5	%/V
	Each timer, astable(5)			0.15			0.3		
Output-pulse rise time		C_L = 15 pF, T_A = 25°C		100	200(4)		100	300	ns
Output-pulse fall time		C_L = 15 pF, T_A = 25°C		100	200(4)		100	300	ns

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.
(3) Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values: R_A = 2 kΩ to 100 kΩ, C = 0.1 µF.
(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(5) Values specified are for a device in an astable circuit similar to Figure 12, with the following component values: R_A = 1 kΩ to 100 kΩ, C = 0.1 µF.

Typical Characteristics

Data for temperatures below –40°C and above 105°C are applicable for SE555 circuits only.

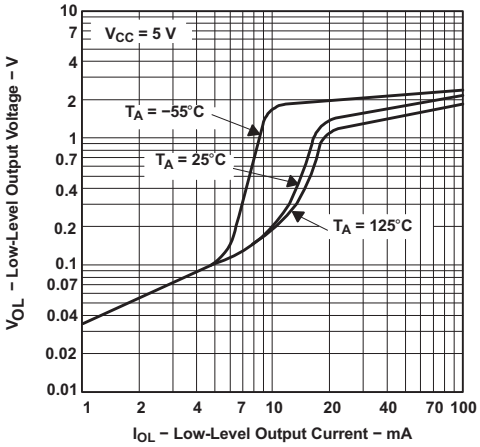


Figure 1. Low-Level Output Voltage vs Low-Level Output Current

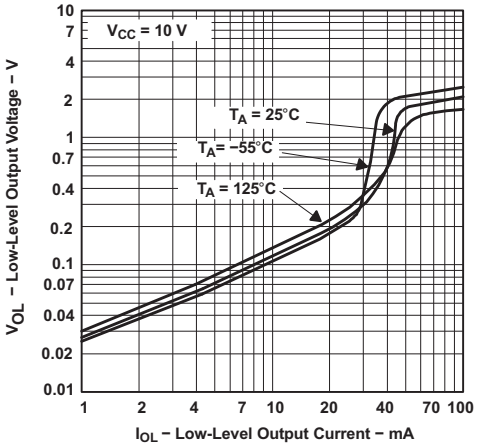


Figure 2. Low-Level Output Voltage vs Low-Level Output Current

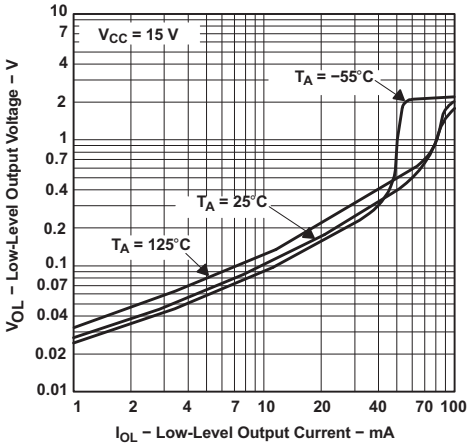


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

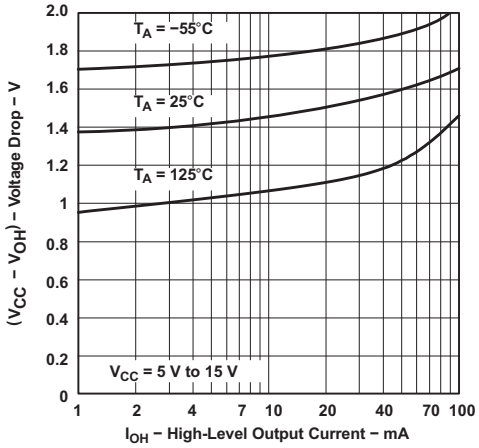


Figure 4. Drop Between Supply Voltage and Output vs High-Level Output Current

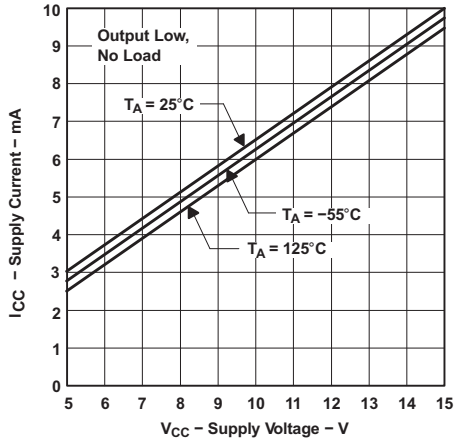


Figure 5. Supply Current vs Supply Voltage

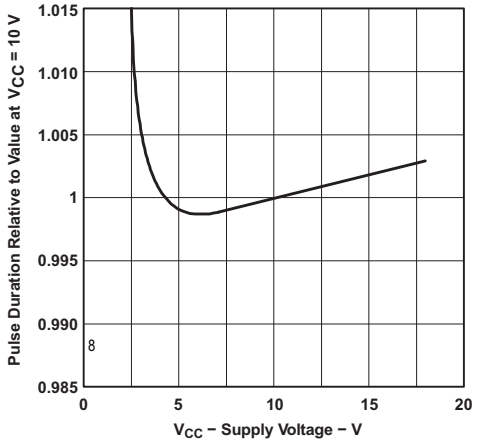


Figure 6. Normalized Output Pulse Duration (Monostable Operation) vs Supply Voltage

Typical Characteristics (continued)

Data for temperatures below –40°C and above 105°C are applicable for SE555 circuits only.

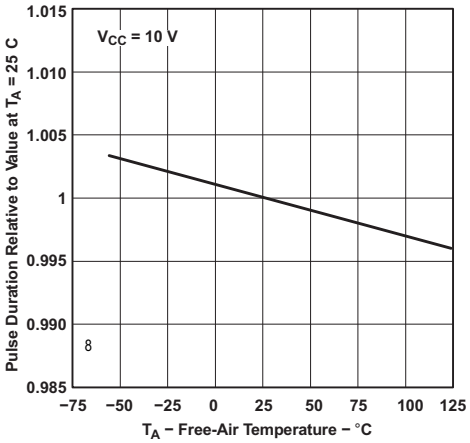


Figure 7. Normalized Output Pulse Duration (Monostable Operation) vs Free-Air Temperature

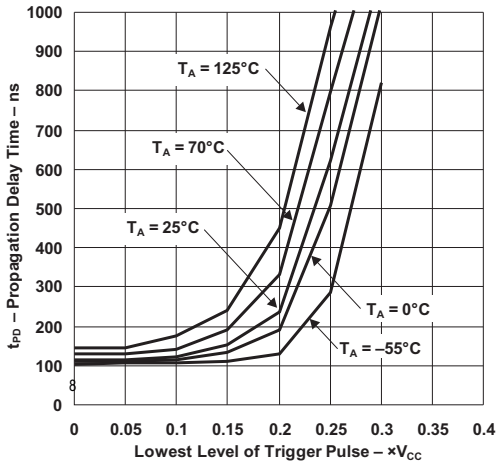


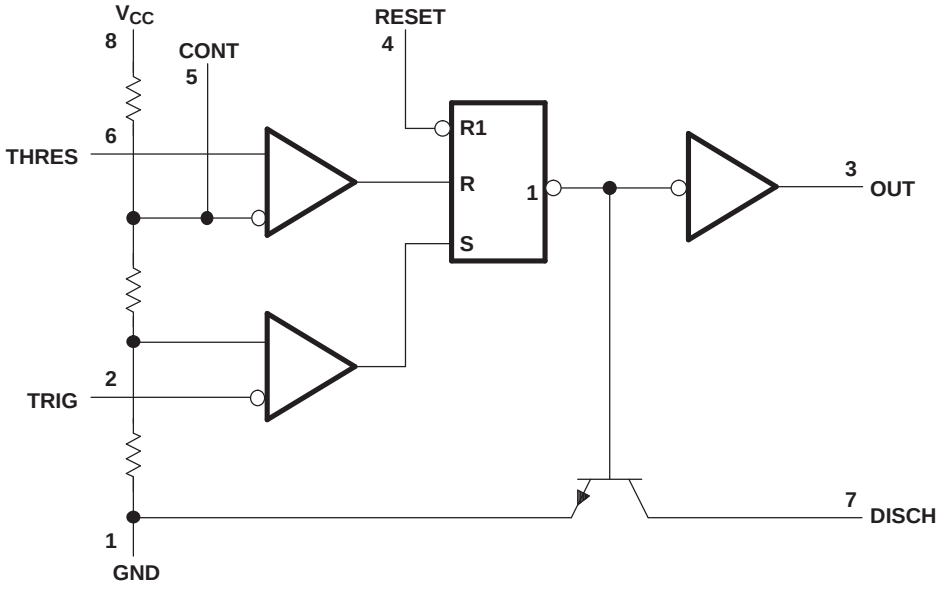
Figure 8. Propagation Delay Time vs Lowest Voltage Level of Trigger Pulse

Detailed Description

Overview

The xx555 timer is a popular and easy to use for general purpose timing applications from 10 µs to hours or from < 1mHz to 100 kHz. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the a-stable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor. Maximum output sink and discharge sink current is greater for higher VCC and less for lower VCC.

Functional Block Diagram



A. Pin numbers shown are for the D, JG, P, PS, and PW packages.

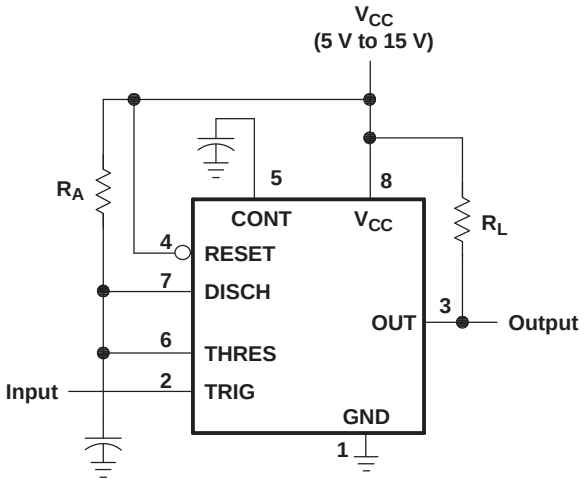
B. RESET can override TRIG, which can override THRES.

Feature Description

Mono-stable Operation

For mono-stable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.

Feature Description (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10 µs before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 µs, which limits the minimum monostable pulse width to 10 µs. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_AC$. Figure 11 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC}.

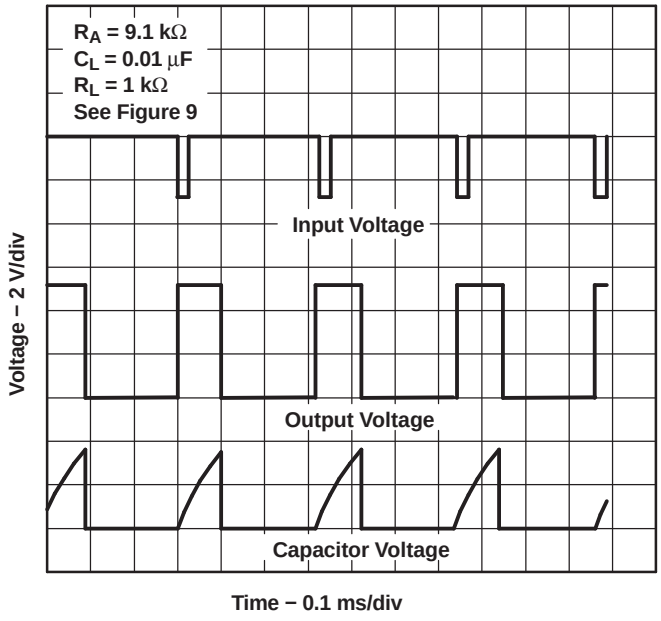


Figure 10. Typical Monostable Waveforms

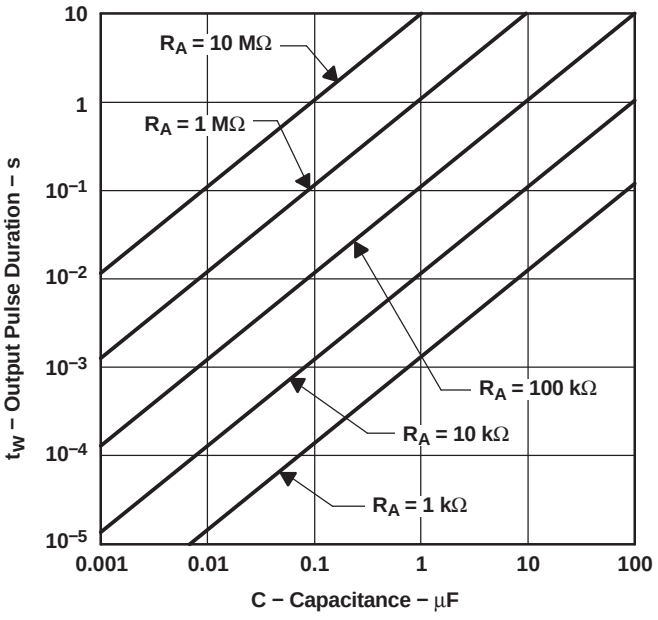


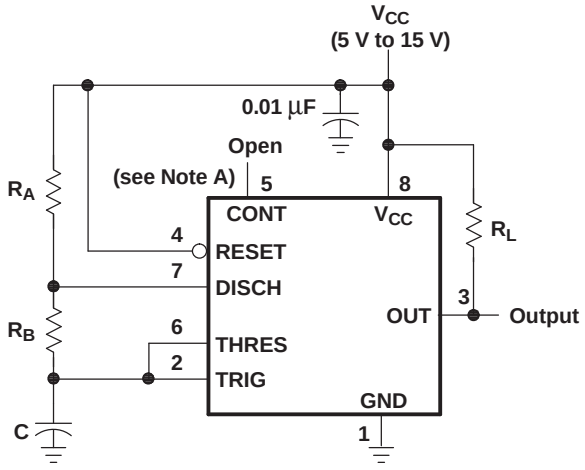
Figure 11. Output Pulse Duration vs Capacitance

Feature Description (continued)

A-stable Operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the mono-stable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

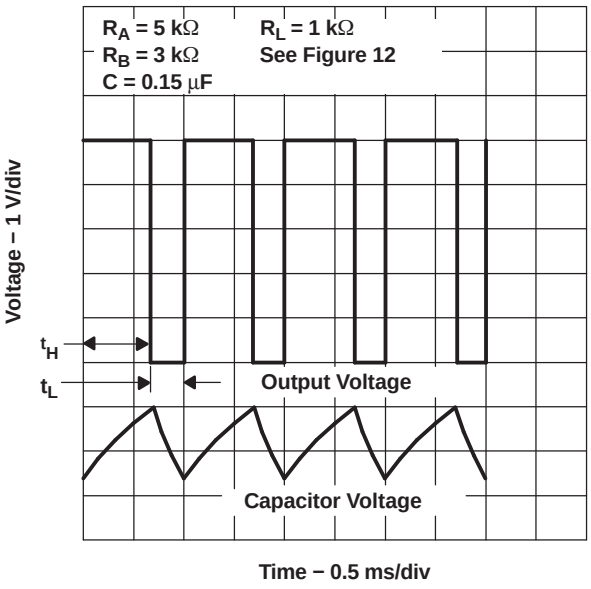


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C \quad (1)$$

$$t_L = 0.693(R_B)C \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B}{R_A + R_B} \quad (7)$$

Feature Description (continued)

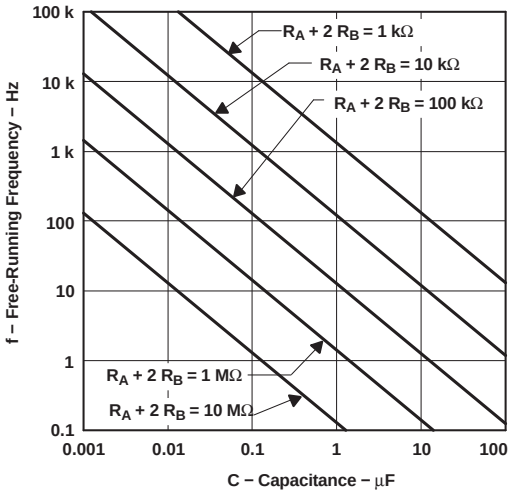


Figure 14. Free-Running Frequency

Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 15 shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.

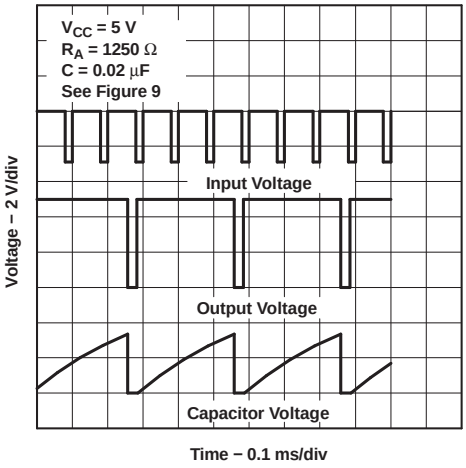


Figure 15. Divide-by-Three Circuit Waveforms

Device Functional Modes

Table 1. Function Table

RESET	TRIGGER VOLTAGE(1)	THRESHOLD VOLTAGE(1)	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{CC}	Irrelevant	High	Off
High	>1/3 V_{CC}	>2/3 V_{CC}	Low	On
High	>1/3 V_{CC}	<2/3 V_{CC}	As previously established	

(1) Voltage levels shown are nominal.

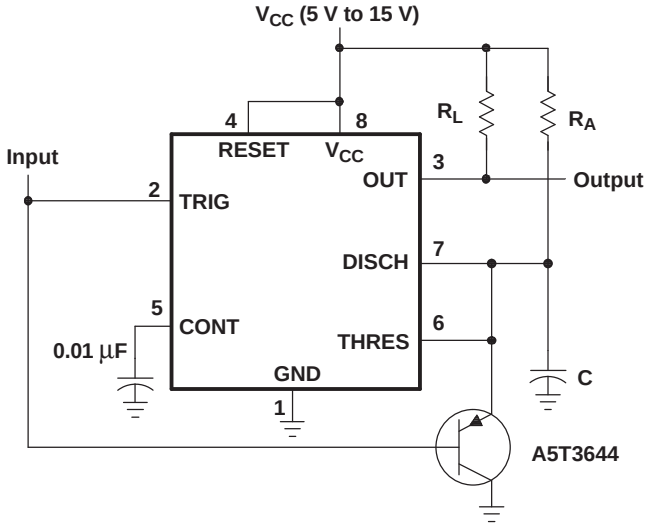
Application Information

The xx555 timer devices use resistor and capacitor charging delay to provide a programmable time delay or operating frequency. This section presents a simplified discussion of the design process.

Typical Applications

Missing-Pulse Detector

The circuit shown in Figure 16 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 17.



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 16. Circuit for Missing-Pulse Detector

Design Requirements

Input fault (missing pulses) must be input high. Input stuck low will not be detected because timing capacitor "C" will remain discharged.

Detailed Design Procedure

Choose R_A and C so that $R_A \times C >$ [maximum normal input high time]. R_L improves V_{OH}, but it is not required for TTL compatibility.

Typical Applications (continued)

Application Curves

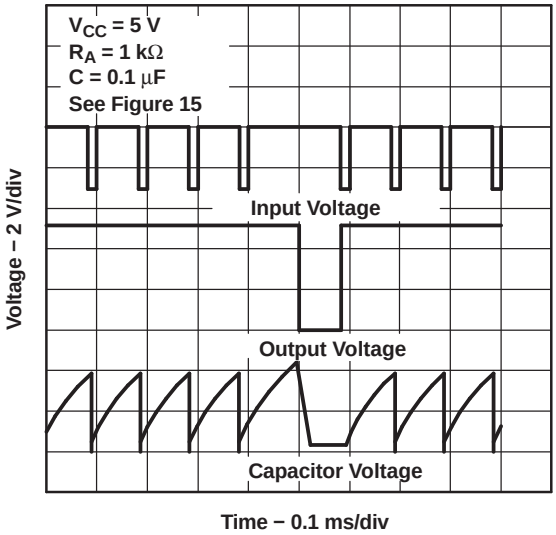
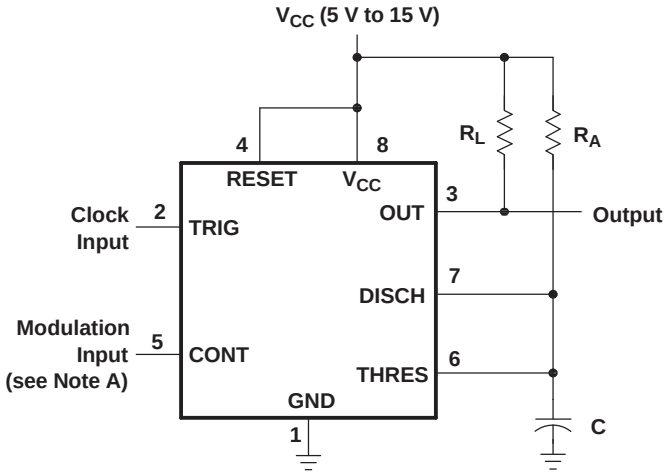


Figure 17. Completed Timing Waveforms for Missing-Pulse Detector

Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

Typical Applications (continued)

Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 VCC. Modulation input can vary from ground to VCC. The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is based RC on an negative exponential curve.

Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH}, but it is not required for TTL compatibility.

Application Curves

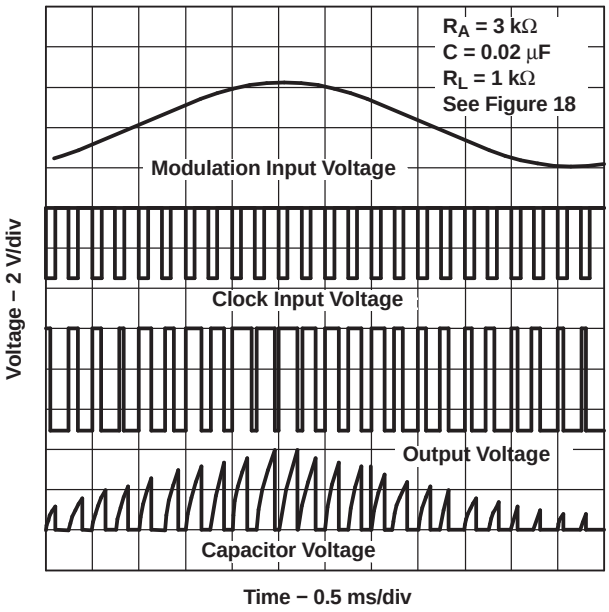
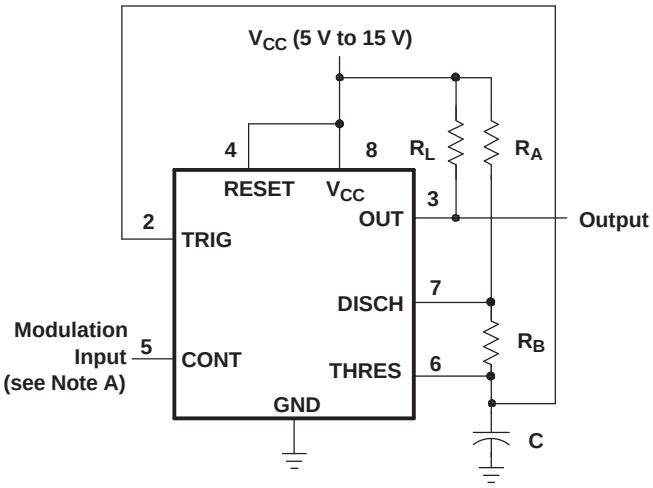


Figure 19. Pulse-Width-Modulation Waveforms

Pulse-Position Modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

Typical Applications (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

Design Requirements

Both DC and AC coupled modulation input will change the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle will vary with the modulation voltage.

Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in A-stable Operation section. R_L improves V_{OH}, but it is not required for TTL compatibility.

Typical Applications (continued)

Application Curves

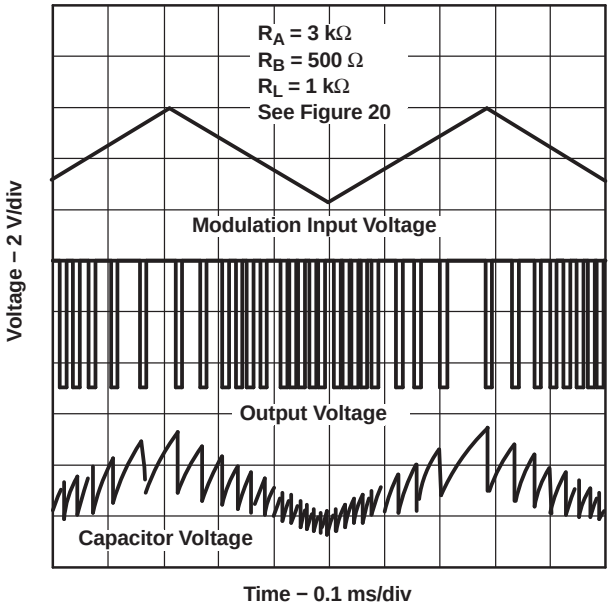
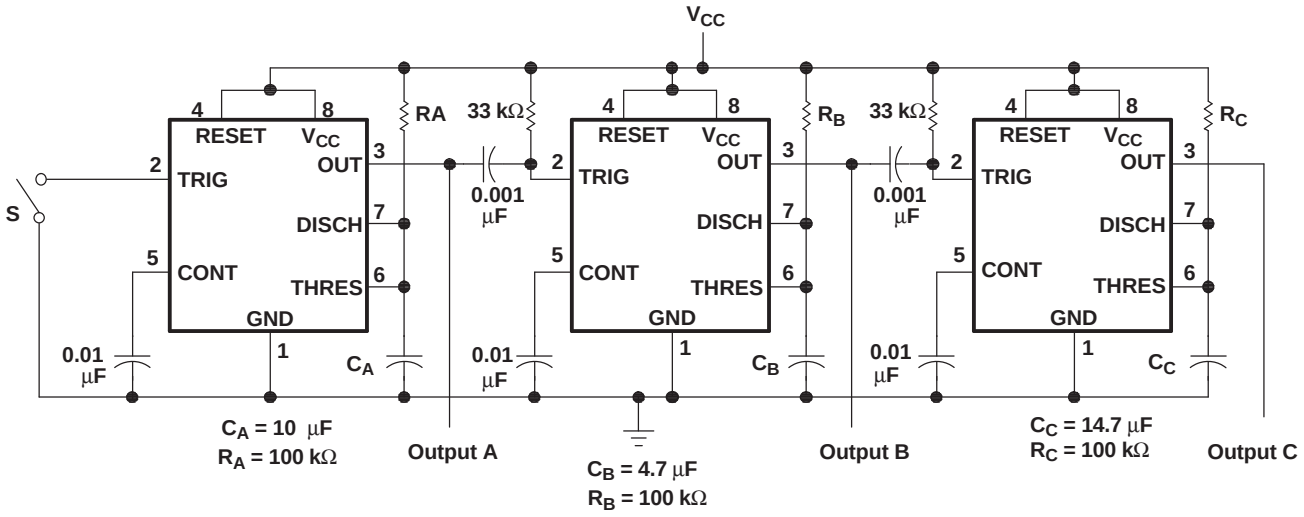


Figure 21. Pulse-Position-Modulation Waveforms

Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: S closes momentarily at t = 0.

Figure 22. Sequential Timer Circuit

Typical Applications (continued)

Design Requirements

The sequential timer application chains together multiple mono-stable timers. The joining components are the 33-kΩ resistors and 0.001-µF capacitors. The output high to low edge passes a 10-µs start pulse to the next monostable.

Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula. $t_w = 1.1 \times R \times C$.

Application Curves

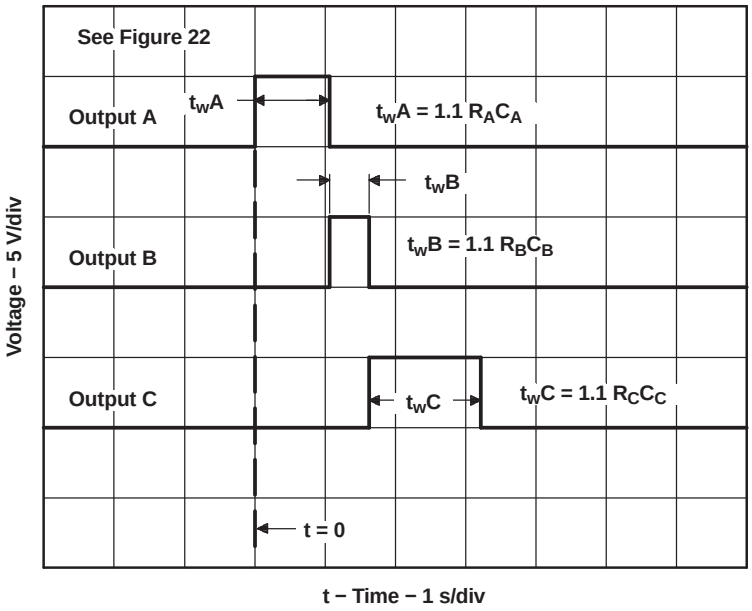


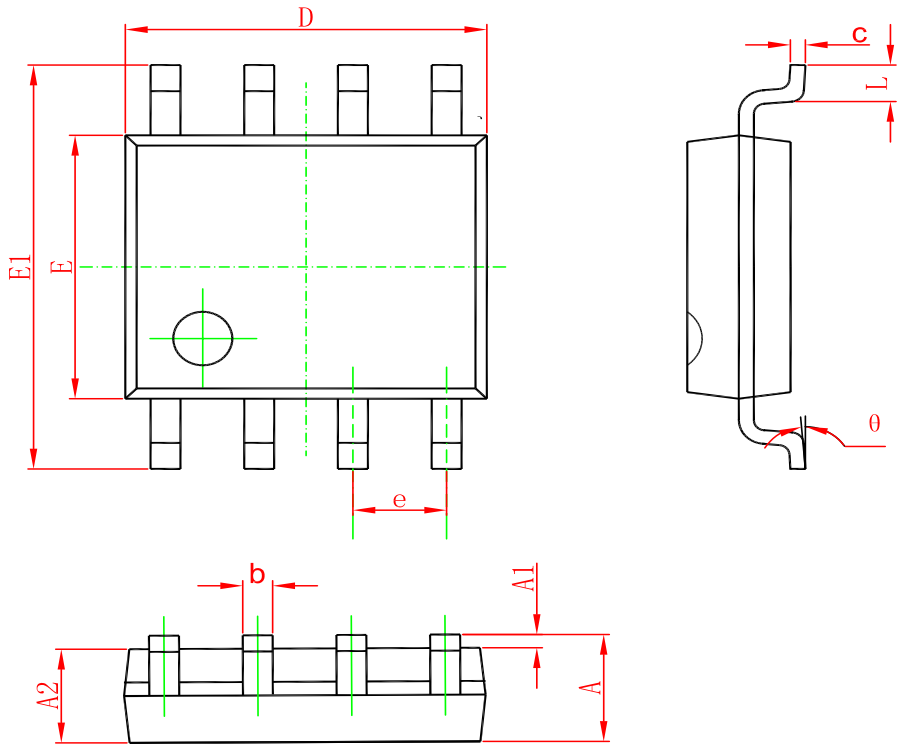
Figure 23. Sequential Timer Waveforms

Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 16 V. (18 V for SE555). A bypass capacitor is highly recommended from VCC to ground pin; ceramic 0.1 µF capacitor is sufficient.

PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Ordering information

Order code	Package	Baseqty	Deliverymode
UMW NA555DR	SOP-8	2500	Tape and reel
UMW NE555DR	SOP-8	2500	Tape and reel
UMW SA555DR	SOP-8	2500	Tape and reel
UMW SE555DR	SOP-8	2500	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)