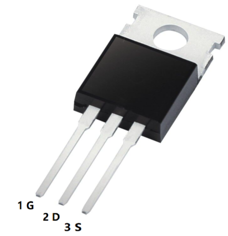
100 V N-Channel MOSFET

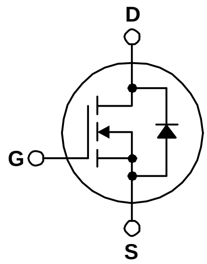
General Description

This N-Channel MV MOSFET is produced using process that has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.



Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



Features

- $V_{DS\,(V)}$ =100V
- I_D = 76 A (V_{GS} = 10V)
- $R_{DS(ON)}$ < 8.5mΩ (V_{GS}=10V)

MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted.

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25°C	(Note 3)	76	A
	-Continuous	T_C = 100°C	(Note 3)	54	
	-Pulsed		(Note 1)	304	
E_{AS}	Single Pulse Avalanche Energy		(Note 2)	181	mJ
P_D	Power Dissipation	T_C = 25°C		107	W
	Power Dissipation	T_A = 25°C		2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +175	°C

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FDP8D5N10	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		57		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
		V_{DS} = 80 V, T_J= 150°C			500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 130 μA	2.0	3.0	4.0	V
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 76 A		7.4	8.5	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 76 A		68		S
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		1765	2475	pF
C_{oss}	Output Capacitance			1010	1415	pF
C_{rss}	Reverse Transfer Capacitance			16	25	pF
R_g	Gate Resistance		0.1	0.8	1.6	Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 76 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		12	22	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			18	28	ns
t_f	Fall Time			4	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 76 A		25	34	nC
Q_{gs}	Gate to Source Gate Charge			9		nC
Q_{gd}	Gate to Drain "Miller" Charge			5		nC
Q_{oss}	Output Charge	V_{DD} = 50 V, V_{GS} = 0 V		68		nC
I_S	Maximum Continuous Drain to Source Diode Forward Current				76	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current				304	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 76 A		1.0	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, V_{DD} = 50 V, I_F = 76 A, dI_F/dt = 100 A/μs		58	92	ns
Q_{rr}	Reverse Recovery Charge			53	85	nC
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, V_{DD} = 50 V, I_F = 76 A, dI_F/dt = 300 A/μs		51	81	ns
Q_{rr}	Reverse Recovery Charge			141	226	nC

Notes:

1. Pulsed Id please refer to Figure 11 & Figure 12 "Forward Bias Safe Operating Area" for more details.
2. E_{AS} of 181 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 11 A, V_{DD} = 100 V, V_{GS} = 10 V. 100% test at L = 0.3 mH, I_{AS} = 25 A.
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics T_J = 25 °C unless otherwise noted.

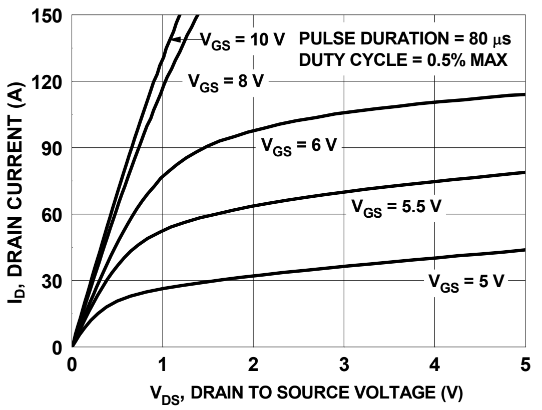


Figure 1. On Region Characteristics

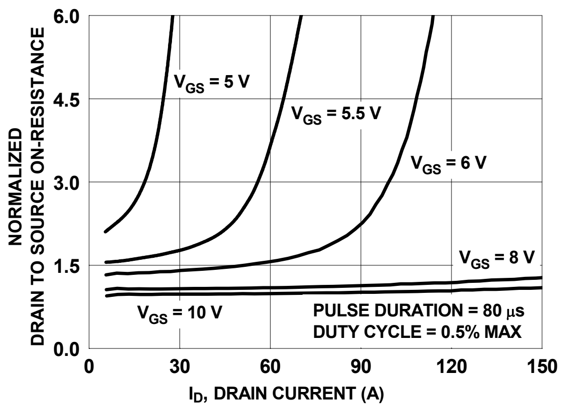


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

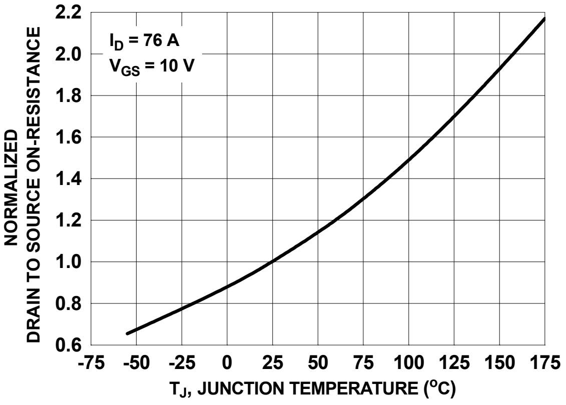


Figure 3. Normalized On Resistance vs. Junction Temperature

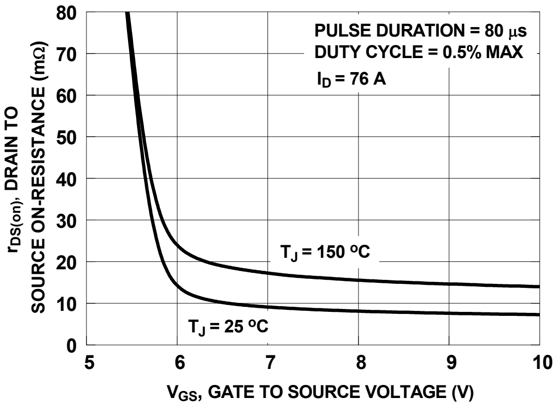


Figure 4. On-Resistance vs. Gate to Source Voltage

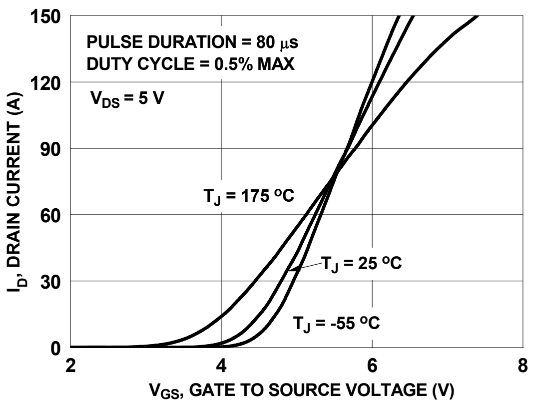


Figure 5. Transfer Characteristics

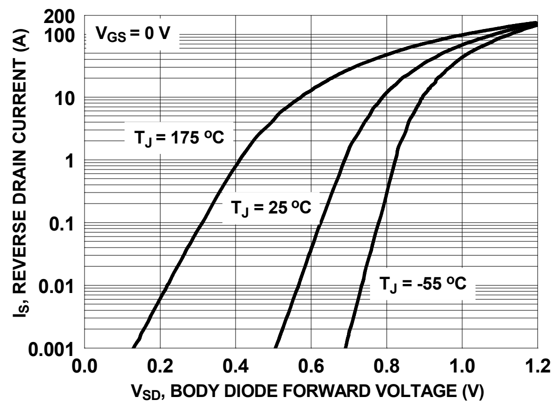


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted.

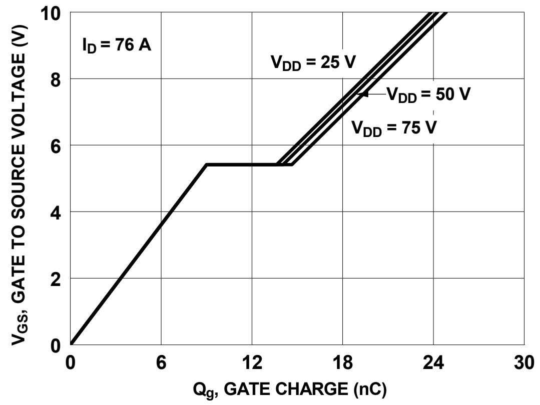


Figure 7. Gate Charge Characteristics

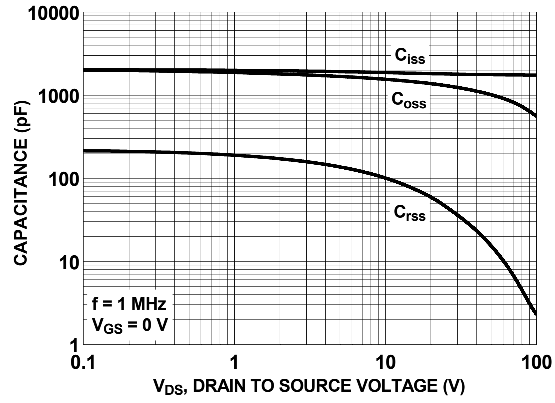


Figure 8. Capacitance vs. Drain to Source Voltage

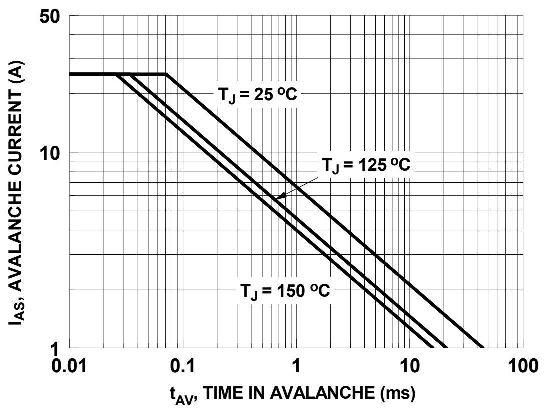


Figure 9. Unclamped Inductive Switching Capability

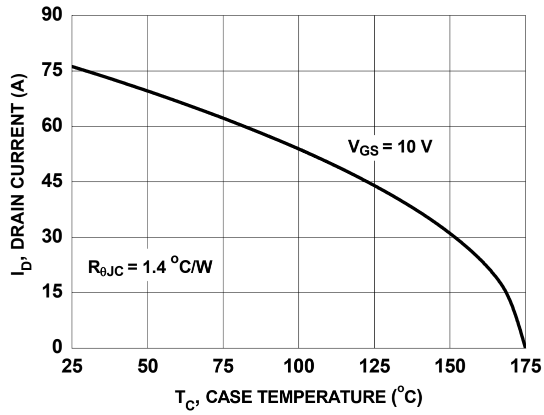


Figure 10. Maximum Continuous Drain Current vs. Case Temperature for FDP8D5N10C

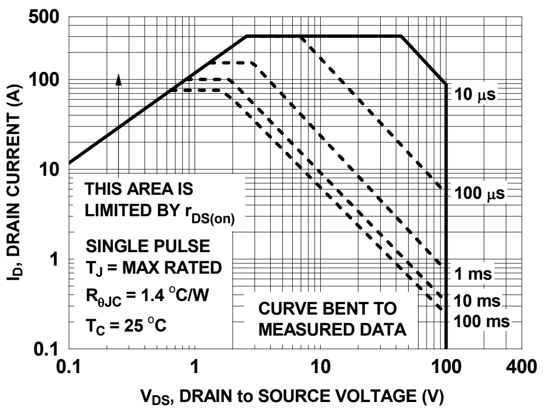


Figure 11. Forward Bias Safe Operating Area for FDP8D5N10C

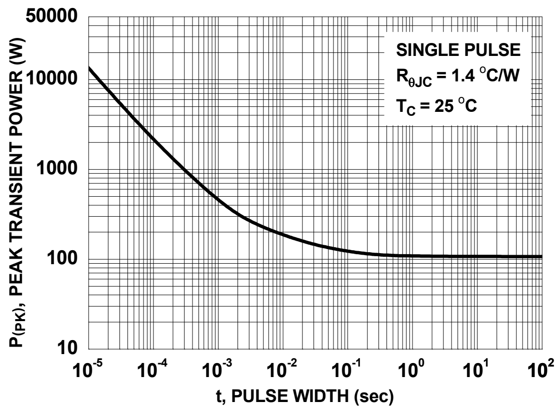


Figure 12. Single Pulse Maximum Power Dissipation for FDP8D5N10C

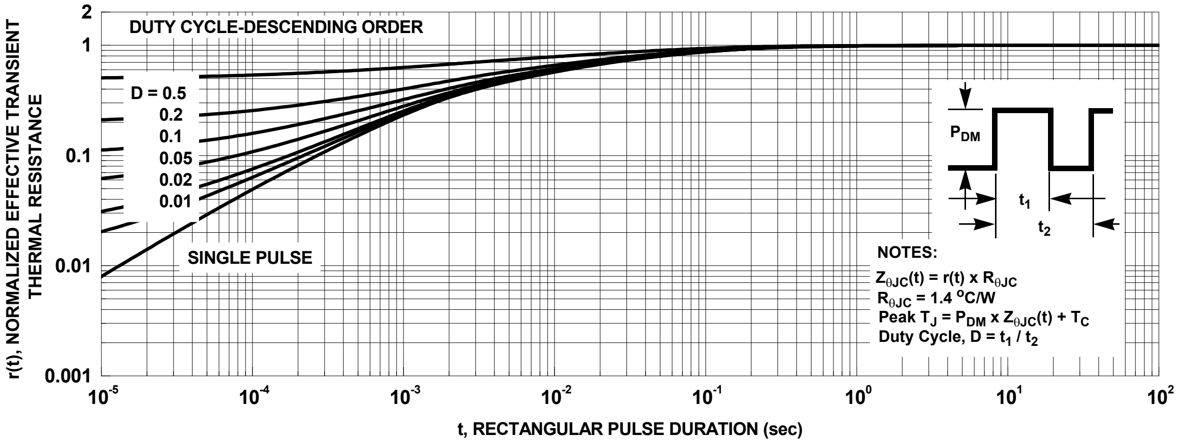


Figure 13. Junction-to-Case Transient Thermal Response Curve for FDP2D3N10C

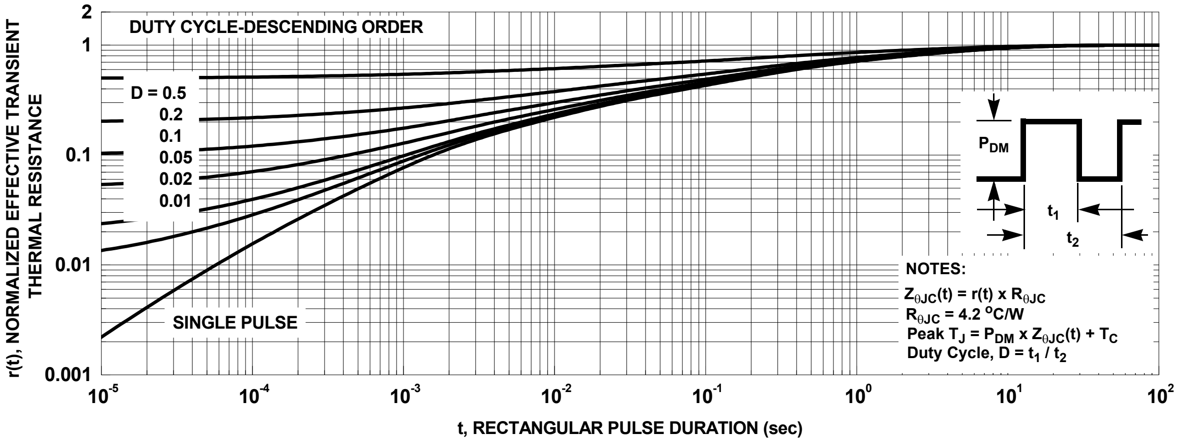
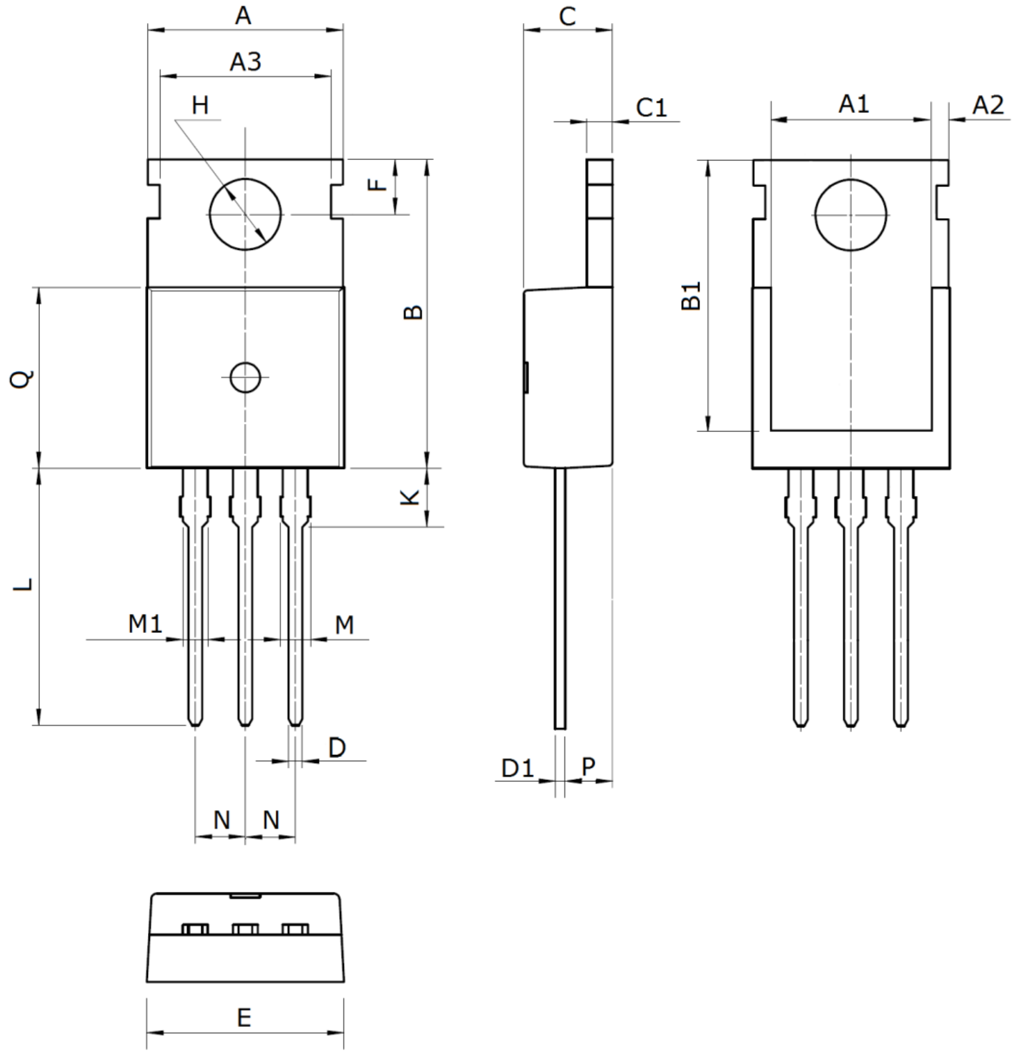


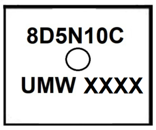
Figure 14. Junction-to-Case Transient Thermal Response Curve for FDPF2D3N10C

Package Mechanical Data TO-220



Symbol	Dimensions (mm)	Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A	10.0±0.3	C1	1.3±0.2	L	13.2±0.4
A1	8.0±0.2	D	0.8±0.2	M	1.38±0.1
A2	0.94±0.1	D1	0.5±0.1	M1	1.28±0.1
A3	8.7±0.1	E	10.0±0.3	N	2.54(typ)
B	15.6±0.4	F	2.8 ±0.1	P	2.4±0.3
B1	13.2 ±0.2	H	3.6±0.1	Q	9.15±0. 25
C	4.5±0. 2	K	3.1±0.2		

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDP8D5N10C	TO-220	1000	Tube and box

单击下面可查看定价，库存，交付和生命周期等信息

[>>UMW(友台半导体)]