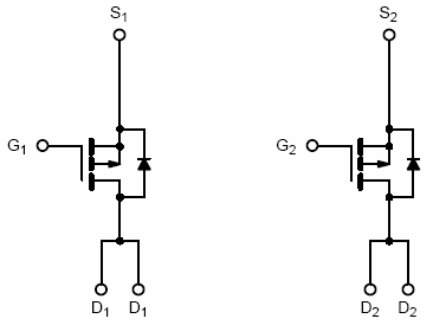
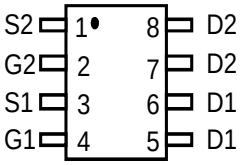
DESCRIPTION

STP4925 is the dual P-Channel logic enhancement mode power field effect transistor are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management,and other battery powered circuits where high-side switching



FEATURES

- $V_{DS\ (V)}$ = -30V
- $R_{DS(ON)}$ < 25mΩ (V_{GS} = 10V)
- $R_{DS(ON)}$ < 32mΩ (V_{GS} = 4.5V)



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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

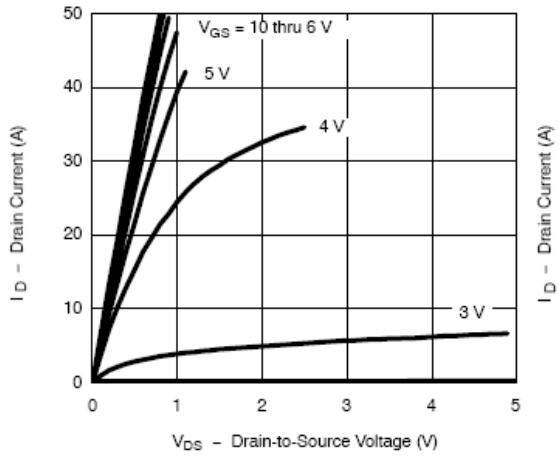
Parameter		Symbol	Typical	Unit
Drain - Source Voltage		V_{DSS}	-30	V
Gate - Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (TJ=150 ℃)	T_A=25 ℃ T_A=70 ℃	I_D	-7.2 -5.6	A
Pulsed Drain Current		I_{DM}	-50	A
Continuous Source Current (Diode Conduction)		I_S	-2.3	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	2.8 1.8	W
Operation Junction Temperature		T_J	-55/150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance -Junction to Ambient		$R_{\theta JA}$	70	℃/W

ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

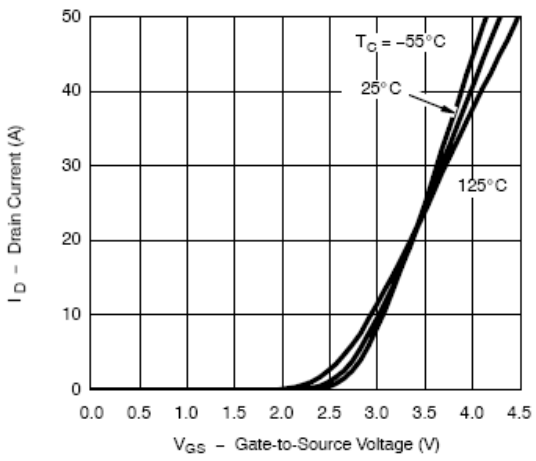
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain - Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D= -250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V $_{GS}$,I_D= -250 uA	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V $_{GS}$= ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS} T_J= 55	V_{DS}= -30 V,V_{GS}=0V			-1	uA
		V_{DS}= -30 V,V_{GS}=0V			-5	
Drain - source On - Resistance	$R_{DS(on)}$	V_{GS}= -10V, I $_D$= -7.2A V_{GS}= -4.5V,I $_D$= -5.6 A		21 29	25 32	mΩ
Forward Tran Conductance	gfs	V_{DS}= -10V,I $_D$= -9.0A		24		S
Diode Forward Voltage	V_{SD}	I_S= -2. 3A,V_{GS}=0V		-0.8	-1. 0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V,V $_{GS}$=-10V I_D≡ -9.0A		16	24	nC
Gate - Source Charge	Q_{gs}			2.3		
Gate - Drain Charge	Q_{gd}			4.5		
Input Capacitance	Ciss	V_{DS} = -15 V,VGS= 0V f=1MHz		1650		pF
Output Capacitance	Coss			350		
Reverse Transfer Capacitance	Crss			235		
Turn - On Time	$t_{d(on)}$ tr	V_{DD}=15V,R $_L$=15 Ω I_D= -1.0A,V $_{GEN}$= -10V R_G=6 Ω		16	30	nS
				17	30	
Turn - Off Time	$t_{d(off)}$ tf			65	110	
				35	80	

TYPICAL CHARACTERICTICS （25℃ Unless Note ）

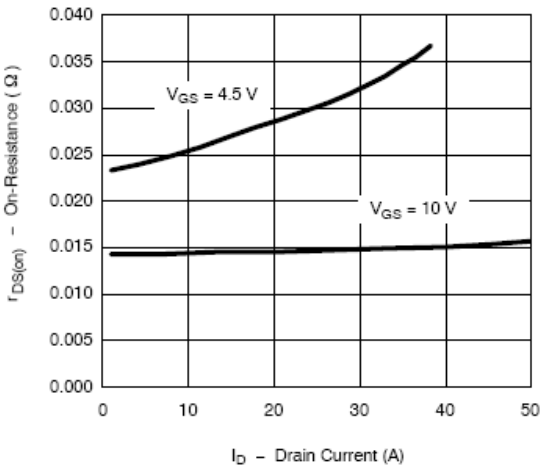
Output Characteristics



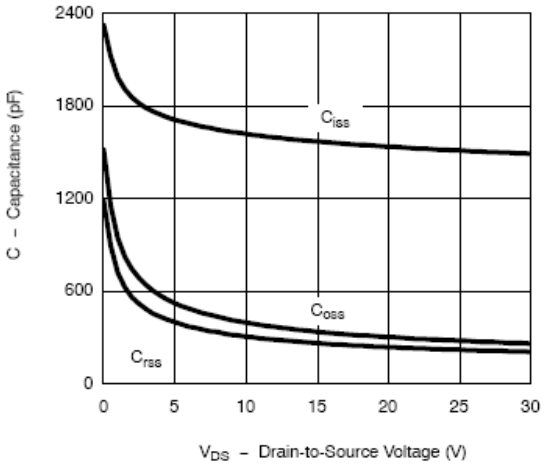
Transfer Characteristics



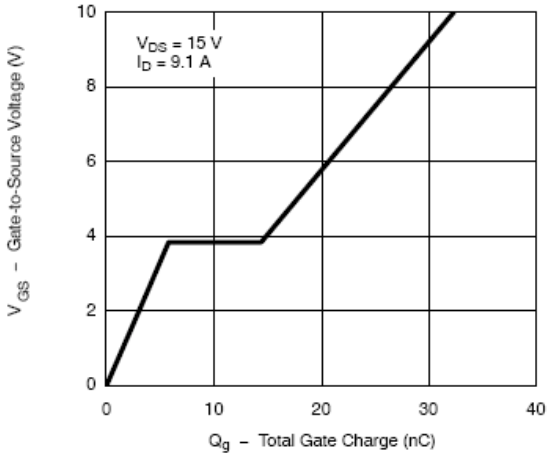
On-Resistance vs. Drain Current



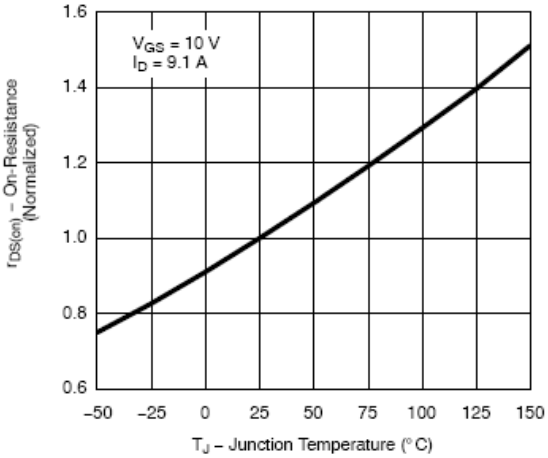
Capacitance



Gate Charge

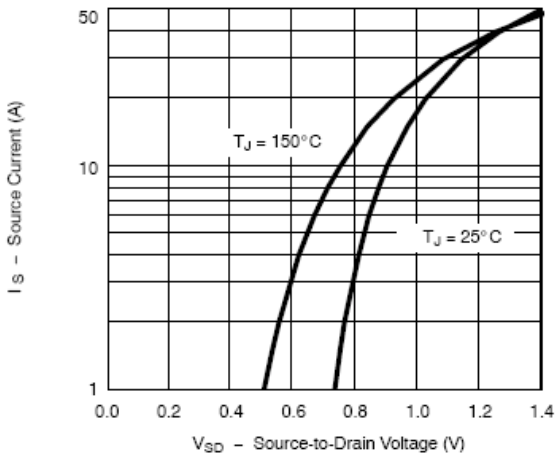


On-Resistance vs. Junction Temperature

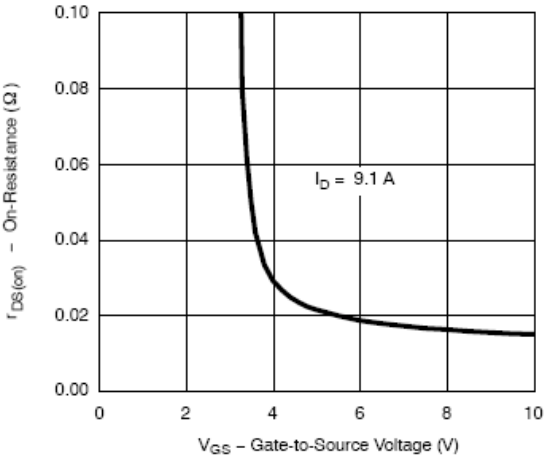


TYPICAL CHARACTERICTICS （25℃ Unless Note ）

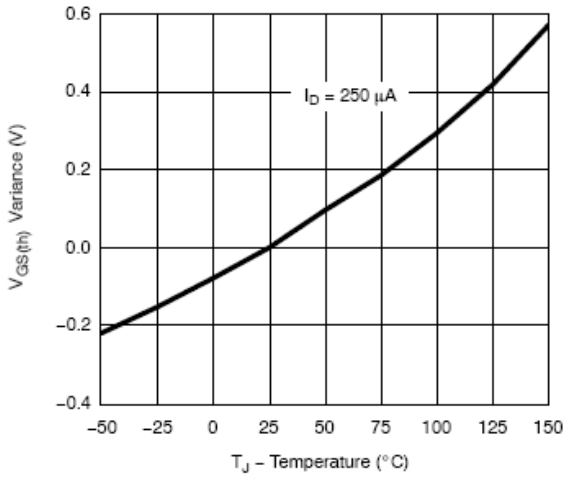
Source-Drain Diode Forward Voltage



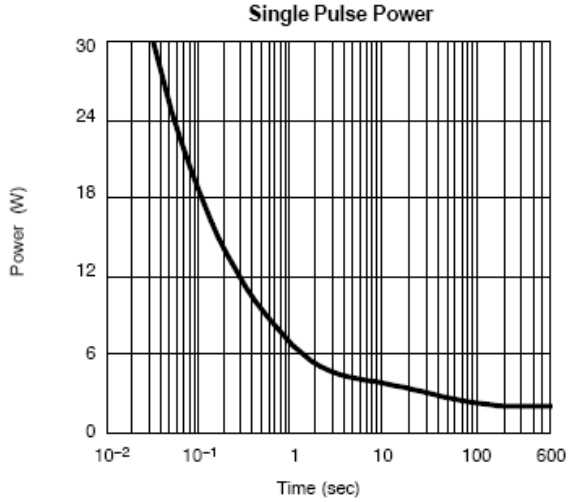
On-Resistance vs. Gate-to-Source Voltage



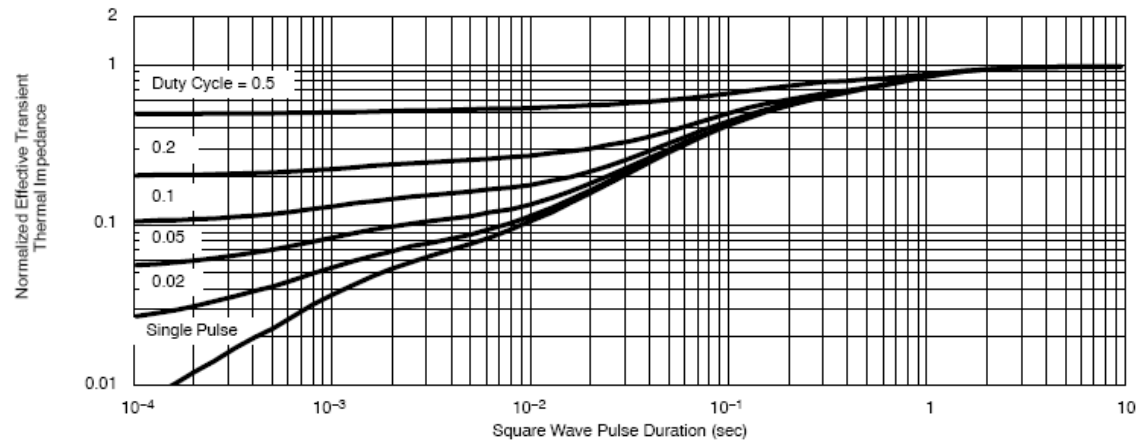
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Foot



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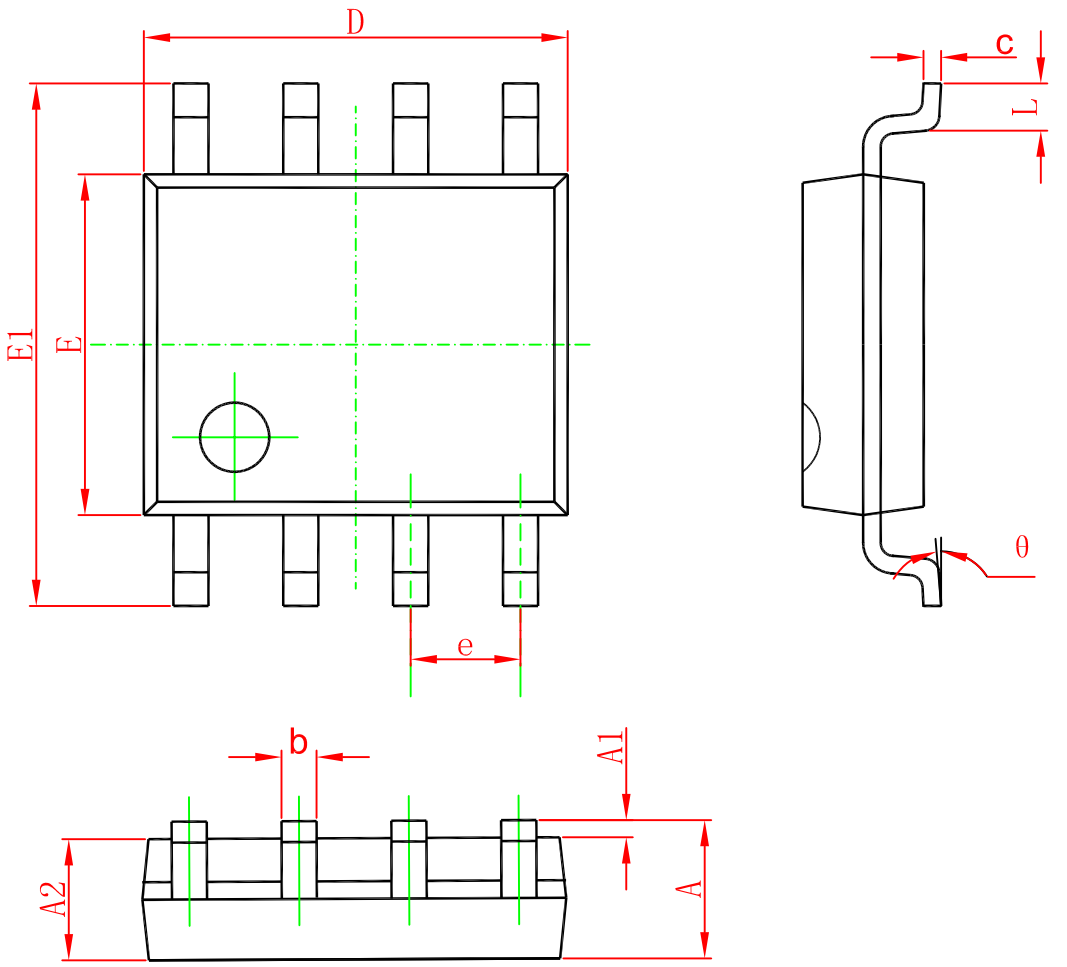
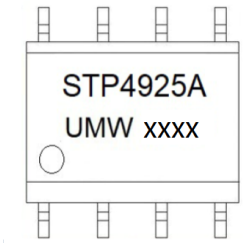


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Order code	Package	Baseqty	Deliverymode
UMW STP4925A	SOP-8	3000	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)