

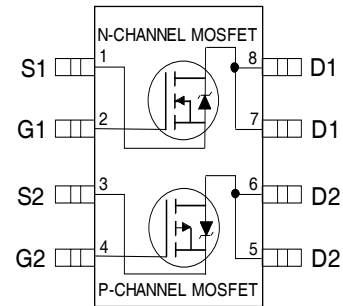
Features

N-Ch:

- $V_{DS} (V) = 25V$
- $R_{DS(ON)} < 100m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 160 m\Omega$ ($V_{GS} = 4.5V$)

P-Ch:

- $V_{DS} (V) = -25V$
- $R_{DS(ON)} < 250m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 400 m\Omega$ ($V_{GS} = 4.5V$)
- Advanced Process Technology Ultra
- Low On-Resistance
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free



Top View

Description

The SOP-8 has been modified through a customized eadframe "or enhanced therma characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave solderino techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.5	-2.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.8	-1.8	
I_{DM}	Pulsed Drain Current ①	14	-10	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	3.0	-3.0	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④			62.5	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	N-Ch	25			V	V _{GS} = 0V, I _D = 250μA
		P-Ch	-25				V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	N-Ch		0.030		V/°C	Reference to 25°C, I _D = 1mA
		P-Ch		-0.015			Reference to 25°C, I _D = -1mA
R _{DS(ON)}	Static Drain-to-Source On-Resistance	N-Ch		83	100	mΩ	V _{GS} = 10V, I _D = 1.0A ③
				140	160		V _{GS} = 4.5V, I _D = 0.50A ③
		P-Ch		160	250		V _{GS} = -10V, I _D = -1.0A ③
				300	400		V _{GS} = -4.5V, I _D = -0.50A ③
V _{GS(th)}	Gate Threshold Voltage	N-Ch	1.0		3.0	V	V _{DS} = V _{GS} , I _D = 250μA
		P-Ch	-1.0		-3.0		V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	N-Ch		4.3		S	V _{DS} = 15V, I _D = 3.5A ③
		P-Ch		3.1			V _{DS} = -15V, I _D = -3.5A ③
I _{DSS}	Drain-to-Source Leakage Current	N-Ch			2.0	μA	V _{DS} = 20V, V _{GS} = 0V
		P-Ch			-2.0		V _{DS} = -20V, V _{GS} = 0V
		N-Ch		25			V _{DS} = 20V, V _{GS} = 0V, T _J = 55°C
		P-Ch		-25			V _{DS} = -20V, V _{GS} = 0V, T _J = 55°C
I _{GSS}	Gate-to-Source Forward Leakage	N-P			±100		V _{GS} = ± 20V
Q _g	Total Gate Charge	N-Ch		9.4	27	nC	N-Channel I _D = 2.3A, V _{DS} = 12.5V, V _{GS} = 10V ③
P-Ch		10	25				
Q _{gs}	Gate-to-Source Charge	N-Ch			1.7	nC	P-Channel I _D = -2.3A, V _{DS} = -12.5V, V _{GS} = -10V
		P-Ch		1.9			
Q _{gd}	Gate-to-Drain ("Miller") Charge	N-Ch			3.1	nC	P-Channel I _D = -2.3A, V _{DS} = -12.5V, V _{GS} = -10V
		P-Ch			2.8		
t _{d(on)}	Turn-On Delay Time	N-Ch		7.0	20	ns	N-Channel V _{DD} = 25V, I _D = 1.0A, R _G = 6.0Ω, R _D = 25Ω
		P-Ch		12	40		
t _r	Rise Time	N-Ch		9.0	20	ns	P-Channel V _{DD} = -25V, I _D = -1.0A, R _G = 6.0Ω, R _D = 25Ω
		P-Ch		13	40		
t _{d(off)}	Turn-Off Delay Time	N-Ch		45	90	ns	P-Channel V _{DD} = -25V, I _D = -1.0A, R _G = 6.0Ω, R _D = 25Ω
		P-Ch		45	90		
t _f	Fall Time	N-Ch		25	50	ns	P-Channel V _{DD} = -25V, I _D = -1.0A, R _G = 6.0Ω, R _D = 25Ω
		P-Ch		25	50		
L _S	Internal Drain Inductance	N-P		4.0		nH	Between lead, 6mm (0.25in.) from package and center of die contact
P-Ch		37	50				
L _P	Internal Source Inductance	N-P		6.0		nH	Between lead, 6mm (0.25in.) from package and center of die contact
P-Ch		37	50				
C _{iss}	Input Capacitance	N-Ch		330		pF	N-Channel V _{GS} = 0V, V _{DS} = 15V, f = 1.0MHz
		P-Ch		290			
C _{oss}	Output Capacitance	N-Ch		250		pF	P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
		P-Ch		210			
C _{rss}	Reverse Transfer Capacitance	N-Ch		61		pF	P-Channel V _{GS} = 0V, V _{DS} = -15V, f = 1.0MHz
		P-Ch		67			

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	N-Ch			2.0	A	
		P-Ch			-2.0		
I _{SM}	Pulsed Source Current (Body Diode) ①	N-Ch			14	A	
		P-Ch			-9.2		
V _{SD}	Diode Forward Voltage	N-Ch			1.2	V	T _J = 25°C, I _S = 1.3A, V _{GS} = 0V ③
		P-Ch			-1.2		T _J = 25°C, I _S = -1.3A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	N-Ch		36	54	ns	N-Channel T _J = 25°C, I _F = 1.3A, di/dt = 100A/μs
		P-Ch		69	100		
Q _{rr}	Reverse Recovery Charge	N-Ch		41	75	nC	P-Channel T _J = 25°C, I _F = -1.3A, di/dt = 100A/μs ③
		P-Ch		90	180		
t _{on}	Forward Turn-On Time	N-P					Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② N-Channel I_{SD} ≤ 3.5A, di/dt ≤ 90A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
P-Channel I_{SD} ≤ -2.3A, di/dt ≤ 90A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ Surface mounted on FR-4 board, t ≤ 10sec.

N-Channel

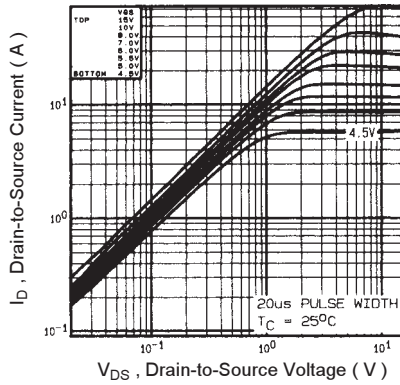


Fig 1. Typical Output Characteristics

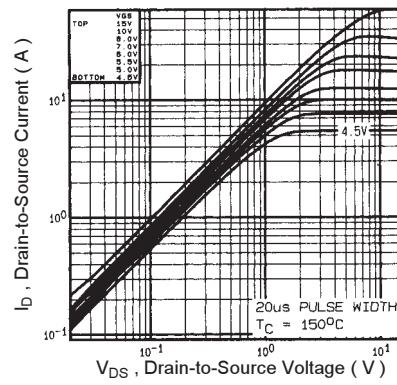


Fig 2. Typical Output Characteristics

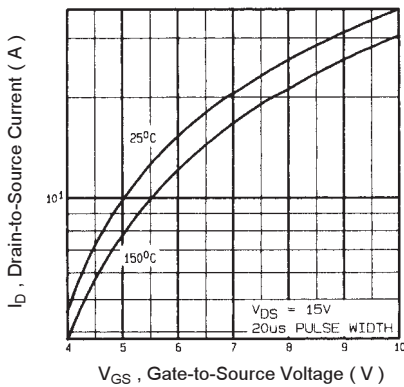


Fig 3. Typical Transfer Characteristics

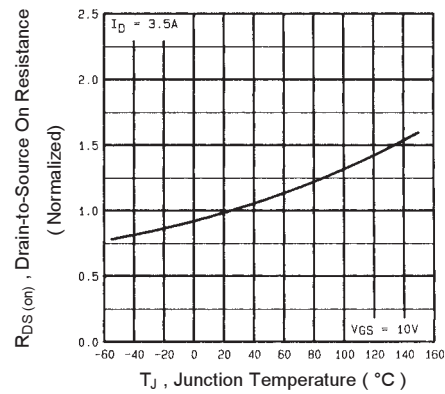


Fig 4. Normalized On-Resistance Vs. Temperature

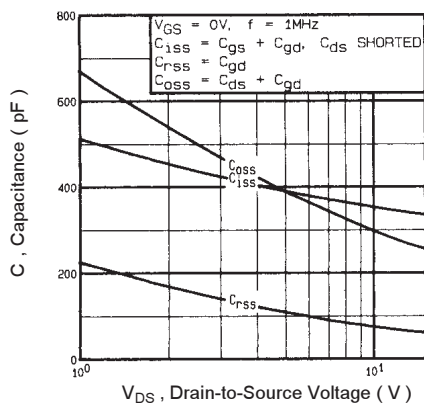


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

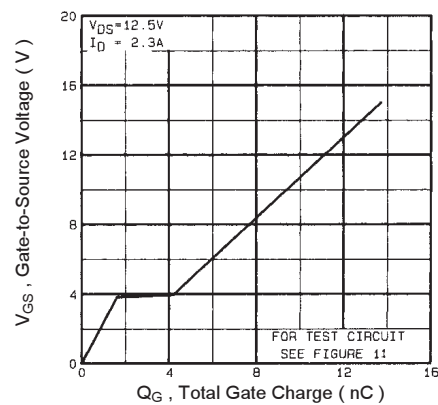


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

N-Channel

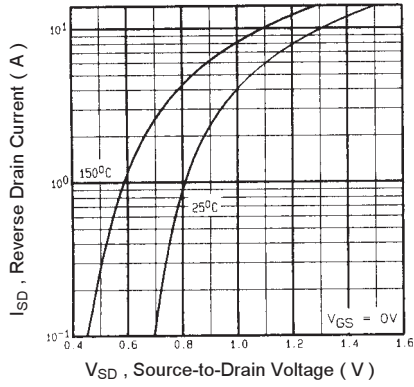


Fig 7. Typical Source-Drain Diode Forward Voltage

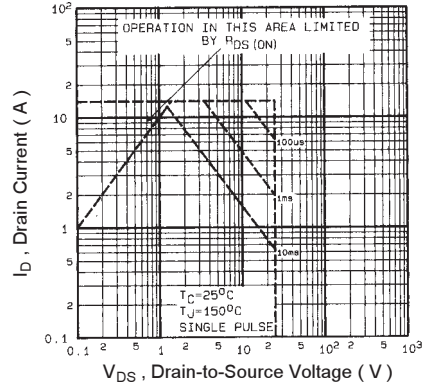


Fig 8. Maximum Safe Operating Area

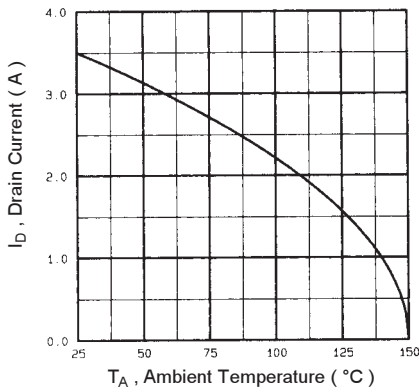


Fig 9. Maximum Drain Current Vs. Ambient Temperature

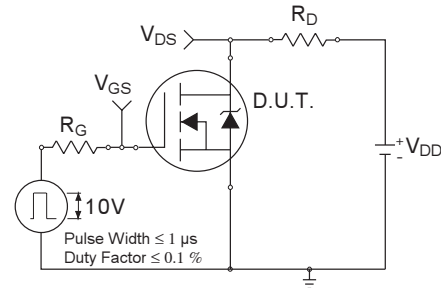


Fig 10a. Switching Time Test Circuit

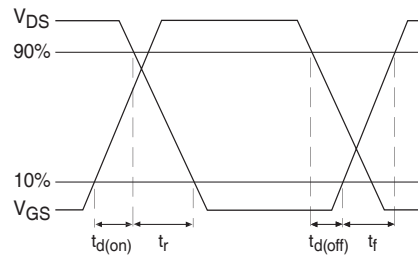


Fig 10b. Switching Time Waveforms

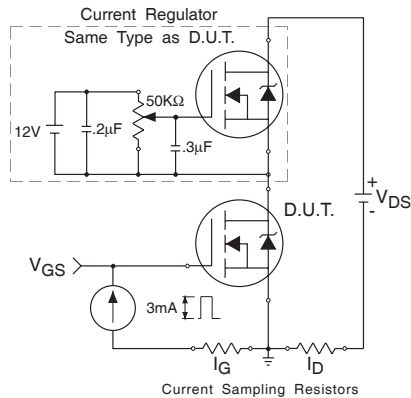


Fig 11a. Gate Charge Test Circuit

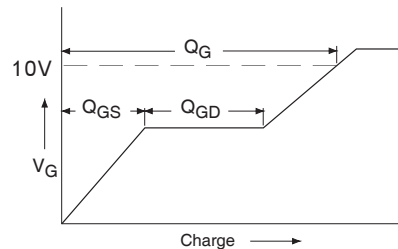


Fig 11b. Basic Gate Charge Waveform

P-Channel

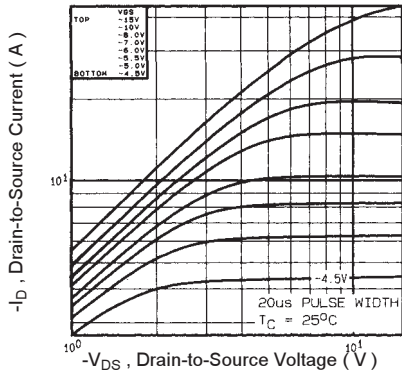


Fig 12. Typical Output Characteristics

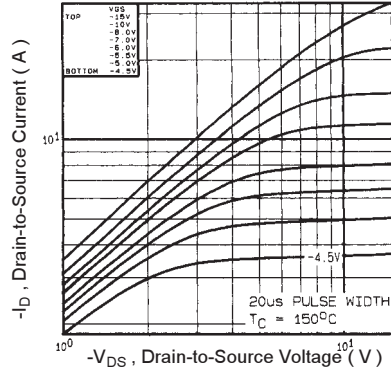


Fig 13. Typical Output Characteristics

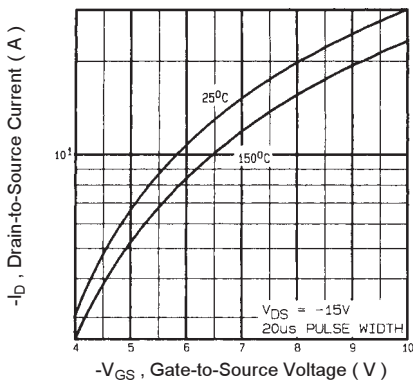


Fig 14. Typical Transfer Characteristics

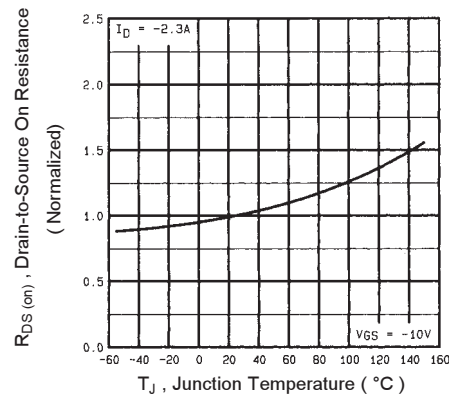


Fig 15. Normalized On-Resistance Vs. Temperature

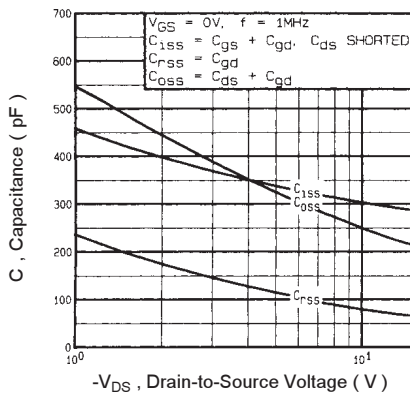


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

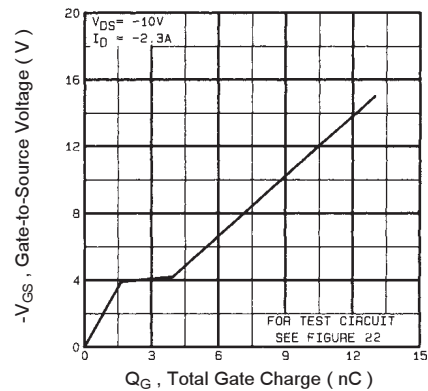


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

P-Channel

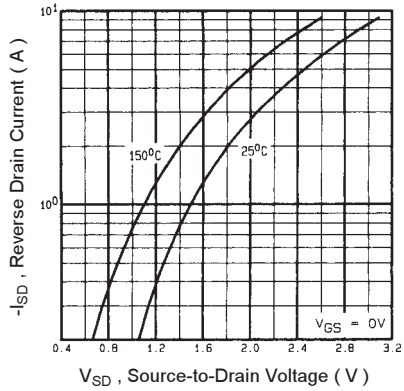


Fig 18. Typical Source-Drain Diode Forward Voltage

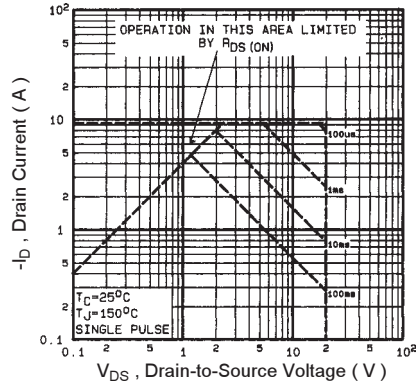


Fig 19. Maximum Safe Operating Area

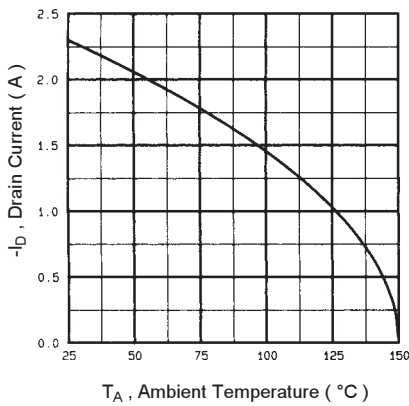


Fig 20. Maximum Drain Current Vs. Ambient Temperature

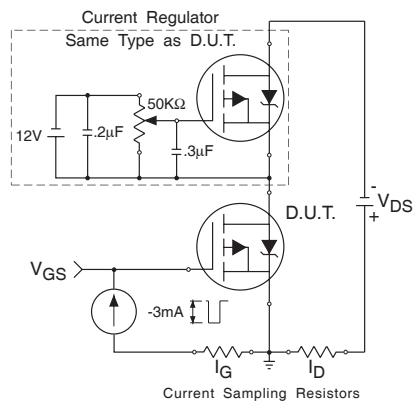


Fig 22a. Gate Charge Test Circuit

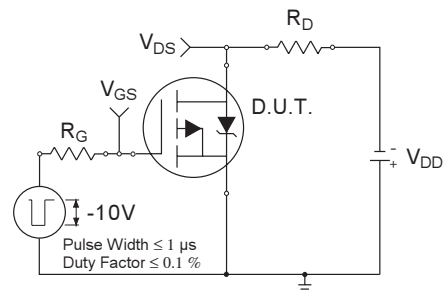


Fig 21a. Switching Time Test Circuit

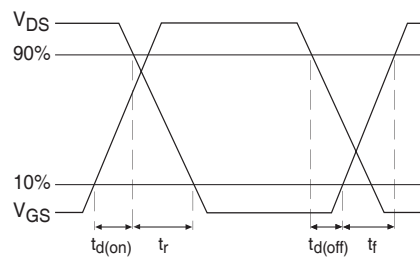


Fig 21b. Switching Time Waveforms

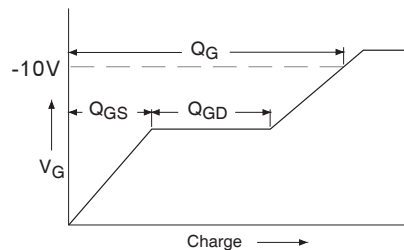


Fig 22b. Basic Gate Charge Waveform

N & P-Channel

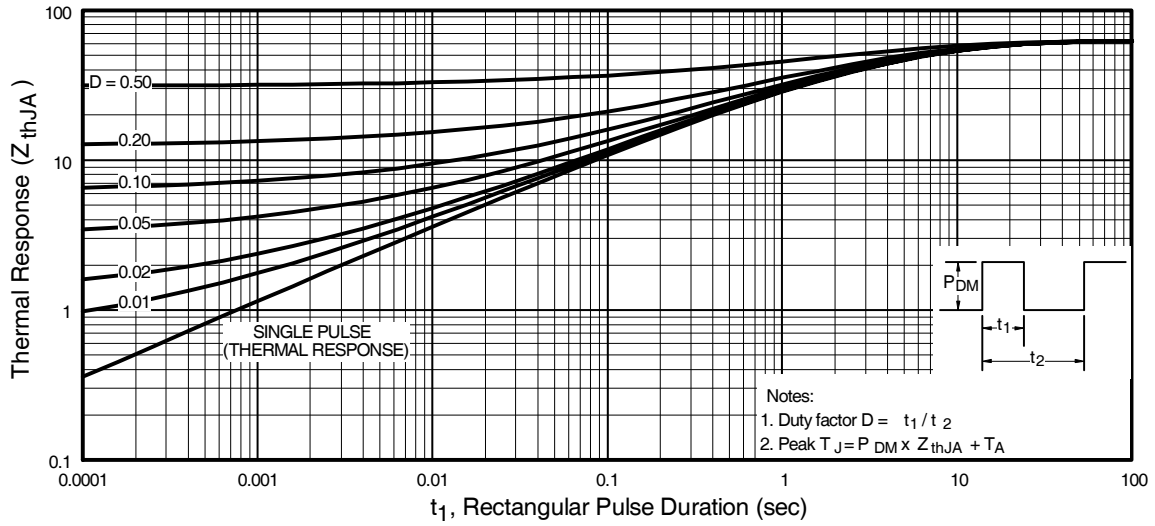
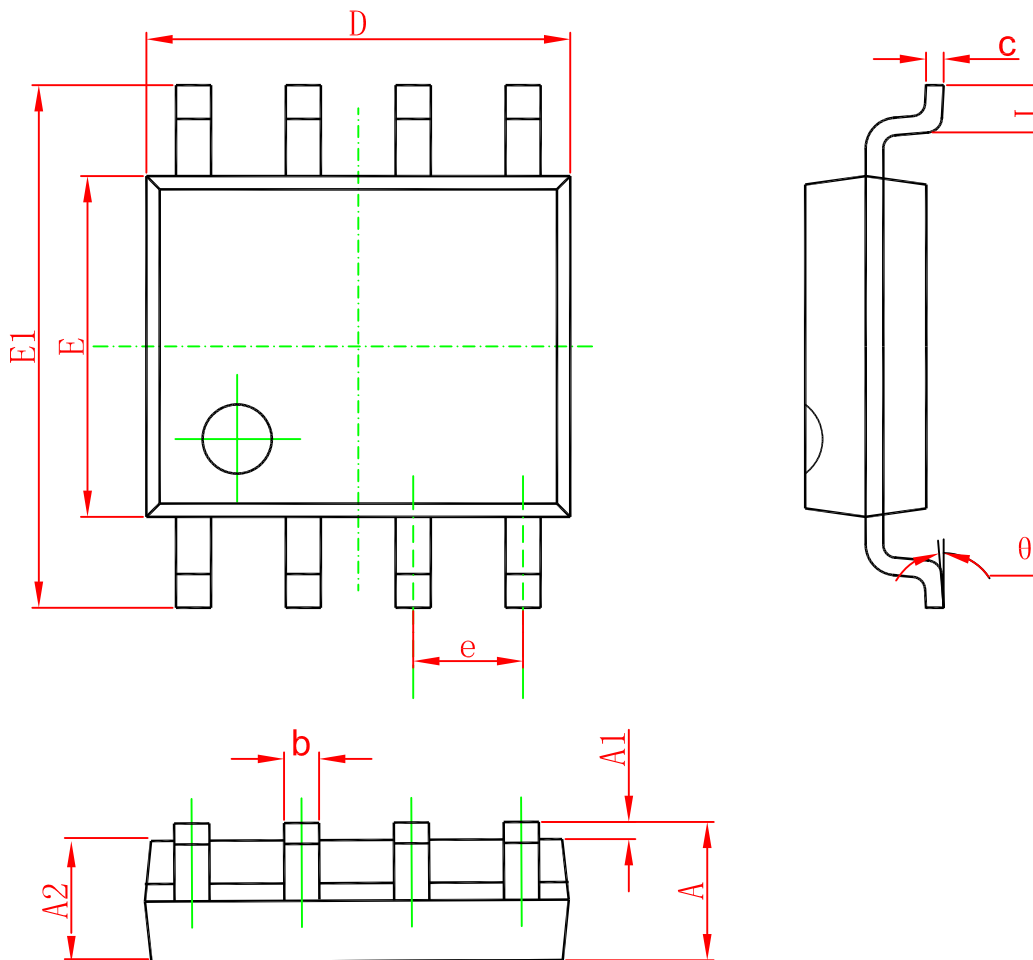


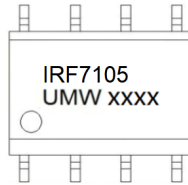
Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRF7105TR	SOP-8	3000	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

[>>UMW\(友台半导体\)](#)