FDN337

N-Channel 30 V (D-S) MOSFET

General Description

These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

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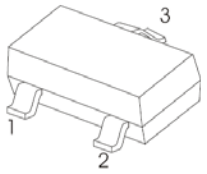
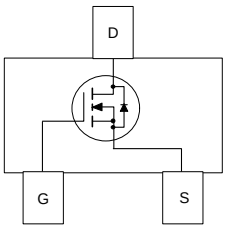


1. GATE
2. SOURCE
3. DRAIN

Features

- $V_{DS\ (V)}$ = 30V
- I_D= 2.2A (V_{GS}=4.5V)
- $R_{DS(ON)}$ ＜ 65mΩ (V_{GS} = 4.5V)
- $R_{DS(ON)}$ ＜ 82mΩ (V_{GS} = 2.5V)
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter	FDN337N	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage - Continuous	±8	V
I_D	Drain/Output Current - Continuous	2.2	A
	- Pulsed	10	
P_D	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		41		mV/ °C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V,V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4	0.7	1	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = 250 µA, Referenced to 25 °C		-2.3		mV/ °C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 2.2 A		54	65	mΩ
		V_{GS} = 2.5 V, I_D = 2 A		70	82	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 2.2 A		13		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		300		pF
C_{oss}	Output Capacitance			145		pF
C_{rss}	Reverse Transfer Capacitance			35		pF
SWITCHING CHARACTERISTICS (Note)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		4	10	ns
t_r	Turn - On Rise Time			10	18	ns
$t_{D(off)}$	Turn - Off Delay Time			17	28	ns
t_f	Turn - Off Fall Time			4	10	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 2.2 A, V_{GS} = 4.5 V		7	9	nC
Q_{gs}	Gate-Source Charge			1.1		nC
Q_{gd}	Gate-Drain Charge			1.9		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note)		0.65	1.2	V

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Typical $R_{\theta JA}$ using the board layouts shown below on FR-4 PCB in a still air environment :

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

a. 250°C/W when mounted on 0.02 in^2 pad of 2oz Cu.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz Cu.

Typical Electrical Characteristics

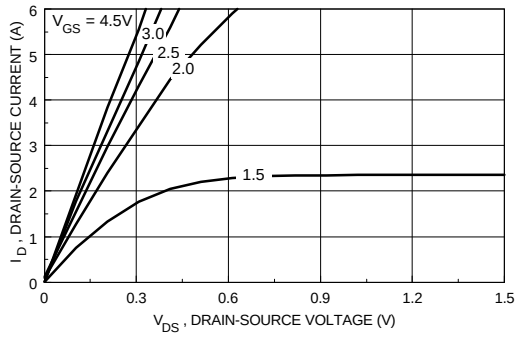


Figure 1. On-Region Characteristics.

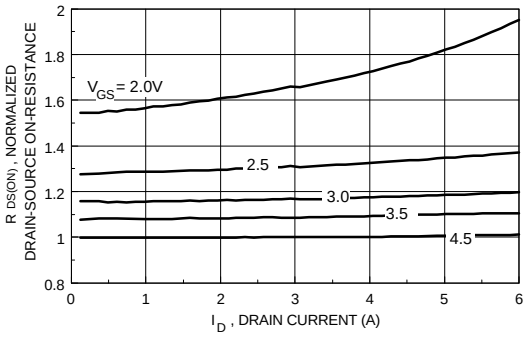


Figure 2. On-Resistance Variation with Drain Current and Gate

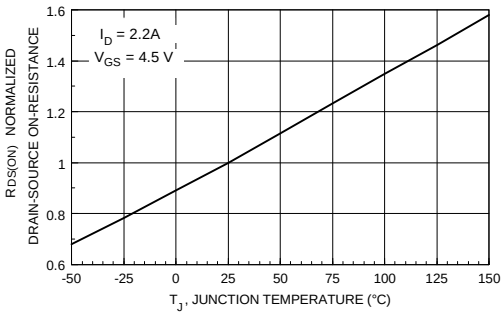


Figure 3. On-Resistance Variation with Temperature.

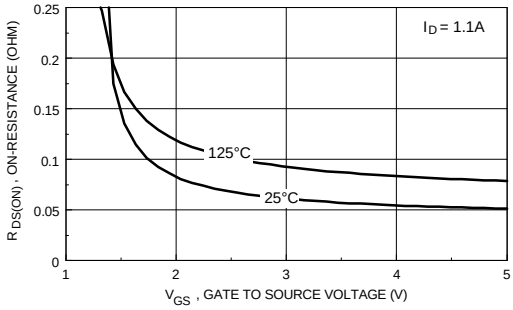


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

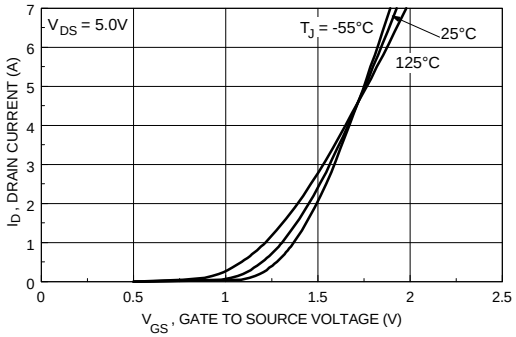
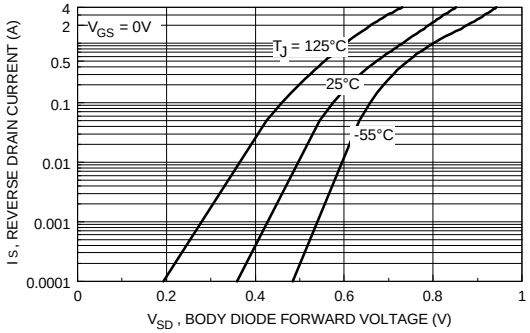


Figure 5. Transfer Characteristics.



Typical Electrical Characteristics (continued)

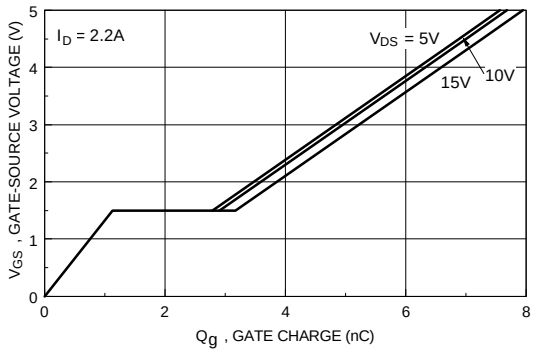


Figure 7. Gate Charge Characteristics.

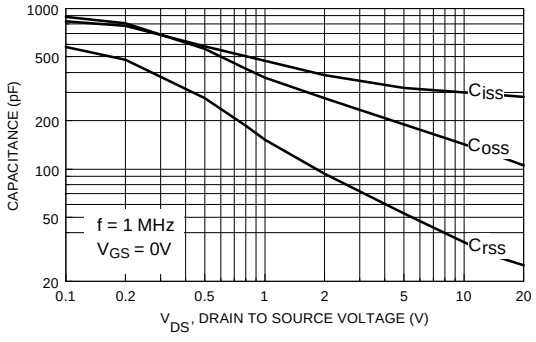


Figure 8. Capacitance Characteristics.

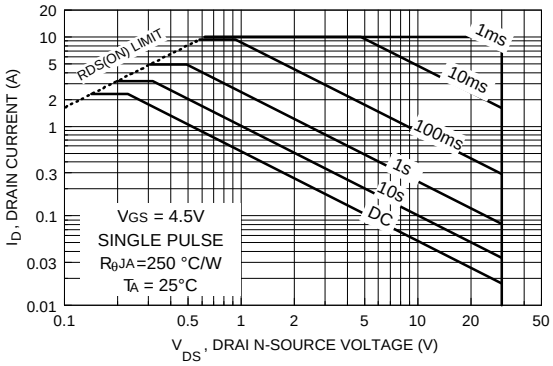


Figure 9. Maximum Safe Operating Area.

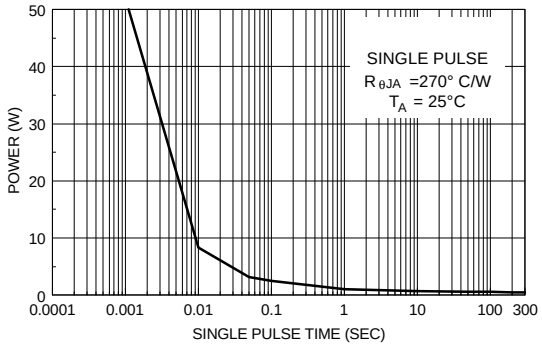


Figure 10. Single Pulse Maximum Power Dissipation.

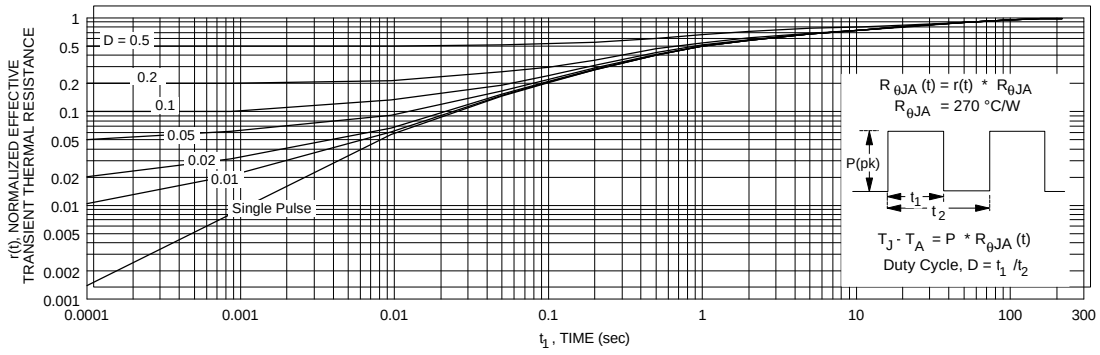
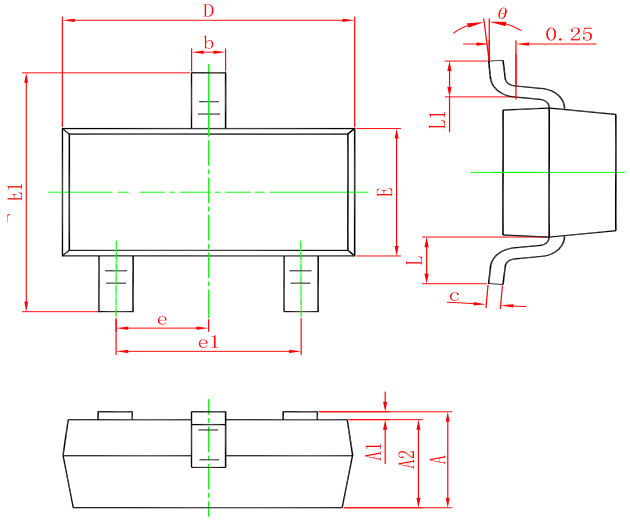


Figure 11. Transient Thermal Response Curve.

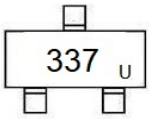
Thermal characterization performed using the conditions described in note 1b.
Transient thermal response will change depending on the circuit board design.

SOT-23 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDN337N	SOT-23	3000	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)