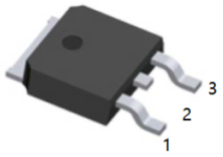
Applications

- DC/DC converter
- Low side notebook

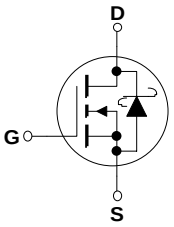


1.G 2.D 3.S

TO-252(DPAK) top view

Features

- V_{DS}(V) = 30V
- I_D = 90A (V_{GS}= 10V)
- $R_{DS(ON)}$ <5.7mΩ (V_{GS} = 10V)
- $R_{DS(ON)}$ <7.1mΩ (V_{GS} = 4.5V)
- Low gate charge (46nC typical)
- High power and current handling capability



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 3)	90	A
	– Pulsed	(Note 1a)	100	
P_D	Power Dissipation for Single Operation	(Note 1)	70	W
		(Note 1a)	3.1	
		(Note 1b)	1.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	°C/W

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, V_{DD} = 15 V, I_D = 16A		108	250	mJ
I_{AR}	Drain-Source Avalanche Current				16	A
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C		31		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			500	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	1	1.5	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C		–3.6		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 16 A V_{GS} = 4.5 V, I_D = 15 A		4.7 5.8	5.7 7.1	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 16 A		61		S
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		2500		pF
C_{oss}	Output Capacitance			710		pF
C_{rss}	Reverse Transfer Capacitance			270		pF
R_G	Gate Resistance	V_{GS} = 0 V, f = 1.0 MHz		1.6		Ω
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		12	21	ns
t_r	Turn–On Rise Time			12	22	ns
$t_{d(off)}$	Turn–Off Delay Time			46	74	ns
t_f	Turn–Off Fall Time			28	44	ns
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		20	32	ns
t_r	Turn–On Rise Time			24	38	ns
$t_{d(off)}$	Turn–Off Delay Time			35	56	ns
t_f	Turn–Off Fall Time			27	43	ns
$Q_{g(TOT)}$	Total Gate Charge, Vgs = 10V	V_{DS} = 15 V, I_D = 16 A		46	64	nC
Q_g	Total Gate Charge, Vgs = 5V			25	35	nC
Q_{gs}	Gate–Source Charge			7		nC
Q_{gd}	Gate–Drain Charge			9		nC

Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_S	Maximum Continuous Drain–Source Diode Forward Current				3.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.5 A (Note 2)		0.4	0.7	V
t_{RR}	Diode Reverse Recovery Time	dI_F/dt = 300A/us, I_F = 16A		25		ns
I_{RM}	Maximum Recovery Current			1.9		A
Q_{RR}	Diode Reverse Recovery Charge			24		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in^2 pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10V. Package current limitation is 21A

Typical Characteristics

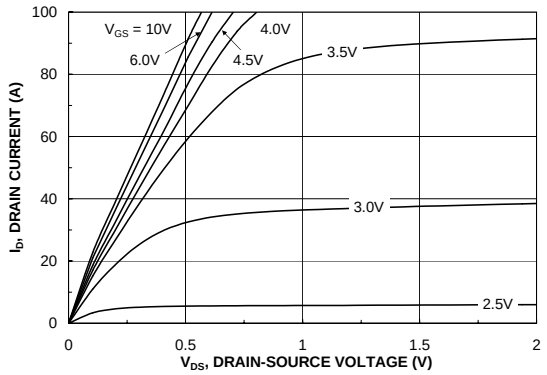


Figure 1. On-Region Characteristics

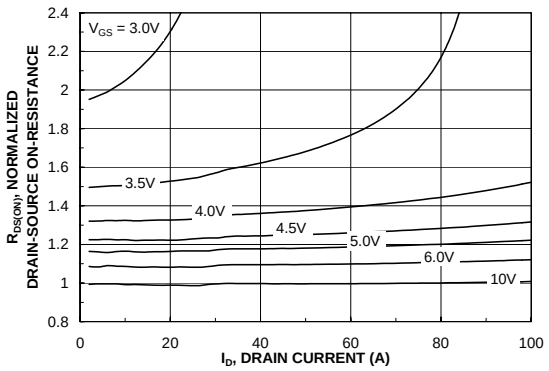


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

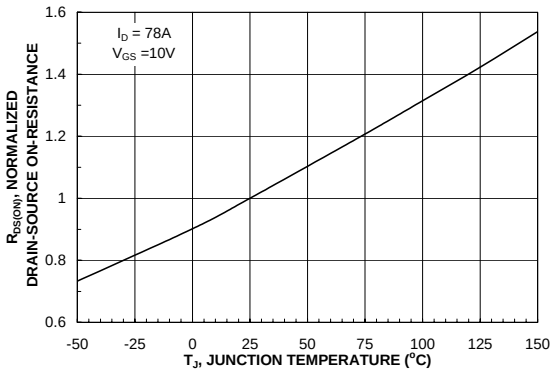


Figure 3. On-Resistance Variation with Temperature

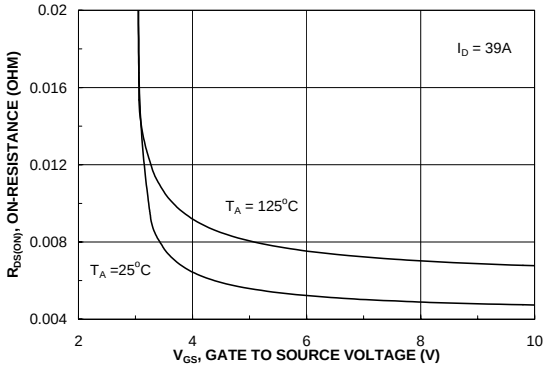


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

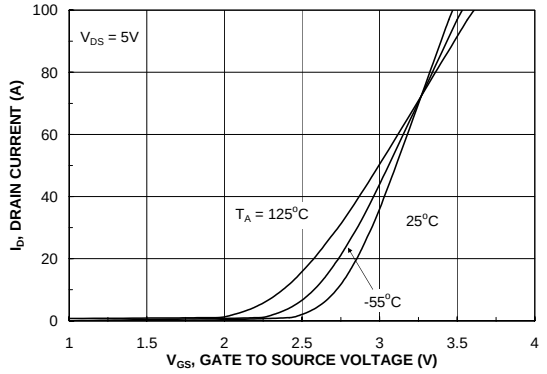


Figure 5. Transfer Characteristics

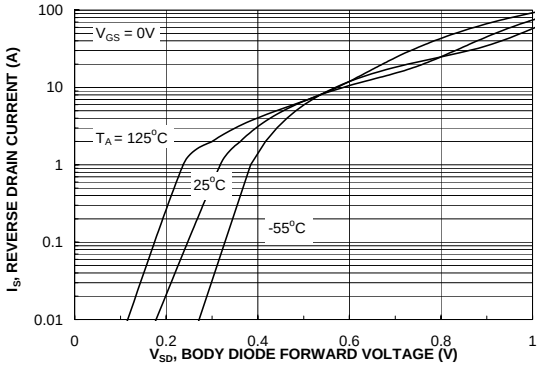


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

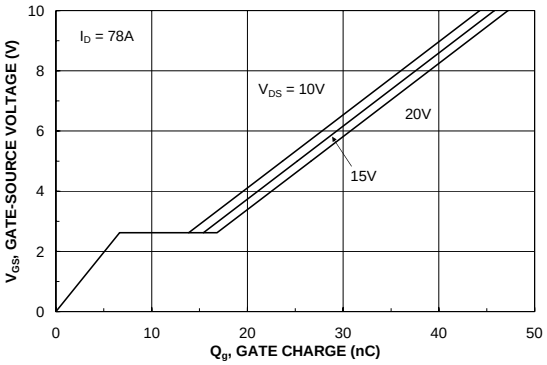


Figure 7. Gate Charge Characteristics

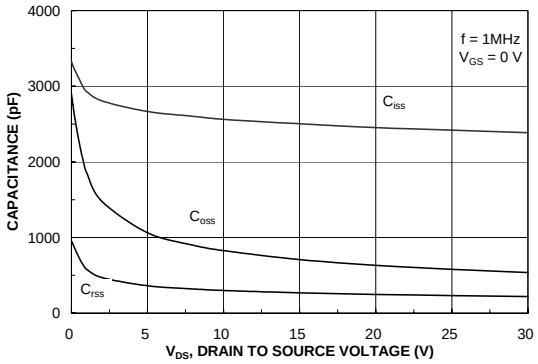


Figure 8. Capacitance Characteristics

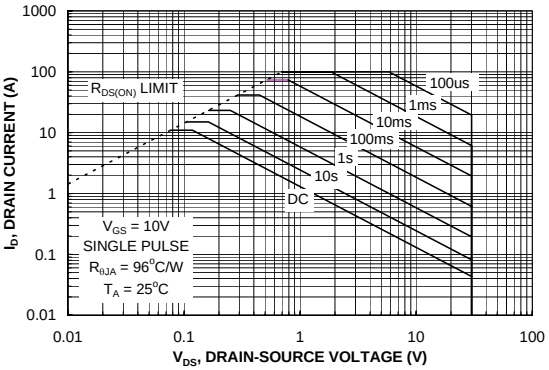


Figure 9. Maximum Safe Operating Area

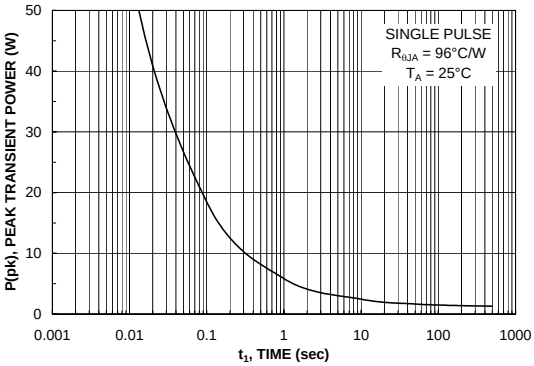


Figure 10. Single Pulse Maximum Power Dissipation

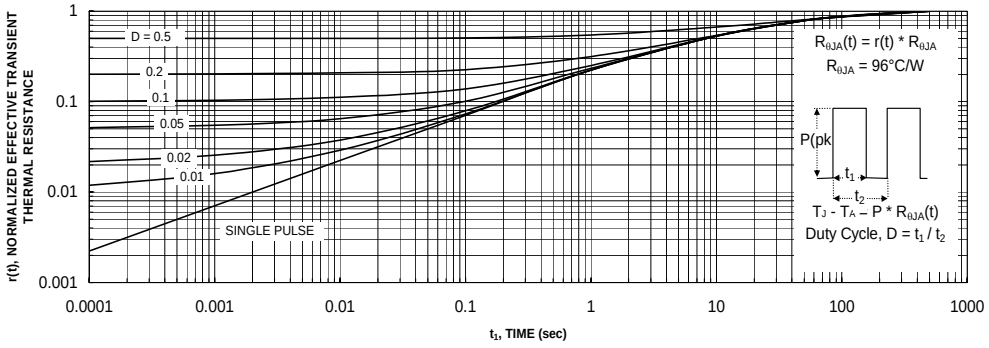
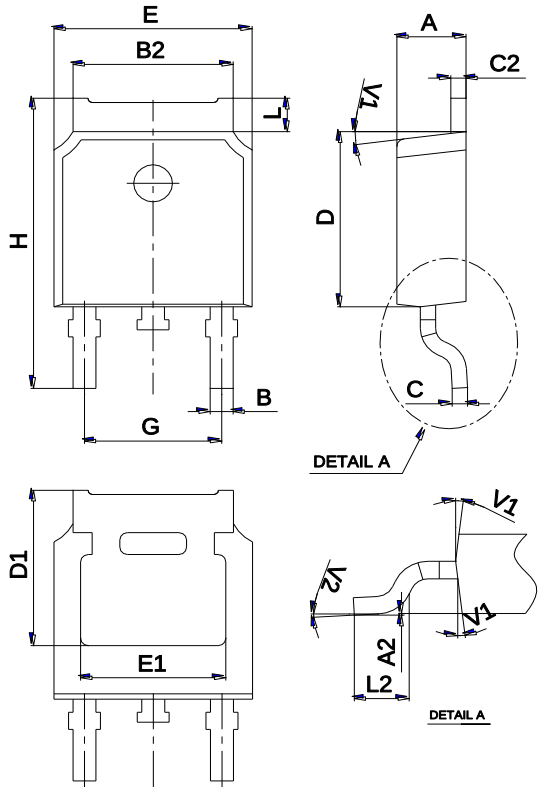


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking

Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDD6676AS	TO-252	2500	Tape and reel

单击下面可查看定价，库存，交付和生命周期等信息

>>UMW(友台半导体)