



2P50

POWER MOSFET

-2A, -500V P-CHANNEL POWER MOSFET

■ DESCRIPTION

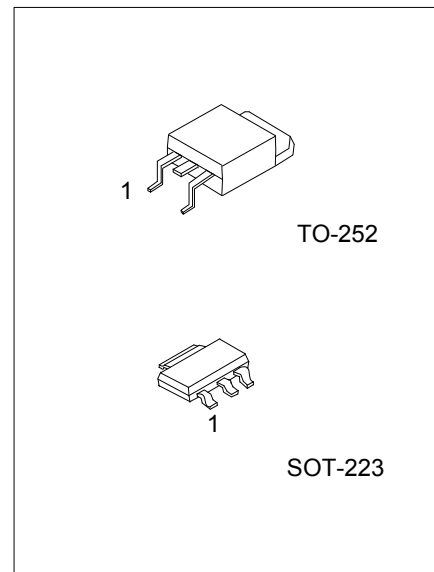
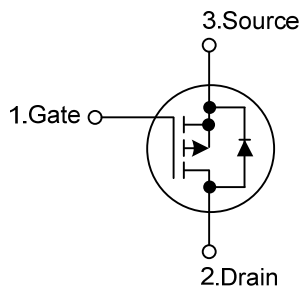
The UTC **2P50** is a P-channel MOS Field Effect Transistor. it uses UTC's advanced technology to provide the customers with high switching speed and a minimum on-state resistance.

The UTC **2P50** is suitable for high voltage switching applications.

■ FEATURES

- * $R_{DS(ON)} \leq 8.5\Omega$ @ $V_{GS}=-10V, I_D=-1.0A$
- * High switching speed
- * Low input capacitance

■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2P50L-AA3-R	2P50G-AA3-R	SOT-223	G	D	S	Tape Reel
2P50L-TN3-R	2P50G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>2P50G-AA3-R</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) AA3: SOT-223, TN3: TO-252 (3) G: Halogen Free and Lead Free, L: Lead Free
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■ MARKING

SOT-223	TO-252

■ ABSOLUTE MAXIMUM RATING ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	-500	V
Gate-Source Voltage		V_{GSS}	± 30	V
Drain Current	DC	$I_{D(DC)}$	-2	A
	Pulsed (Note 2)	$I_{D(pulse)}$	-6	A
Single Avalanche Energy (Note 3)		E_{AS}	150	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	16.5	V/ns
Power Dissipation ($T_C=25^\circ\text{C}$)	SOT-223	P_D	6.9	W
	TO-252		41	W
Junction Temperature		T_J	+150	$^\circ\text{C}$
Storage Temperature Range		T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating : Pulse width limited by maximum junction temperature.

3. $L=88\text{mH}$, $I_{AS}=-1.85\text{A}$, $V_{DD}=-50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$.

4. $I_{SD} \leq -2.0\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	SOT-223	θ_{JA}	150	$^\circ\text{C}/\text{W}$
	TO-252		110	$^\circ\text{C}/\text{W}$
Junction to Case	SOT-223	θ_{JC}	18	$^\circ\text{C}/\text{W}$
	TO-252		3	$^\circ\text{C}/\text{W}$

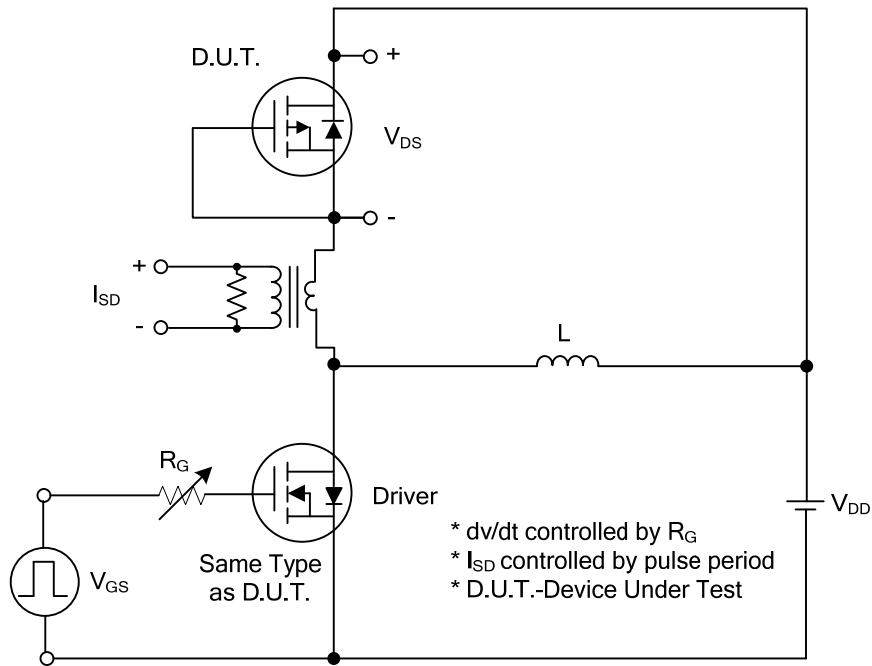
■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=-500\text{V}$, $V_{GS}=0\text{V}$			-10	μA
Gate-Source Leakage Current	I_{GSS}	Forward			+100	nA
		Reverse	$V_{GS}=-30\text{V}$, $V_{DS}=0\text{V}$		-100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-2.0		-4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10\text{V}$, $I_D=-1.0\text{A}$			8.5	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{GS}=0\text{V}$, $V_{DS}=-25\text{V}$, $f=1.0\text{MHz}$		343		pF
Output Capacitance	C_{OSS}			59		pF
Reverse Transfer Capacitance	C_{RSS}			9		pF
SWITCHING PARAMETERS						
Total Gate Charge	Q_G	$V_{DS}=-100\text{V}$, $V_{GS}=-10\text{V}$, $I_D=-2\text{A}$, $I_G=-1\text{mA}$ (Note 1, 2)		11.5		nC
Gate to Source Charge	Q_{GS}			2.8		nC
Gate to Drain Charge	Q_{GD}			3.2		nC
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD}=-100\text{V}$, $V_{GS}=-10\text{V}$, $I_D=-2\text{A}$, $R_G=25\Omega$ (Note 1, 2)		6.4		ns
Rise Time	t_R			16		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			37		ns
Fall-Time	t_F			25		ns
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I_S				-2	A
Maximum Body-Diode Pulsed Current	I_{SM}				-6	A
Diode Forward Voltage	V_{SD}	$I_F=-2\text{A}$, $V_{GS}=0\text{V}$			1.4	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F=-2\text{A}$, $V_{GS}=0\text{V}$, $di/dt=100\text{A}/\mu\text{s}$		200		ns
Body Diode Reverse Recovery Charge	Q_{rr}			1800		nC

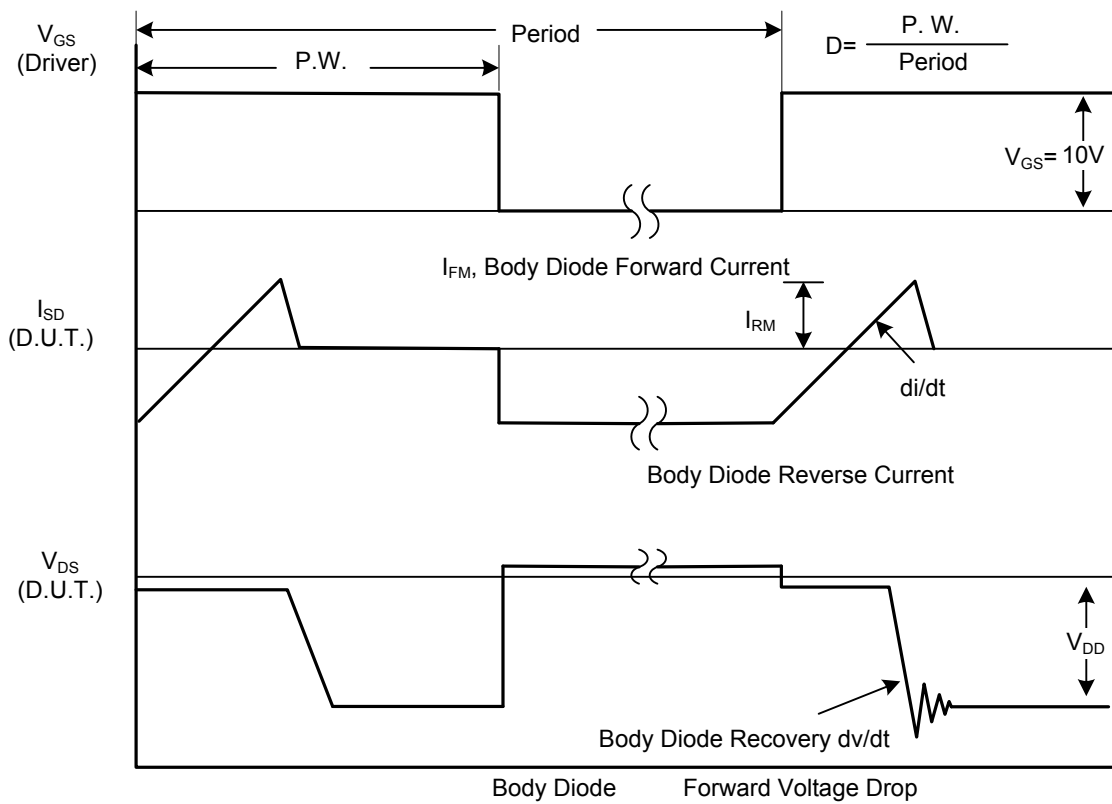
Notes: 1. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

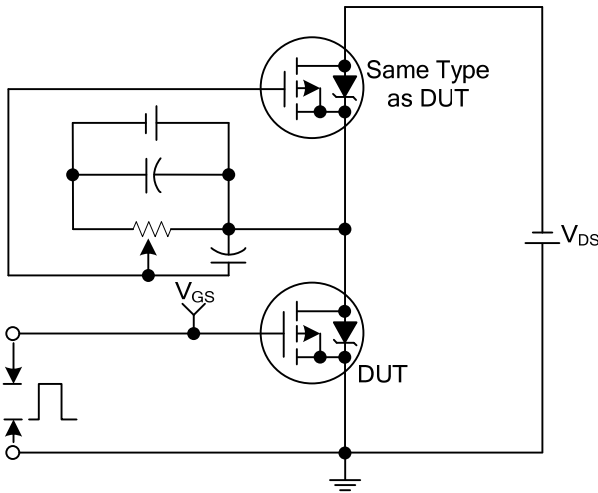


Peak Diode Recovery dv/dt Test Circuit

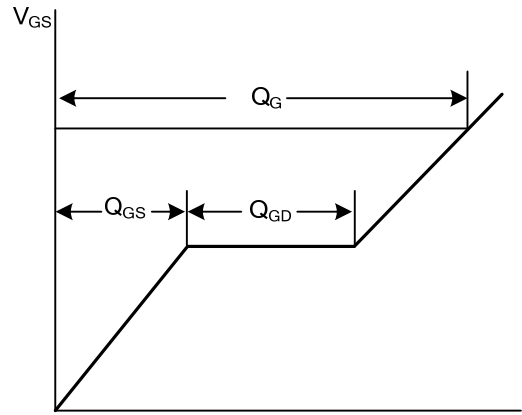


Peak Diode Recovery dv/dt Waveforms

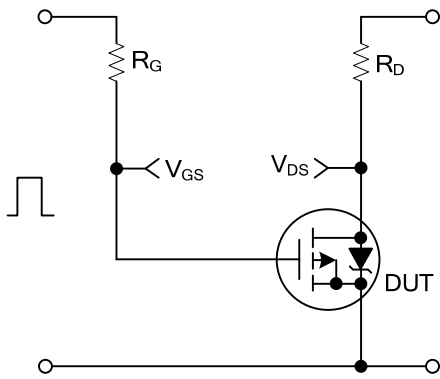
■ TEST CIRCUITS AND WAVEFORMS



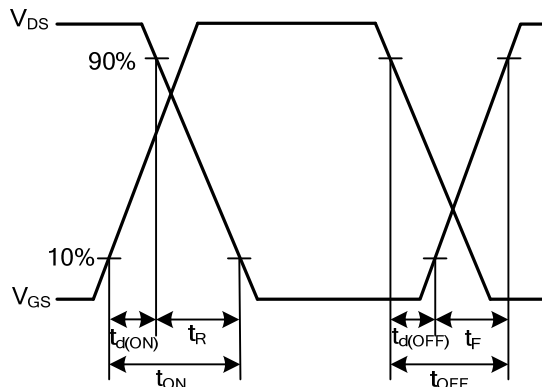
Gate Charge Test Circuit



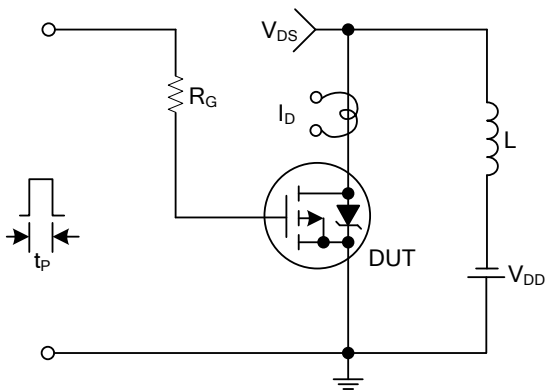
Gate Charge Waveforms



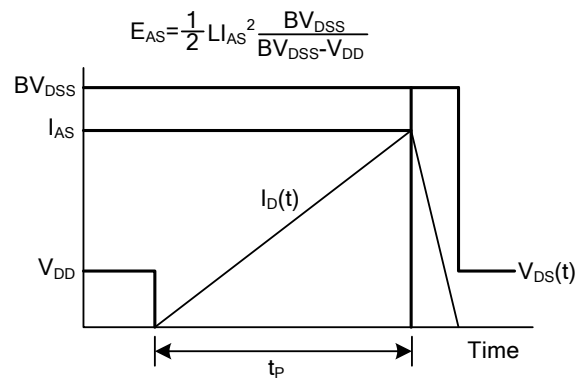
Resistive Switching Test Circuit



Resistive Switching Waveforms

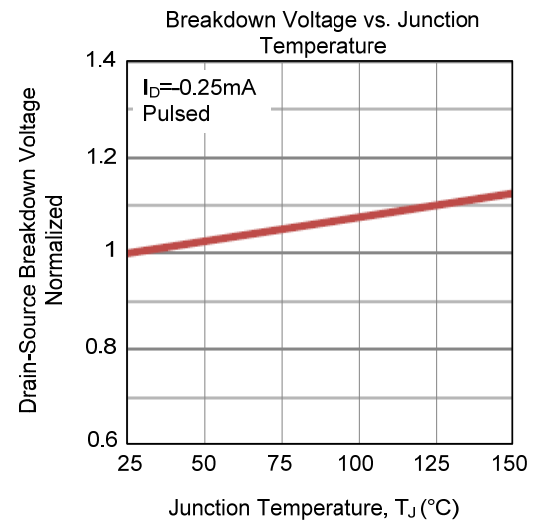
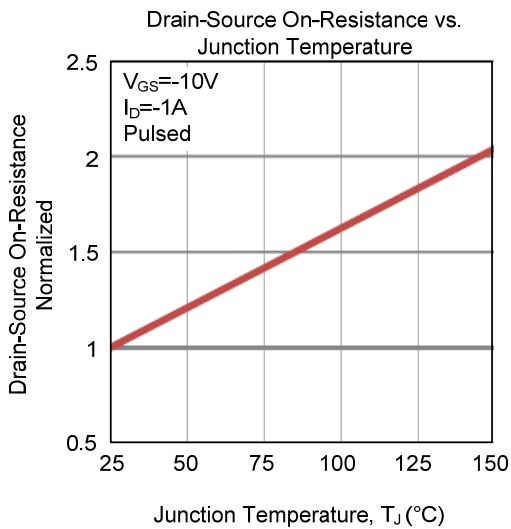
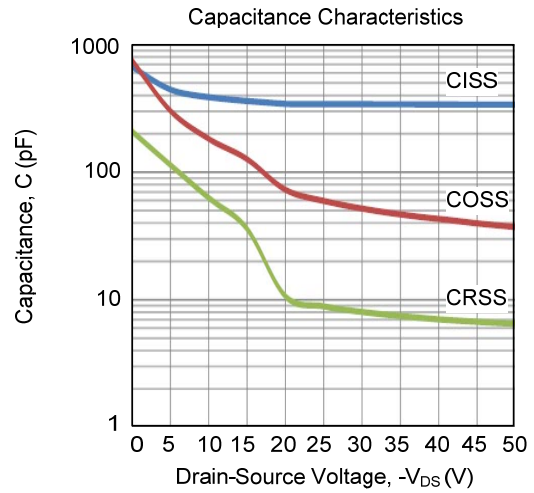
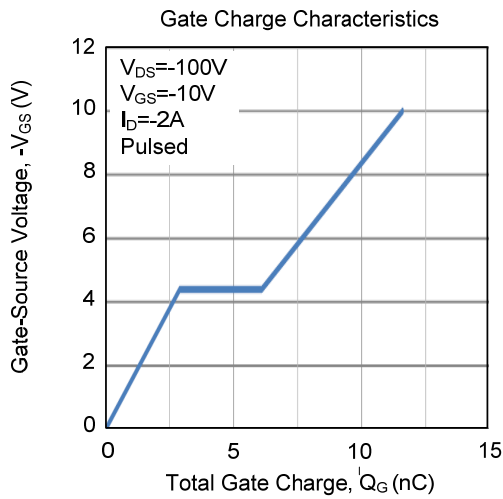
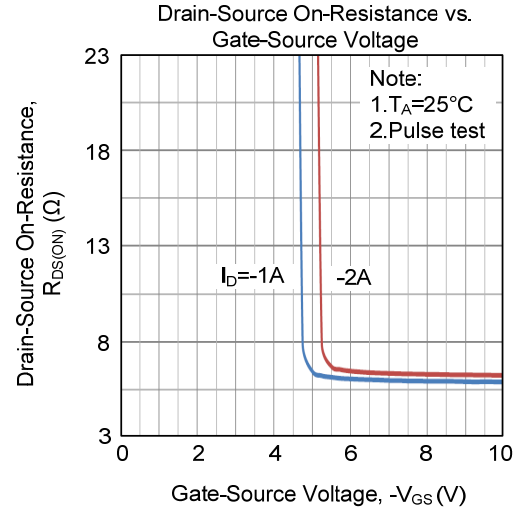
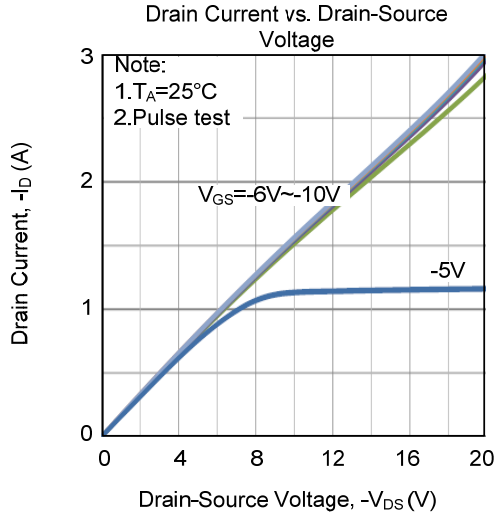


Unclamped Inductive Switching Test Circuit

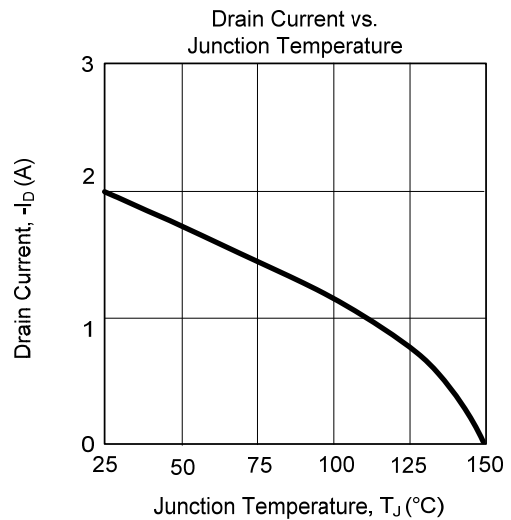
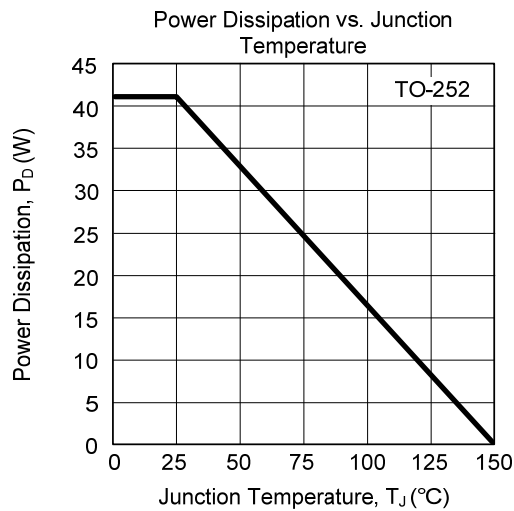
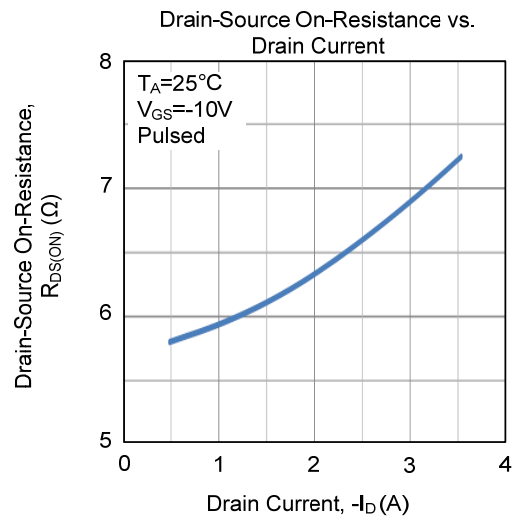
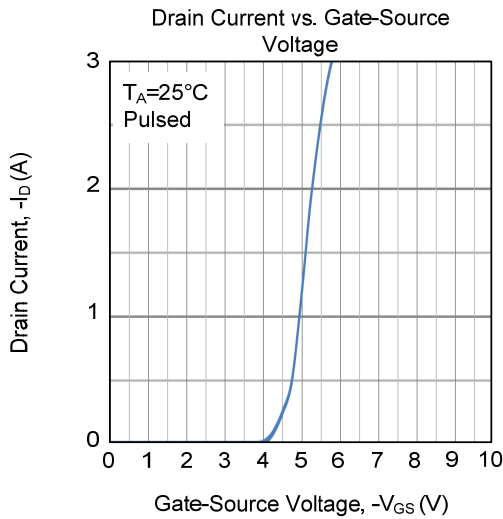
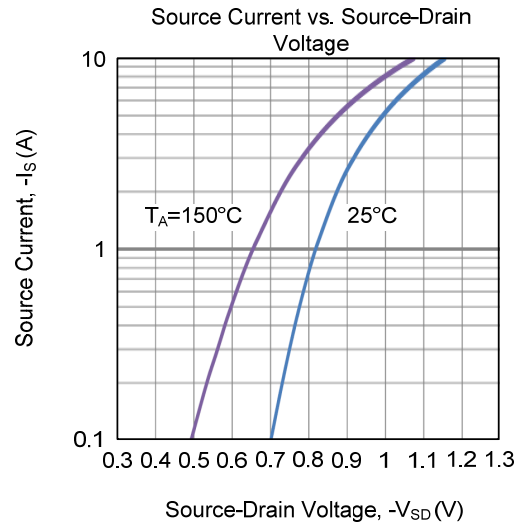
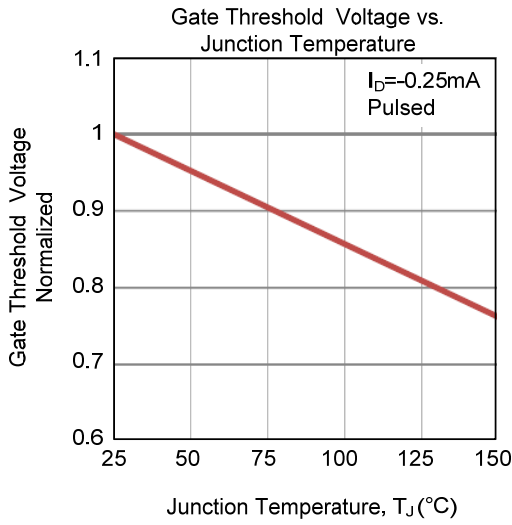


Unclamped Inductive Switching Waveforms

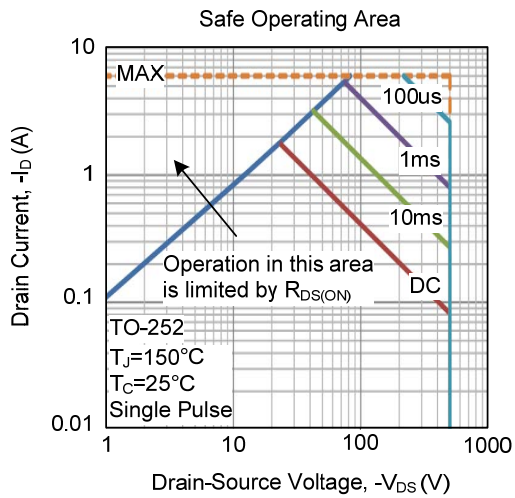
■ TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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