



UC3842A/3843A

LINEAR INTEGRATED CIRCUIT

CURRENT MODE PWM CONTROL CIRCUITS

DESCRIPTION

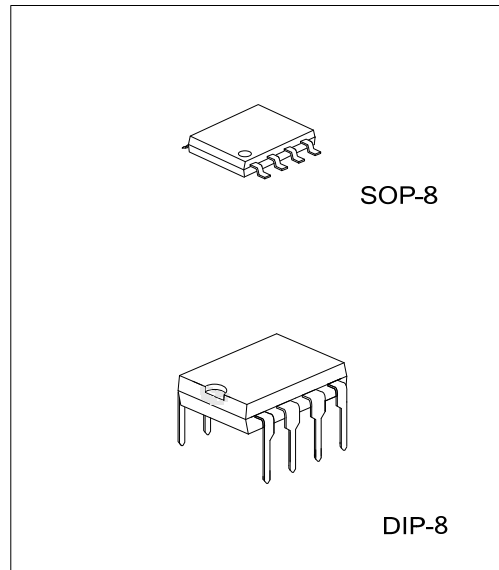
The UTC **UC3842A/3843A** provide the necessary functions to implement off-line or DC to DC fixed frequency current mode , controlled switching circuits with minimal external components.

FEATURES

- *Low Start Up Current (Typical 0.12mA)
- *Automatic Feed Forward Compensation
- *Pulse-by-Pulse Current Limiting
- *Under-voltage Lockout with Hysteresis
- *Double Pulse Suppression
- *High Current Totem Pole Output to Drive MOSFET Directly
- *Internally Trimmed Band Gap Reference
- *500kHz Operation

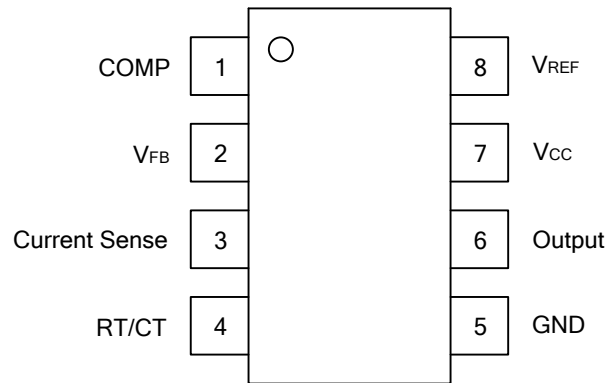
ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|-----------------|----------------|---------|-----------|
| Lead Free | Halogen Free | | |
| UC3842AL-D08-T | UC3842AP-D08-T | DIP-8 | Tube |
| UC3842AL-S08-R | UC3842AP-S08-R | SOP-8 | Tape Reel |
| UC3842AL-S08-T | UC3842AP-S08-T | SOP-8 | Tube |
| UC3843AL-D08-T | UC3843AP-D08-T | DIP-8 | Tube |
| UC3843AL-S08-R | UC3843AP-S08-R | SOP-8 | Tape Reel |
| UC3843AL-S08-T | UC3843AP-S08-T | SOP-8 | Tube |

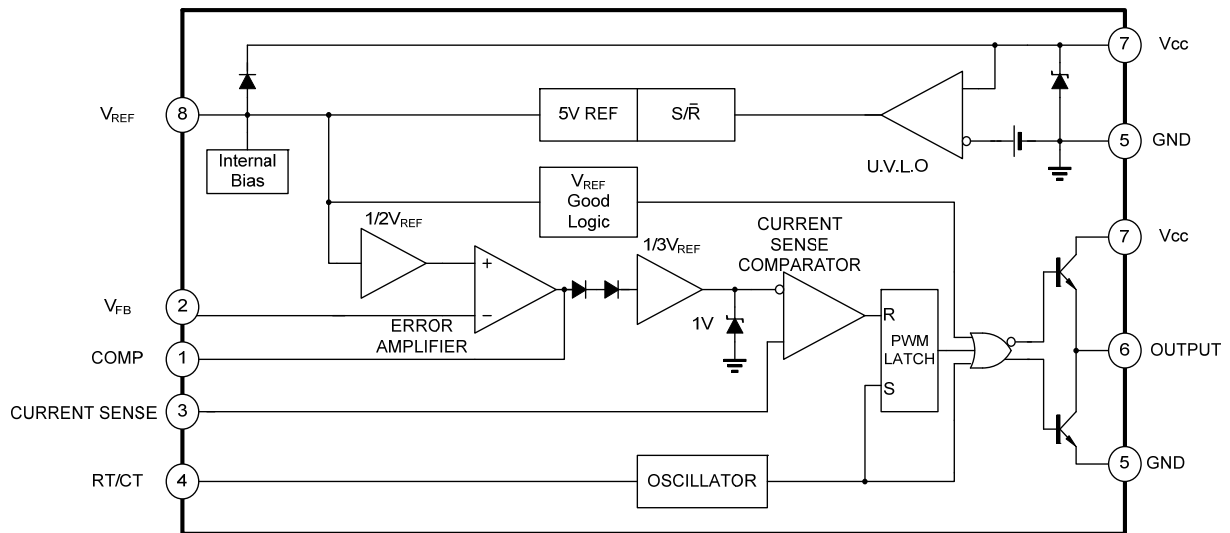


| | |
|---|---|
| <p>UC3842AL-D08-T</p> <p>(1)Packing Type (2)Package Type (3)Lead Free</p> | <p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) P: Halogen Free, L: Lead Free</p> |
|---|---|

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|--|----------------|---------------|----------------------|
| Supply Voltage(Low Impedance Source) | V_{CC} | 30 | V |
| Supply Voltage($I_{CC}<30\text{mA}$) | V_{CC} | Self Limiting | V |
| Analog Inputs (Pin 2,3) | $V_{I(ANA)}$ | -0.3 ~ +6.3 | V |
| Output Current (Peak) | $I_{O(PEAK)}$ | ± 1 | A |
| Error Amplifier Output Sink Current | $I_{SINK(EA)}$ | 10 | mA |
| Output Energy (Capacity Load) | | 5 | μJ |
| Power Dissipation($T_A \leq 25^\circ\text{C}$) | DIP-8 | 1250 | mW |
| | SOP-8 | 800 | |
| Derated at $T_A > 25^\circ\text{C}$ | | 8 | mW/ $^\circ\text{C}$ |
| Junction Temperature | T_J | +150 | $^\circ\text{C}$ |
| Storage Temperature | T_{STG} | -65 ~ +150 | $^\circ\text{C}$ |

Note Absolute maximum ratings are those values beyond which the device which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CC}=15\text{V}$, $R_T=10\text{k}\Omega$, $C_T=3.3\text{nF}$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|--------------------------|---|------|------|------|----------------------|
| REFERENCE SECTION | | | | | | |
| Output Voltage | V_{REF} | $T_J=25^\circ\text{C}, I_{OUT}=1\text{mA}$ | 4.9 | 5 | 5.1 | V |
| Line Regulation | ΔV_{REF} | $12 \leq V_{IN} \leq 25\text{V}$ | | 6 | 20 | mV |
| Load Regulation | ΔV_{REF} | $1 \leq I_{OUT} \leq 20\text{mA}$ | | 6 | 25 | mV |
| Temperature Stability | | (Note 1) | | 0.2 | 0.4 | mV/ $^\circ\text{C}$ |
| Total Output Variation | | Line, Load, Temp (Note 1) | 4.82 | | 5.18 | V |
| Output Noise Voltage | V_{OSC} | $10\text{Hz} \leq f \leq 10\text{kHz}, T_J=25^\circ\text{C}$ (Note 1) | | 50 | | μV |
| Long Term Stability | | $T_A=25^\circ\text{C}, 1000\text{Hrs}$ (Note 1) | | 5 | 25 | mV |
| Output Short Circuit | I_{SC} | | -30 | -100 | -180 | mA |
| OSCILLATOR SECTION | | | | | | |
| Initial Accuracy | f | $T_J=25^\circ\text{C}$ | 47 | 52 | 57 | kHz |
| Voltage Stability | $\Delta f/\Delta V_{CC}$ | $12 \leq V_{CC} \leq 25\text{V}$ | | 0.2 | 1 | % |
| Temperature Stability | | $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 1) | | 5 | | % |
| Amplitude | V_{OSC} | V_{PIN4} peak to peak | | 1.7 | | V |
| ERROR AMPLIFIER SECTION | | | | | | |
| Input Voltage | $V_{I(EA)}$ | $V_{PIN1}=2.5\text{V}$ | 2.42 | 2.50 | 2.58 | V |
| Input Bias Current | $I_{I(BIAS)}$ | | | -0.3 | -2 | μA |
| AVOL | | $2\text{V} \leq V_{OUT} \leq 4\text{V}$ | 60 | 90 | | dB |
| Unity Gain Bandwidth | | $T_J=25^\circ\text{C}$ (Note 1) | 0.7 | 1 | | MHz |
| PSRR | | $I_2 \leq V_{CC} \leq 25\text{V}$ | 60 | 70 | | dB |
| Output Sink Current | $I_{O(SINK)}$ | $V_{PIN2}=2.7\text{V}, V_{PIN1}=1.1\text{V}$ | 2 | 6 | | mA |
| Output Source Current | $I_{O(SOURCE)}$ | $V_{PIN2}=2.3\text{V}, V_{PIN1}=5\text{V}$ | -0.5 | -0.8 | | mA |
| V_{OUT} High | V_{OH} | $V_{PIN2}=2.3\text{V}, R_L=15\text{k}\Omega$ to GND | 5 | 6 | | V |
| V_{OUT} Low | V_{OL} | $V_{PIN2}=2.7\text{V}, V_{PIN1}=1.1\text{V}$ | | 0.7 | 1.1 | V |

■ ELECTRICAL CHARACTERISTICS(Cont.)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|---------------|------------------------------------|-----------------------|------|------|---------|---|
| CURRENT SENSE SECTION | | | | | | | |
| Gain | G_V | (Note 2, 3) | 2.85 | 3 | 3.15 | V/V | |
| Maximum Input signal | $V_{I(MAX)}$ | $V_{PIN1}=5V$ (Note 2) | 0.9 | 1 | 1.1 | V | |
| PSRR | | $12V \leq V_{CC} \leq 25V$ | | 70 | | dB | |
| Input Bias Current | I_{BIAS} | | | -2 | -10 | μA | |
| Delay to Output | | $V_{PIN3}=0$ to 2V | | 150 | 300 | ns | |
| OUTPUT SECTION | | | | | | | |
| Output Level | Low | V_{OL} | $I_{O(SINK)}=20mA$ | | 0.1 | 0.4 | V |
| | | | $I_{O(SINK)}=200mA$ | | 1.5 | 2.2 | V |
| | High | V_{OH} | $I_{O(SOURCE)}=20mA$ | 13 | 13.5 | | V |
| | | | $I_{O(SOURCE)}=200mA$ | 12 | 13.5 | | V |
| Rise Time | t_R | $T_J=25^\circ C, C_L=1nF$ (Note 1) | | 50 | 150 | ns | |
| Fall Time | t_F | $T_J=25^\circ C, C_L=1nF$ (Note 1) | | 50 | 150 | ns | |
| UNDER-VOLTAGE LOCKOUT OUTPUT SECTION | | | | | | | |
| Start Threshold | 3842A | $V_{TH(ST)}$ | | 14.5 | 16 | 17.5 | V |
| | 3843A | | | 7.8 | 8.4 | 9 | V |
| Min. Operating Voltage | 3842A | $V_{OPR(MIN)}$ | After Turn On | 8.5 | 10 | 11.5 | V |
| | 3843A | | | 7 | 7.6 | 8.2 | V |
| PWM SECTION | | | | | | | |
| Duty Cycle | MAX | $D_{(MAX)}$ | | 95 | 97 | 100 | % |
| | MIN | $D_{(MIN)}$ | | | | 0 | % |
| TOTAL STANDBY CURRENT | | | | | | | |
| Start-up Current | I_{ST} | | | 0.12 | 0.3 | mA | |
| Operating Supply Current | $I_{CC(OPR)}$ | $V_{PIN2}=V_{PIN3}=0V$ | | 11 | 17 | mA | |
| V_{CC} Zener Voltage | V_Z | $I_{CC}=25mA$ | | 34 | | V | |

Note:1. These parameters, although guaranteed, are not 100% tested in production.

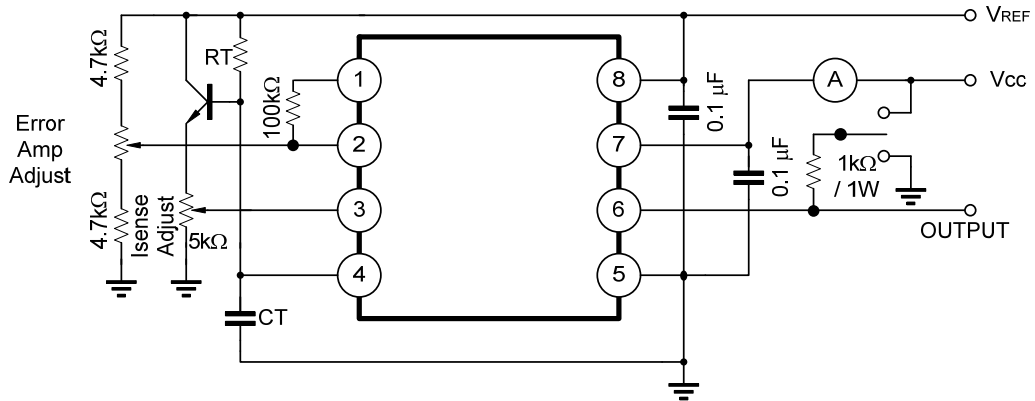
2. Parameters measured at trip point of latch with $V_{PIN2}=0$.

3. Gain defined as:

$$A = \frac{V_{PIN1}}{V_{PIN3}} ; 0 \leq V_{PIN3} \leq 0.8V$$

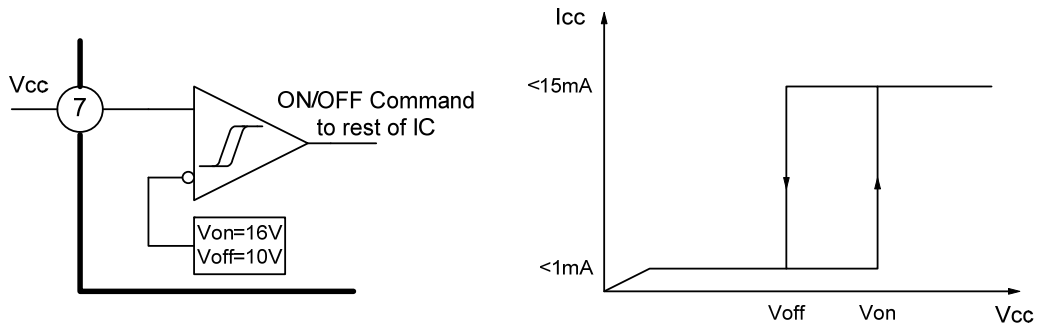
4. Adjust V_{CC} above the start threshold before setting at 15V.

■ OPEN-LOOP LABORATORY TEST FIXTURE



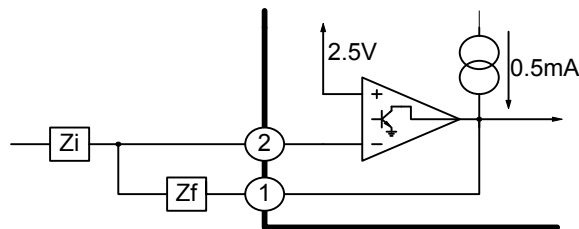
High peak current associated with capacity loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to Pin 5 in single point GND. The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable Ramp to Pin 3.

■ UNDER-VOLTAGE LOCKOUT



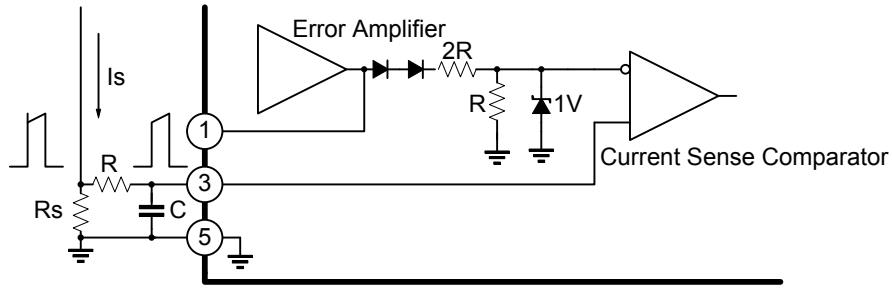
During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin 6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

■ ERROR AMPLIFIER CONFIGURATION



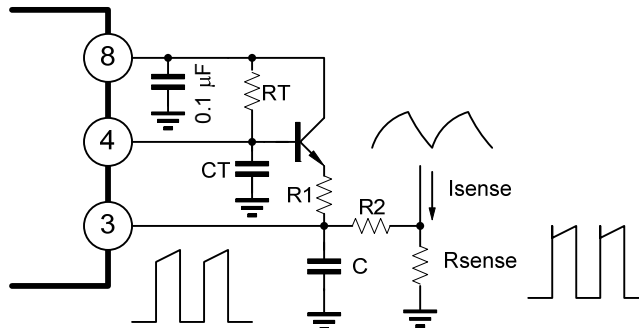
Error amplifier can source or sink up to 0.5mA

■ CURRENT SENSE CIRCUIT



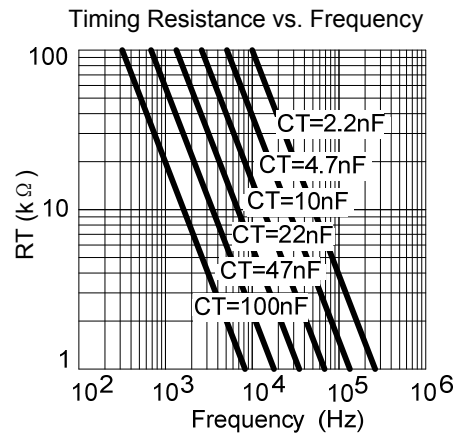
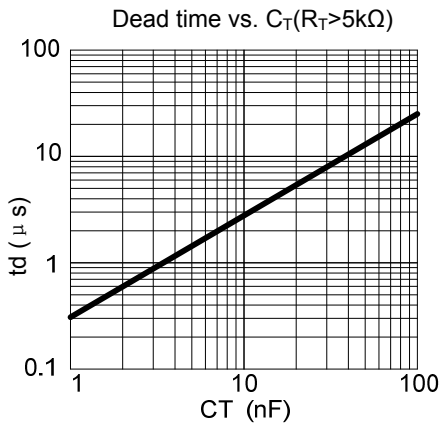
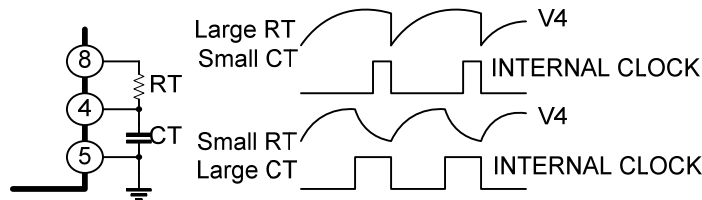
Peak current (I_s) determined by the formula: $I_{S_{MAX}} = 1.0V/R_s$.
 A small RC filter be required to suppress switch transients.

■ SLOPE COMPENSATION

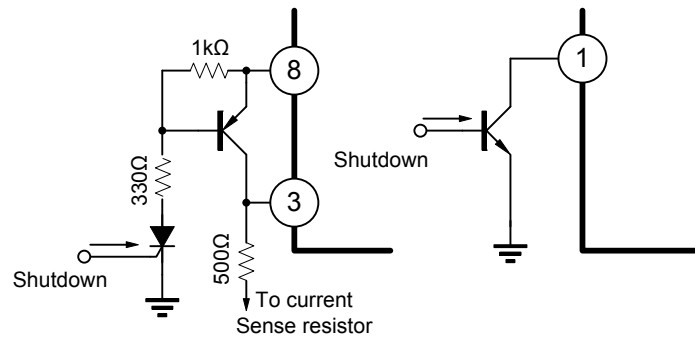


A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over 50%. Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.

■ OSCILLATOR SECTION

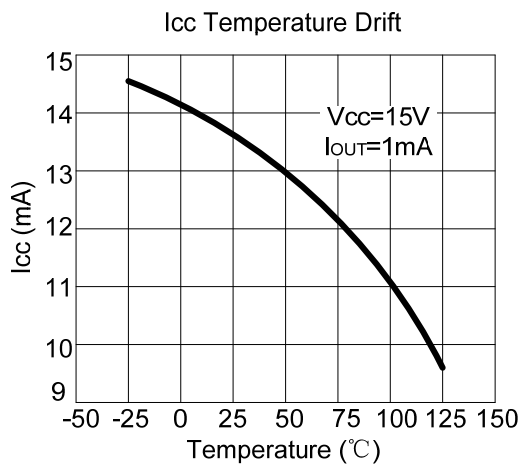
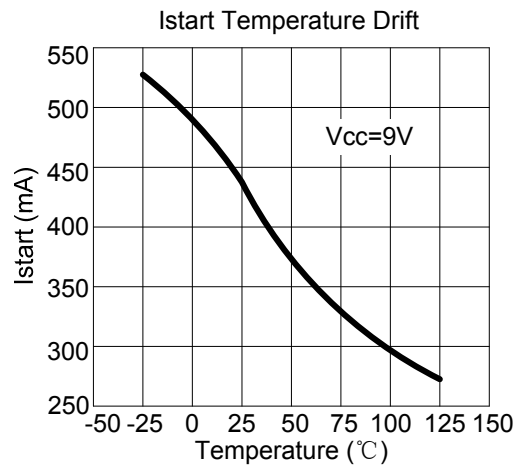
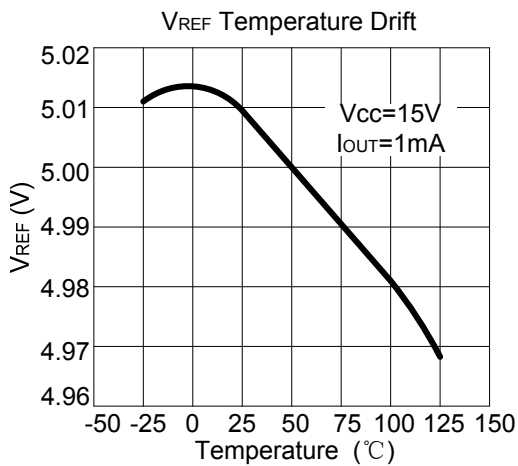
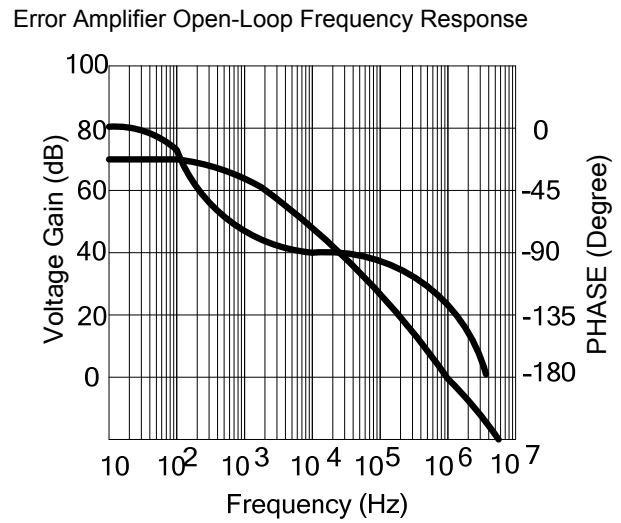
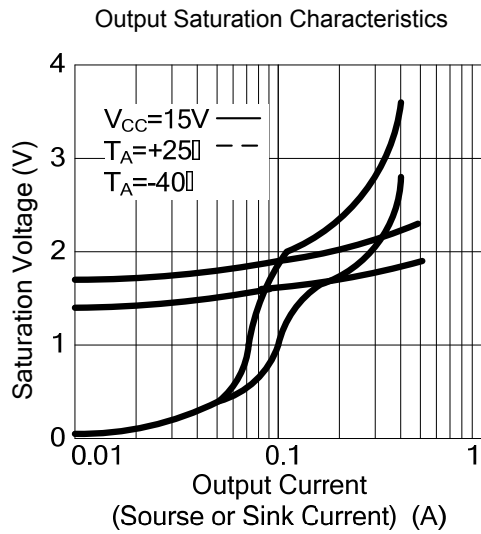


■ SHUTDOWN TECHNIQUES



Shutdown UTC **UC3842A** can be accomplished by two methods; either raise Pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method caused the output of PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at Pins 1 and/or 3 is removed. In one example, an externally latched shut-down may be accomplished by adding an SCR which is reset by cycling V_{CC} below the lower UVLO threshold. At this point the reference turns off allowing the SCR to reset.

■ TYPICAL CHARACTERISTICS



UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.

单击下面可查看定价，库存，交付和生命周期等信息

[>>UTC\(友顺\)](#)