



UC1844/45

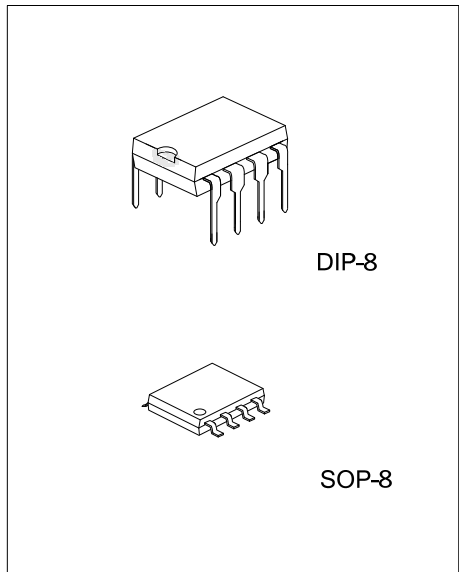
LINEAR INTEGRATED CIRCUIT

HIGH PERFORMANCE CURRENT MODE PWM CONTROLLERS

DESCRIPTION

The UTC **UC1844/1845** are high performance fixed frequency current mode controllers that specifically designed for Off-Line and DC to DC converter applications with minimal external parts count.

The differences between **UC1844** and **UC1845** are the under-voltage lockout thresholds. The **UC1844** ideally suited to off-line applications with UVLO thresholds of 16V_(ON) and 10V_(OFF), and **UC1845** has UVLO thresholds of 8.4V_(ON) and 7.6V_(OFF) for lower voltage applications.



FEATURES

- * Operation output switching frequency up to 500 kHz
- * Automatic feed forward compensation
- * Latching PWM for cycle-by-cycle current limiting
- * High current totem pole output
- * Internally trimmed reference with under voltage lockout
- * UVLO with hysteresis
- * Low startup and operating current

ORDERING INFORMATION

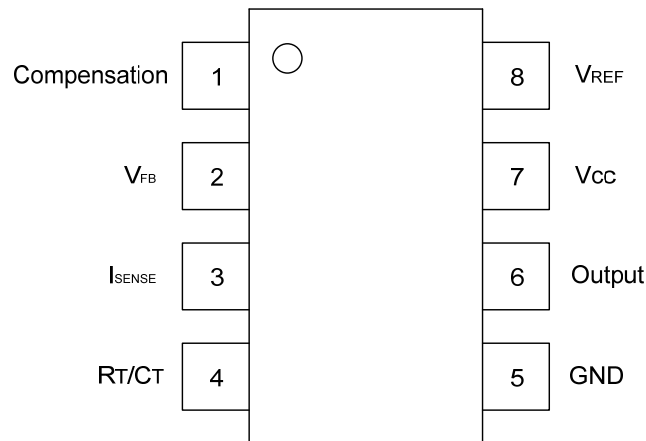
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC1844L-D08-T	UC1844G-D08-T	DIP-8	Tube
UC1844L-S08-R	UC1844G-S08-R	SOP-8	Tape Reel
UC1845L-D08-T	UC1845G-D08-T	DIP-8	Tube
UC1845L-S08-R	UC1845G-S08-R	SOP-8	Tape Reel

<p>UC1844G-D08-T</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

PACKAGE	UC1844	UC1845
DIP-8		
SOP-8		

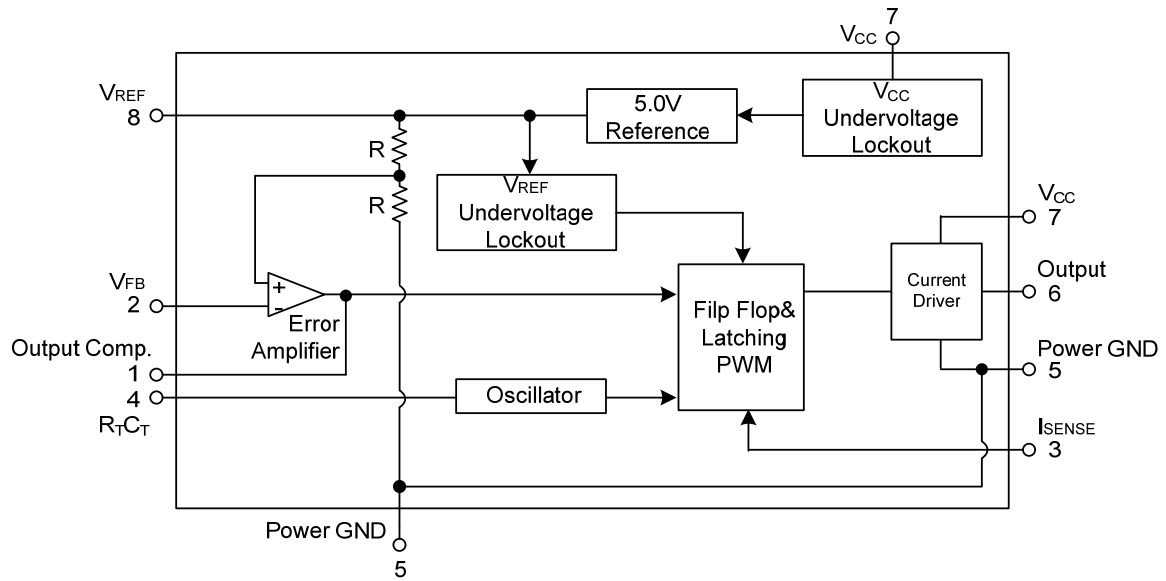
PIN CONFIGURATION



PIN DESCRIPTION

PIN NO	PIN NAME	FUNCTION
1	Compensation	Error amplifier output, this pin is made available for loop compensation.
2	V_{FB}	Voltage Feedback, the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The Oscillator frequency and maximum output duty cycle are programmed by connecting resistor R_T to V_{REF} and capacitor C_T to ground. Operation to 1 MHz is possible.
5	GND	Power ground.
6	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency.
7	V_{CC}	Positive supply.
8	V_{REF}	Reference output, provides charging current for capacitor C_T through resistor R_T .

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Current Sense and Voltage feedback Inputs	V_{IN}	-0.3 ~ +5.5	V
Supply Voltage (Low Impedance Source)	V_{CC}	30	V
Supply Voltage ($I_{CC}<30\text{mA}$)	V_{CC}	Self Limiting	V
Error Amp Output Sink Current	I_{SINK}	10	mA
Output Current, Source or Sink (Note 2)	I_{OUT}	1.0	A
Output Energy (Capacitive Load per cycle)	W	5.0	μJ
Power Dissipation	DIP-8	P_D	1250
	SOP-8		800
Junction Temperature	T_J	+150	$^\circ\text{C}$
Operation Temperature	T_{OPR}	-40 ~ +125	$^\circ\text{C}$
Storage Temperature	T_{STG}	-65 ~ +150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Maximum package power dissipation limits must be observed.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-8	θ_{JA}	100
	SOP-8		156

■ ELECTRICAL CHARACTERISTICS

($T_A=25^\circ\text{C}$, $V_{CC}=15\text{V}$, $R_T=10\text{k}$, $C_T=3.3\text{nF}$, $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE SECTION						
Reference Output Voltage	V_{REF}	$I_{OUT}=1.0\text{mA}$, $T_J=25^\circ\text{C}$	4.9	5.0	5.1	V
Line Regulation	ΔV_{OUT}	$V_{CC}=12\text{V} \sim 25\text{V}$		2.0	20	mV
Load Regulation	ΔV_{OUT}	$I_{OUT}=1.0\text{mA} \sim 20\text{mA}$		15	30	mV
Temperature Stability	t_s			0.2		$\text{mV}/^\circ\text{C}$
Total Output Variation over Line, Load, Temperature	V_{REF}		4.82		5.18	V
Output Noise Voltage	e_N	$f=10\text{Hz} \sim \text{kHz}$, $T_J=25^\circ\text{C}$		50		μV
Long Term Stability	S	$T_A=125^\circ\text{C}$ for 1000 Hours		5		mV
Output Short Circuit Current	I_{SC}		-50	-155	-280	mA
OSCILLATOR SECTION						
Oscillator Voltage Swing	V_{OSC}			1.6		V
Discharge Current	I_{DSG}	$V_{OSC}=2.0\text{V}$, $T_J=25^\circ\text{C}$		10.8		mA
Frequency	f_{OSC}	$T_J=25^\circ\text{C}$	47	52	57	kHz
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	46		60	
Frequency Change with Voltage	$\Delta f_{OSC}/\Delta V$	$V_{CC}=12\text{V} \sim 25\text{V}$		0.2	1.0	%
Frequency Change with Temperature	$\Delta f_{OSC}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		5.0		%
ERROR AMPLIFIER SECTION						
Voltage Feedback Input	V_{FB}	$V_{OUT}=2.5\text{V}$	2.42	2.50	2.58	V
Output Voltage Swing	High	V_{OH}	$R_L=15\text{k}$ to ground, $V_{FB}=2.3\text{V}$	5.0	6.2	V
	Low	V_{OL}	$R_L=15\text{k}$ to V_{REF} , $V_{FB}=2.7\text{V}$		0.8	
Output Current	Sink	I_{SINK}	$V_{OUT}=1.6\text{V}$, $V_{FB}=2.7\text{V}$	2.0	12	mA
	Source	I_{SOURCE}	$V_{OUT}=5.0\text{V}$, $V_{FB}=2.3\text{V}$	-0.5	-1.0	
Input Bias Current	$I_{(BIAS)}$	$V_{FB}=2.7\text{V}$		-0.1	-2.0	μA
Open Loop Voltage Gain	G_{VO}	$V_{OUT}=2.0\text{V} \sim 4.0\text{V}$	65	90		dB
Power Supply Rejection Ratio	PSRR	$V_{CC}=12\text{V} \sim 25\text{V}$	60	70		dB
Unity Gain Bandwidth	GB_W	$T_J=25^\circ\text{C}$	0.7	1.0		MHz

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
CURRENT SENSE SECTION							
Current Sense Input Voltage Gain (Note 2, 3)	G_V		2.85	3.0	3.15	V/V	
Maximum Current Sense Input Threshold (Note 2)	$V_{I(THR)}$		0.9	1.0	1.1	V	
Input Bias Current	$I_{I(BIAS)}$			-2.0	-10	μA	
Power Supply Rejection Ratio	PSRR	$V_{CC}=12V \sim 25V$ (Note 4)		70		dB	
Propagation Delay	$t_{PLH(IN/OUT)}$			150	300	ns	
OUTPUT SECTION							
Output Voltage	Low	V_{OL}	$I_{SINK}=20mA$		0.2	0.8	V
			$I_{SINK}=200mA$		1.6	2.2	V
	High	V_{OH}	$I_{SINK}=20mA$	11	13.5		V
			$I_{SINK}=200mA$	11	13.4		V
Output Voltage with U_{VLO} Activated	$V_{OL(UVLO)}$	$V_{CC}=6.0V, I_{SINK}=1.0mA$		0.7	1.2	V	
Output Voltage Rise Time	t_R	$C_L=1.0nF, T_J=25^\circ C$		50	150	ns	
Output Voltage Fall Time	t_F	$C_L=1.0nF, T_J=25^\circ C$		50	150	ns	
UNDERVOLTAGE LOCKOUT SECTION							
Startup Threshold	UC1844	V_{THR}		14.5	16.0	17.5	V
	UC1845			7.8	8.4	9.0	V
Minimum Operating Voltage After Turn-On	UC1844	$V_{CC(MIN)}$		8.5	10.0	11.5	V
	UC1845			7.0	7.6	8.2	V
PWM SECTION							
Duty Cycle	MAX	DC_{MAX}		47	48	50	%
	MIN	DC_{MIN}				0	%
TOTAL DEVICE							
Power Supply Zener Voltage	V_Z	$I_{CC}=25mA$	30	34		V	
Power Supply Current (Note 4)	I_{CC}	Start Up		0.25	0.5	mA	
		Operating		12	17	mA	

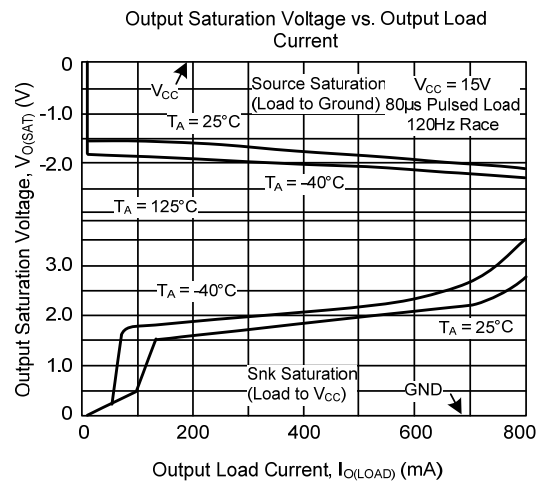
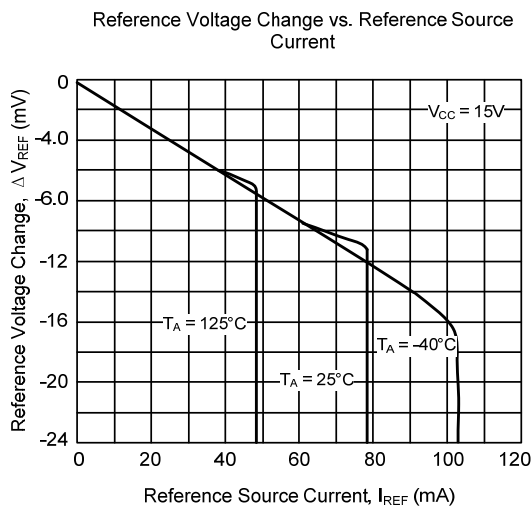
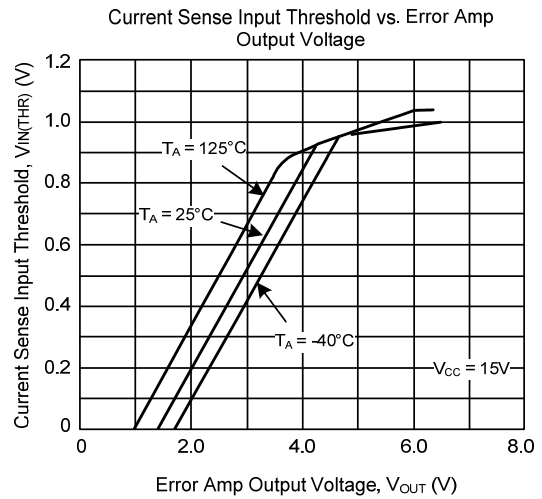
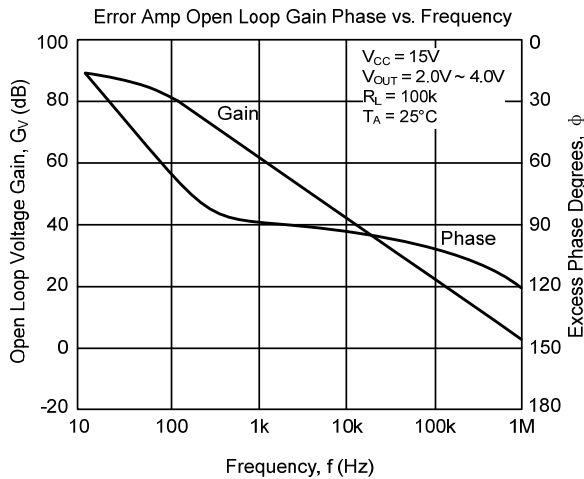
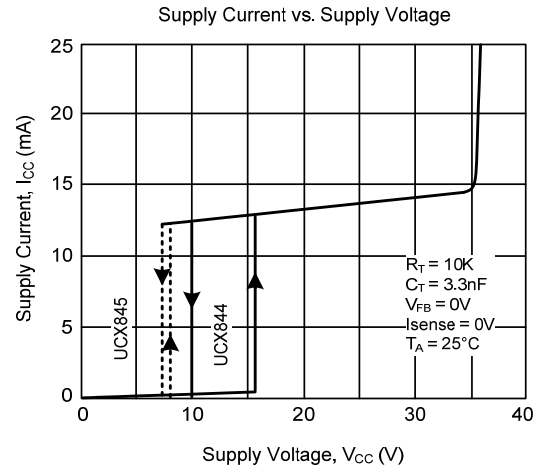
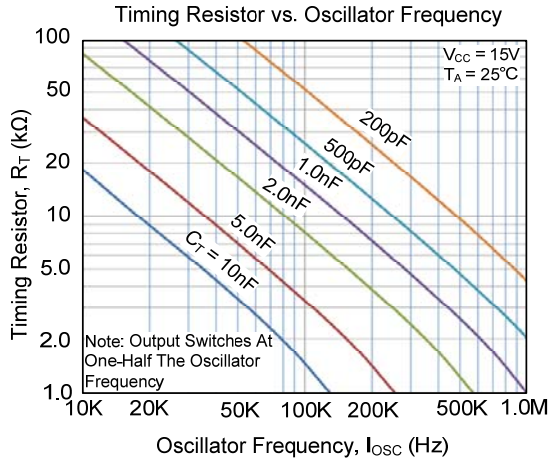
Notes: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

2. This parameter is measured at the latch trip point with $V_{FB}=0V$.

3. Comparator gain is defined as: $A_V = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

4. Adjust V_{CC} above the startup threshold before setting to 15V.

TYPICAL CHARACTERISTICS



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