



U74AUP1G57

CMOS IC

LOW-POWER CONFIGURABLE MULTIPLE-FUNCTION GATE

DESCRIPTION

The **U74AUP1G57** device features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions AND, OR, NAND, NOR, XNOR, inverter, and noninverter. All inputs can be connected to V_{CC} or GND.

This part can be used in any application where an equivalent single gate would work. The biggest benefit to this part is that it can be used for multiple functions on the same board, reducing the total number of part numbers to be used.

FEATURES

- * Single-Supply Voltage Translator
- * Low power dissipation
- * Wide supply voltage range from 0.8V to 3.6V
- * Inputs accept voltages up to 3.6V
- * I_{OFF} supports partial-power-down mode
- * Optimized for 3.3V Operation

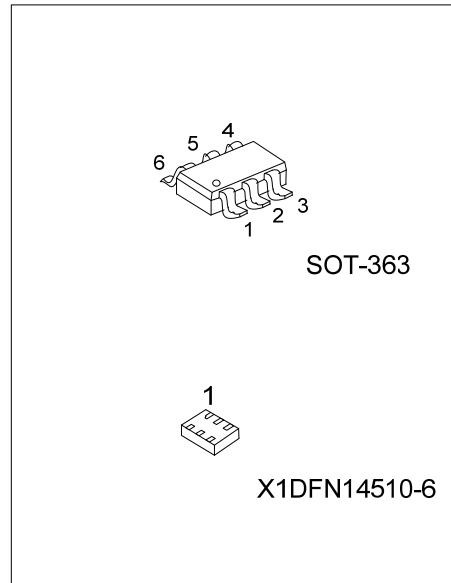
ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AUP1G57L-AL6-R	U74AUP1G57G-AL6-R	SOT-363	Tape Reel
U74AUP1G57L-KAP-R	U74AUP1G57G-KAP-R	X1DFN14510-6	Tape Reel

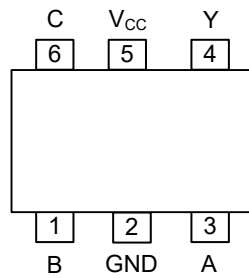
<p>U74AUP1G57G-AL6-R</p> <p>(1)Packing Type (2)Package Type (3)Green Package</p>	<p>(1) R: Tape Reel (2) AL6: SOT-363, KAP: X1DFN14510-6 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

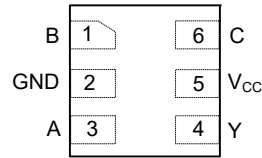
SOT-363	X1DFN14510-6



■ PIN CONFIGURATION



SOT-23-5 / SOT-353



X1DFN14510-6
(TOP VIEW)

■ PIN DESCRIPTION

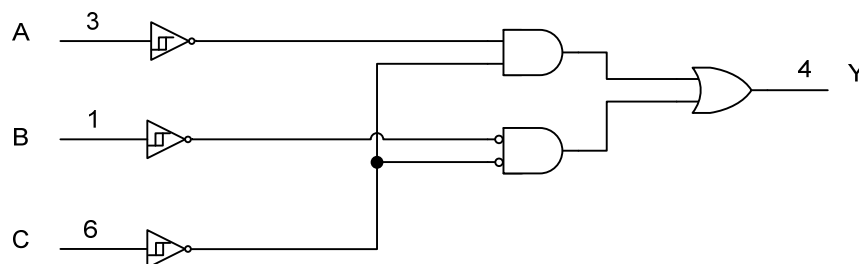
PIN NO.		PIN NAME	I/O	DESCRIPTION
SOT-23-5 SOT-353	X1DFN14510-6			
1	1	B	I	Logic Input 1
2	2	GND	-	Ground
3	3	A	I	Logic Input 0
4	4	Y	O	Logic output
5	5	V _{cc}	-	Power
6	6	C	I	Logic Input 2

■ FUNCTION TABLE

INPUT			OUTPUT
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Note: H: High voltage level; L: Low voltage level.

■ LOGIC DIAGRAM (positive logic)



■ FUNCTION SELECTION TABLE

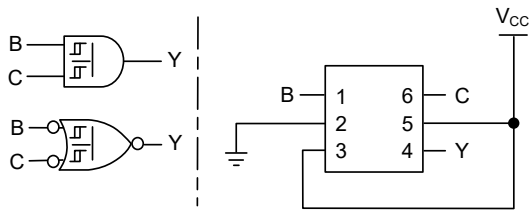


Figure 1. 2-Input AND Gate or 2-Input NOR Gate With Both Inputs Inverted

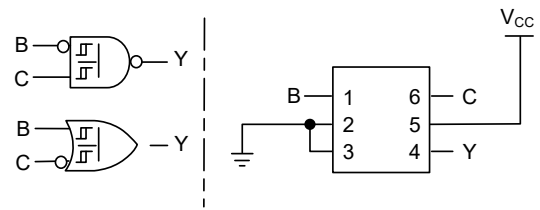


Figure 2. 2-Input NAND Gate With Inverted B Input or 2-Input OR Gate With Inverted C Input

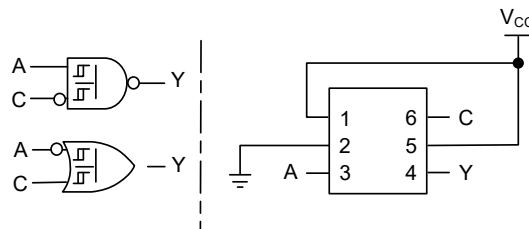


Figure 3. 2-Input NAND Gate With Inverted C Input or 2-Input OR Gate With Inverted A Input

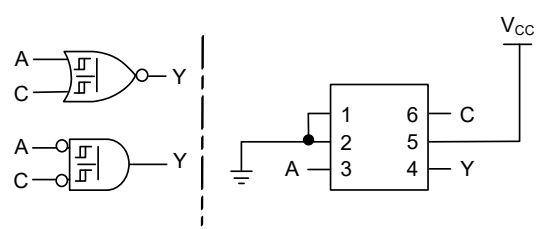


Figure 4. 2-Input NOR Gate or 2-Input AND Gate With Both Inputs Inverted

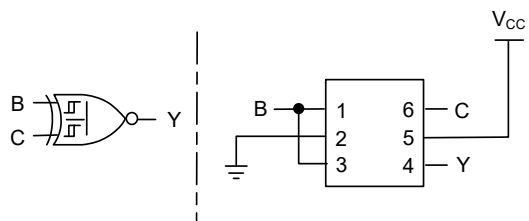


Figure 5. 2-Input XNOR Gate

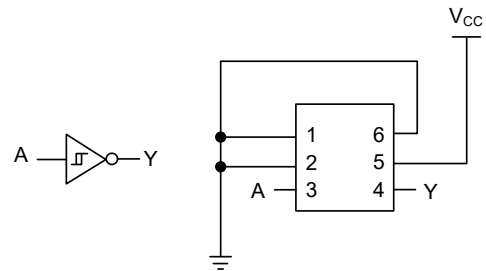


Figure 6. Inverter

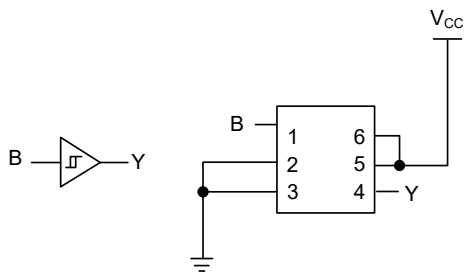


Figure 7. Buffer

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ +4.6	V
Input Voltage	V _{IN}		-0.5 ~ +4.6	V
Output Voltage	V _{OUT}	Output in the power-off state	-0.5 ~ +4.6	V
		Output in the high or low state	-0.5 ~ V _{CC} +0.5	V
Continuous V _{CC} or GND Current	I _{CC}		±50	mA
Continuous Output Current	I _{OUT}		±20	mA
Input Clamp Current	I _{IK}	V _{IN} <0V	-50	mA
Output Clamp Current	I _{OK}	V _{OUT} <0V	-50	mA
Storage Temperature Range	T _{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		0.8		3.6	V
Input Voltage	V _{IN}		0		3.6	V
Output Voltage	V _{OUT}		0		V _{CC}	V
Operating Temperature	T _A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Positive-Going Input Threshold Voltage	V _{T+}	V _{CC} =0.8V	0.3		0.6	V	
		V _{CC} =1.1V	0.53		0.9	V	
		V _{CC} =1.4V	0.74		1.11	V	
		V _{CC} =1.65V	0.91		1.29	V	
		V _{CC} =2.3V	1.37		1.77	V	
		V _{CC} =3.0V	1.88		2.29	V	
Negative-Going Input Threshold Voltage	V _{T-}	V _{CC} =0.8V	0.1		0.6	V	
		V _{CC} =1.1V	0.26		0.65	V	
		V _{CC} =1.4V	0.39		0.75	V	
		V _{CC} =1.65V	0.47		0.84	V	
		V _{CC} =2.3V	0.69		1.04	V	
		V _{CC} =3.0V	0.88		1.24	V	
Hysteresis Voltage (V _{T+} -V _{T-})	ΔV _T	V _{CC} =0.8V	0.07		0.5	V	
		V _{CC} =1.1V	0.08		0.46	V	
		V _{CC} =1.4V	0.18		0.56	V	
		V _{CC} =1.65V	0.27		0.66	V	
		V _{CC} =2.3V	0.53		0.92	V	
		V _{CC} =3.0V	0.79		1.31	V	
High-Level Output Voltage	V _{OH}	V _{CC} =0.8~3.6V, I _{OH} =-20μA	V _{CC} -0.1			V	
		V _{CC} =1.1V, I _{OH} =-1.1mA	0.75×V _{CC}			V	
		V _{CC} =1.4V, I _{OH} =-1.7mA	1.11			V	
		V _{CC} =1.65V, I _{OH} =-1.9mA	1.32			V	
		V _{CC} =2.3V	I _{OH} =-2.3mA	2.05			V
			I _{OH} =-3.1mA	1.9			V
		V _{CC} =3.0V	I _{OH} =-2.7mA	2.72			V
			I _{OH} =-4mA	2.6			V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Low-Level Output Voltage	V_{OL}	$V_{CC}=0.8\sim 3.6V, I_{OL}=20\mu A$			0.1	V	
		$V_{CC}=1.1V, I_{OL}=1.1mA$			$0.3\times V_{CC}$	V	
		$V_{CC}=1.4V, I_{OL}=1.7mA$			0.31	V	
		$V_{CC}=1.65V, I_{OL}=1.9mA$			0.31	V	
		$V_{CC}=2.3V$	$I_{OL}=2.3mA$			0.31	V
			$I_{OL}=3.1mA$			0.44	V
		$V_{CC}=3.0V$	$I_{OL}=2.7mA$			0.31	V
$I_{OL}=4mA$				0.44	V		
Input Leakage Current (All Inputs)	$I_{I(LEAK)}$	$V_{CC}=0\sim 3.6V, V_{IN}=GND\sim 3.6V$			± 0.1	μA	
Power OFF Leakage Current	I_{off}	$V_{CC}=0V, V_{IN}$ or $V_{OUT}=GND\sim 3.6V$			± 0.2	μA	
Quiescent Supply Current	I_{CC}	$V_{CC}=0.8\sim 3.6V, V_{IN}=GND$ or $(V_{CC}\sim 3.6V), I_{OUT}=0A$			0.5	μA	
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=3.3V, V_{IN}=V_{CC}-0.6V$ (Note.) $I_{OUT}=0A$			40	μA	
Input Capacitance	C_I	$V_{CC}=0V$ or $3.6V, V_{IN}=V_{CC}$ or GND		1.5		pF	
Output Capacitance	C_O	$V_{CC}=0V, V_{OUT}=GND$		3.0		pF	

Note: One input at $V_{CC} - 0.6V$, other inputs at V_{CC} or GND .

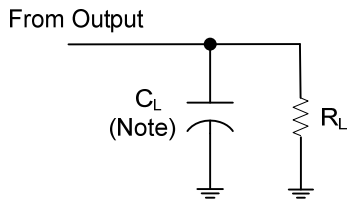
■ SWITCHING CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Propagation delay from input (A, B or C) to output(Y)	t_{PD}	$C_L=5pF, R_L=1M\Omega$	$V_{CC}=0.8V$		29.1		ns	
			$V_{CC}=1.2V\pm 0.1V$	2.6	10.1	13.6	ns	
			$V_{CC}=1.5V\pm 0.1V$	1.9	6.9	9.1	ns	
			$V_{CC}=1.8V\pm 0.15V$	1.4	5.7	7.1	ns	
			$V_{CC}=2.5V\pm 0.2V$	1.1	4.1	5.3	ns	
			$V_{CC}=3.3V\pm 0.3V$	1.0	3.4	4.4	ns	
		$C_L=10pF, R_L=1M\Omega$	$V_{CC}=0.8V$			33.3		ns
			$V_{CC}=1.2V\pm 0.1V$	2.6	11.5	15.1	ns	
			$V_{CC}=1.5V\pm 0.1V$	1.9	7.9	10.3	ns	
			$V_{CC}=1.8V\pm 0.15V$	1.4	6.5	8.1	ns	
			$V_{CC}=2.5V\pm 0.2V$	1.1	4.8	6.1	ns	
			$V_{CC}=3.3V\pm 0.3V$	1.0	4.0	5.1	ns	
		$C_L=15pF, R_L=1M\Omega$	$V_{CC}=0.8V$			37.5		ns
			$V_{CC}=1.2V\pm 0.1V$	3.4	12.8	16.8	ns	
			$V_{CC}=1.5V\pm 0.1V$	2.8	8.8	11.4	ns	
			$V_{CC}=1.8V\pm 0.15V$	2.6	7.2	9.0	ns	
			$V_{CC}=2.5V\pm 0.2V$	1.7	5.4	6.8	ns	
			$V_{CC}=3.3V\pm 0.3V$	1.5	4.4	5.6	ns	
		$C_L=30pF, R_L=1M\Omega$	$V_{CC}=0.8V$			49.8		ns
			$V_{CC}=1.2V\pm 0.1V$	4.6	16.2	21.4	ns	
			$V_{CC}=1.5V\pm 0.1V$	3.6	11.3	14.4	ns	
			$V_{CC}=1.8V\pm 0.15V$	3.1	9.3	11.4	ns	
			$V_{CC}=2.5V\pm 0.2V$	2.6	6.9	8.4	ns	
			$V_{CC}=3.3V\pm 0.3V$	2.3	5.8	7.0	ns	

■ OPERATING CHARACTERISTICS (f=10MHz, T_A=25°C , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C _{PD}	V _{CC} =0.8V		4.0		pF
		V _{CC} =1.2V±0.1V		4.0		pF
		V _{CC} =1.5V±0.1V		4.0		pF
		V _{CC} =1.8V±0.15V		4.0		pF
		V _{CC} =2.5V±0.2V		4.1		pF
		V _{CC} =3.3V±0.3V		4.3		pF

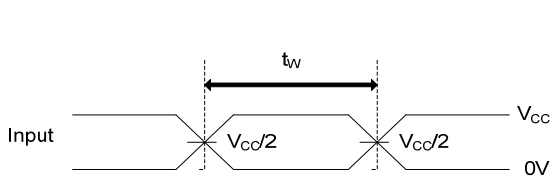
■ TEST CIRCUIT AND WAVEFORMS



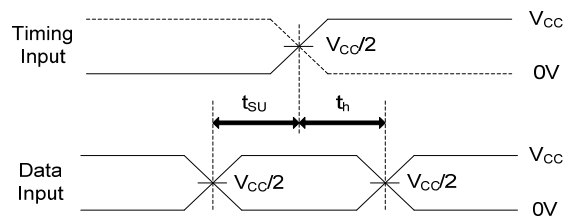
TEST CIRCUIT

Note: C_L includes probe and jig capacitance.

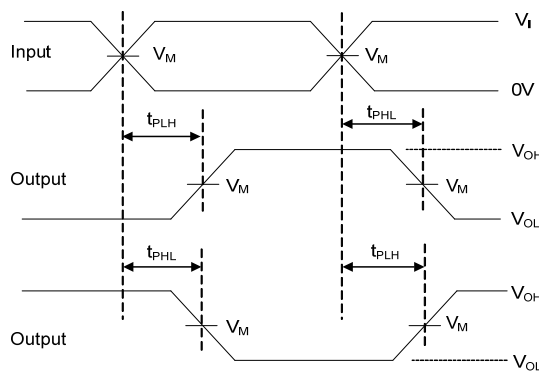
V_{CC}	C_L	V_M	V_I
0.8V	5, 10, 15, 30pF	$V_{CC}/2$	V_{CC}
1.2V±0.1V	5, 10, 15, 30pF	$V_{CC}/2$	V_{CC}
1.5V±0.1V	5, 10, 15, 30pF	$V_{CC}/2$	V_{CC}
1.8V±0.15V	5, 10, 15, 30pF	$V_{CC}/2$	V_{CC}
2.5V±0.2V	5, 10, 15, 30pF	$V_{CC}/2$	V_{CC}
3.3V±0.3V	5, 10, 15, 30pF	$V_{CC}/2$	V_{CC}



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



Voltage Waveforms Propagation Delay Times

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, $Z_o = 50\Omega$.

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