



U74HC164

CMOS IC

8-BIT SERIAL-IN AND PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The **U74HC164** is an 8-bit edge-triggered shift registers with serial input and parallel output. A LOW-to-HIGH transition on the CP will shifts the data one place to the right which is the logical AND of DSA and DSB.

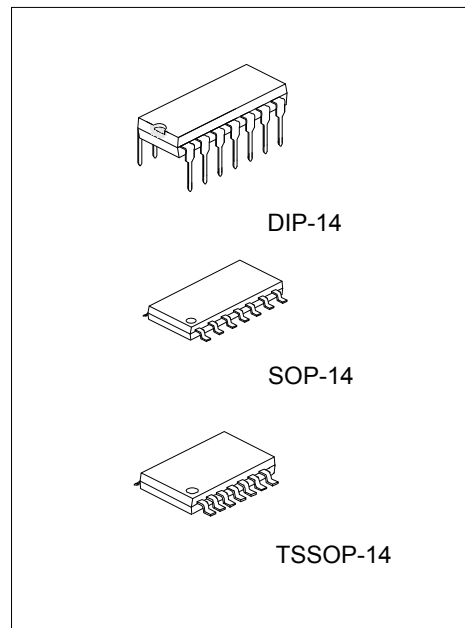
A Low level on the \overline{MR} will clear the registers asynchronously and force the outputs LOW.

FEATURES

- * Operation Voltage Range: 2~6V
- * Asynchronous Reset Input
- * Specified from -40~ +125°C

ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|-----------------|-----------------|----------|-----------|
| Lead Free | Halogen Free | | |
| U74HC164L-D14-T | U74HC164G-D14-T | DIP-14 | Tube |
| U74HC164L-S14-R | U74HC164G-S14-R | SOP-14 | Tape Reel |
| U74HC164L-P14-R | U74HC164G-P14-R | TSSOP-14 | Tape Reel |

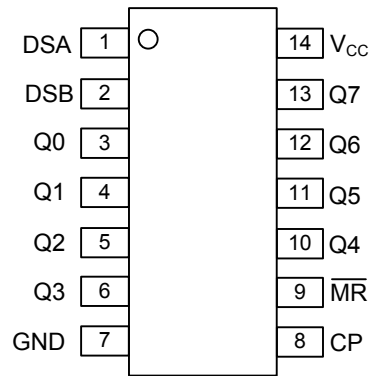


| | |
|------------------------|--|
| <p>U74HC164G-D14-T</p> | <p>(1) R: Tape Reel, T: Tube (2) D14: DIP-14, S14: SOP-14, P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free</p> |
|------------------------|--|

MARKING

| DIP-14 | SOP-14 / TSSOP-14 |
|--------|-------------------|
| | |

■ PIN CONFIGURATION

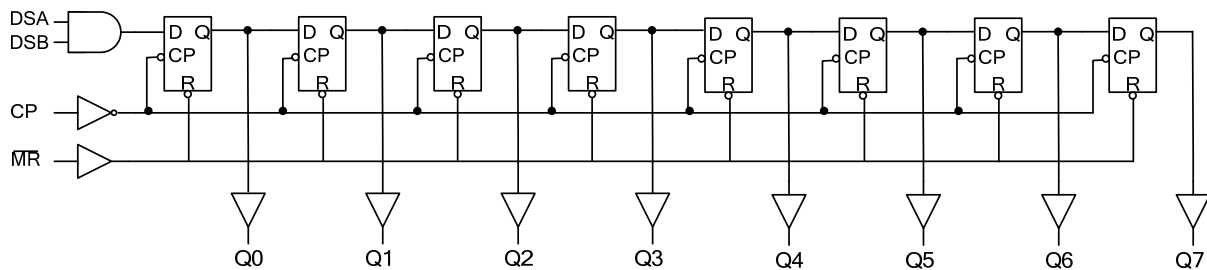


■ FUNCTION TABLE

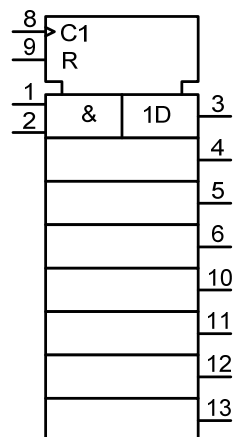
| INPUT | | | | OUTPUT | |
|-----------------|----|-----|-----|--------|----------|
| \overline{MR} | CP | DSA | DSB | Q0 | Q1 to Q7 |
| L | X | X | X | L | L to L |
| H | L | X | X | Q0 | Q1 to Q7 |
| H | ↑ | H | L | L | Q0 to Q6 |
| H | ↑ | H | H | H | Q0 to Q6 |
| H | ↑ | L | H | L | Q0 to Q6 |
| H | ↑ | L | L | L | Q0 to Q6 |

■ FUNCTIONAL DIAGRAM

Logic Diagram



IEC Logic Symbol



■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-------------------------|-----------|------------|------|
| Supply Voltage | V_{CC} | -0.5~ +7 | V |
| V_{CC} or GND Current | I_{CC} | ±50 | mA |
| Output Current | I_{OUT} | ±25 | mA |
| Input Diode Current | I_{IK} | ±20 | mA |
| Switch Diode Current | I_{OK} | ±20 | mA |
| Power Dissipation | DIP-14 | 750 | mW |
| | SOP-14 | 500 | mW |
| | TSSOP-14 | 500 | mW |
| Storage Temperature | T_{STG} | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|---------------------|---------------|-----|-----|----------|------|
| Supply Voltage | V_{CC} | | 2.0 | 5.0 | 6.0 | V |
| Input Voltage | V_{IN} | | 0 | | V_{CC} | V |
| Output Voltage | V_{OUT} | | 0 | | V_{CC} | V |
| Input Transition Rise or Fall Rate | $\Delta t/\Delta v$ | $V_{CC}=2V$ | | | 1000 | ns |
| | | $V_{CC}=4.5V$ | | 6.0 | 500 | ns |
| | | $V_{CC}=6V$ | | | 400 | ns |
| Operating Temperature | T_A | | -40 | | 125 | °C |

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------|--------------|--|------|------|------|------|
| Input Voltage High-Level | V_{IH} | $V_{CC}=2.0V$ | 1.5 | 1.2 | | V |
| | | $V_{CC}=4.5V$ | 3.15 | 2.4 | | V |
| | | $V_{CC}=6.0V$ | 4.2 | 3.2 | | V |
| Input Voltage Low-Level | V_{IL} | $V_{CC}=2.0V$ | | 0.8 | 0.5 | V |
| | | $V_{CC}=4.5V$ | | 2.1 | 1.35 | V |
| | | $V_{CC}=6.0V$ | | 2.8 | 1.8 | V |
| Output Voltage High-Level | V_{OH} | $V_{CC}=2.0V, I_{OH}=20\mu A$ | 1.9 | 2.0 | | V |
| | | $V_{CC}=4.5V, I_{OH}=20\mu A$ | 4.4 | 4.5 | | V |
| | | $V_{CC}=6.0V, I_{OH}=20\mu A$ | 5.9 | 6.0 | | V |
| | | $V_{CC}=4.5V, I_{OH}=4mA$ | 3.98 | 4.32 | | V |
| | | $V_{CC}=6.0V, I_{OH}=5.2mA$ | 5.48 | 5.81 | | V |
| Output Voltage Low-Level | V_{OL} | $V_{CC}=2.0V, I_{OL}=20\mu A$ | | 0 | 0.1 | V |
| | | $V_{CC}=4.5V, I_{OL}=20\mu A$ | | 0 | 0.1 | V |
| | | $V_{CC}=6.0V, I_{OL}=20\mu A$ | | 0 | 0.1 | V |
| | | $V_{CC}=4.5V, I_{OL}=4mA$ | | 0.15 | 0.26 | V |
| | | $V_{CC}=6.0V, I_{OL}=5.2mA$ | | 0.16 | 0.26 | V |
| Input Leakage Current | $I_{(LEAK)}$ | $V_{IN}=V_{CC}$ or GND, $V_{CC}=6.0V$ | | | ±0.1 | μA |
| Quiescent Supply Current | I_Q | $V_{IN}=V_{CC}$ or GND, $V_{CC}=6.0V, I_{OUT}=0$ | | | 8 | μA |
| Input Capacitance | C_{IN} | | | 3.5 | | pF |

■ DYNAMIC CHARACTERISTICS

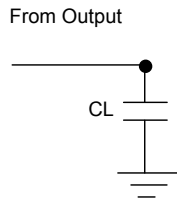
($T_A=25^\circ\text{C}$, $\text{GND}=0\text{V}$; $t_R=t_F=6\text{ns}$; $C_L=50\text{pF}$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------------------------------|-----------------------------|-----|-----|-----|------|
| Propagation Delay From CP to Qn | $t_{\text{PHL}}, t_{\text{PLH}}$ | $V_{\text{CC}}=2.0\text{V}$ | | 41 | 170 | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | | 15 | 34 | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | | 12 | 29 | ns |
| Propagation Delay From $\overline{\text{MR}}$ to Qn | t_{PHL} | $V_{\text{CC}}=2.0\text{V}$ | | 39 | 140 | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | | 14 | 28 | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | | 11 | 24 | ns |
| Output Transition Time | $t_{\text{THL}}, t_{\text{TLH}}$ | $V_{\text{CC}}=2.0\text{V}$ | | 19 | 75 | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | | 7 | 15 | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | | 6 | 13 | ns |
| Clock Pulse Width High or Low | t_w | $V_{\text{CC}}=2.0\text{V}$ | 80 | 14 | | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | 16 | 5 | | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | 14 | 4 | | ns |
| Master Reset Pulse Width Low | t_w | $V_{\text{CC}}=2.0\text{V}$ | 60 | 17 | | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | 12 | 6 | | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | 10 | 5 | | ns |
| Removal Time $\overline{\text{MR}}$ to CP | t_{rem} | $V_{\text{CC}}=2.0\text{V}$ | 60 | 17 | | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | 12 | 6 | | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | 10 | 5 | | ns |
| Setup Time DSA and DSB to CP | t_{SU} | $V_{\text{CC}}=2.0\text{V}$ | 60 | 8 | | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | 12 | 3 | | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | 10 | 2 | | ns |
| Hold Time DSA and DSB to CP | t_{H} | $V_{\text{CC}}=2.0\text{V}$ | +4 | -6 | | ns |
| | | $V_{\text{CC}}=4.5\text{V}$ | +4 | -2 | | ns |
| | | $V_{\text{CC}}=6.0\text{V}$ | +4 | -2 | | ns |
| Maximum clock pulse frequency | f_{MAX} | $V_{\text{CC}}=2.0\text{V}$ | 6 | 23 | | MHz |
| | | $V_{\text{CC}}=4.5\text{V}$ | 30 | 71 | | MHz |
| | | $V_{\text{CC}}=6.0\text{V}$ | 35 | 85 | | MHz |
| Clock Frequency | f_{CLOCK} | $V_{\text{CC}}=2.0\text{V}$ | | | 6 | MHz |
| | | $V_{\text{CC}}=4.5\text{V}$ | | | 31 | MHz |
| | | $V_{\text{CC}}=6.0\text{V}$ | | | 36 | MHz |

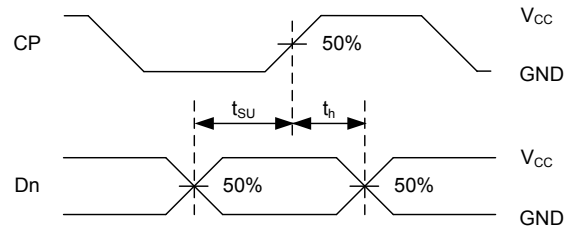
■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|-----------------|-----------------|-----|-----|-----|------|
| Power Dissipation Capacitance | C_{PD} | No load | | 40 | | pF |

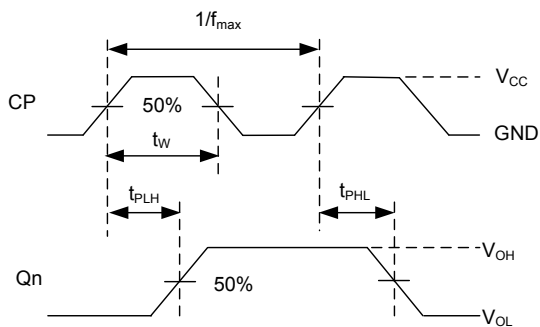
■ TEST CIRCUIT AND WAVEFORMS



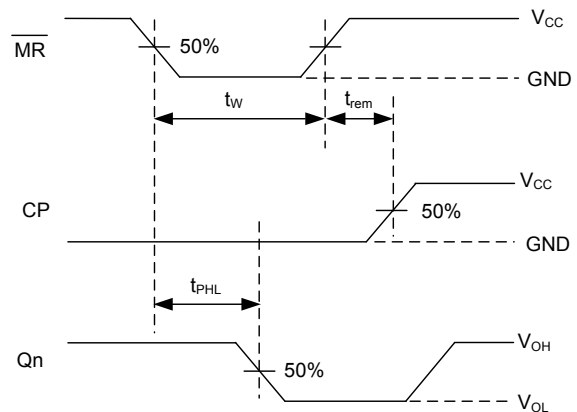
TEST CIRCUIT



SETUP TIME AND HOLD TIME



PROPAGATION DELAY TIMES FROM CP TO Qn



PROPAGATION DELAY TIMES FROM \overline{MR} TO Qn

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