



U74LVC3G17

CMOS IC

TRIPLE SCHMITT-TRIGGER BUFFER

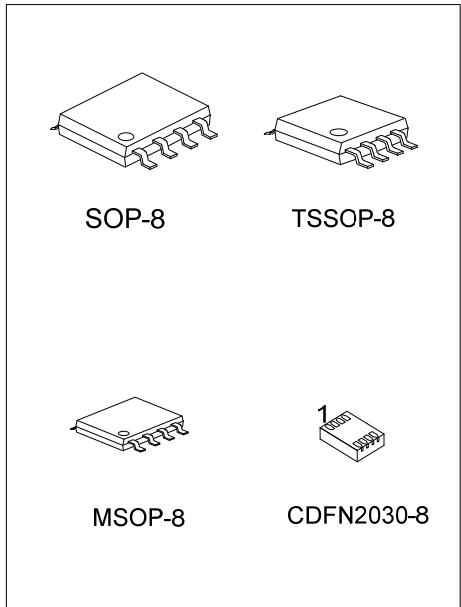
DESCRIPTION

The **U74LVC3G17** is designed as three independent buffers with Schmitt-trigger action. it may have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

This device has power-down protective circuit, preventing device destruction when it is powered down.

FEATURES

- * Wide supply voltage range from 1.65V to 5.5V
- * Inputs accept voltages up to 5.5V
- * I_{OFF} supports partial-power-down mode
- * Low static power consumption; I_{CC}=10μA (Max.)



ORDERING INFORMATION

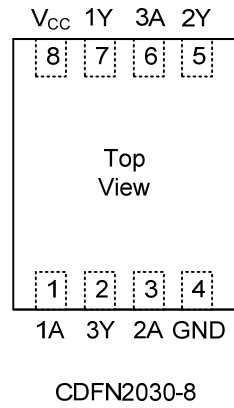
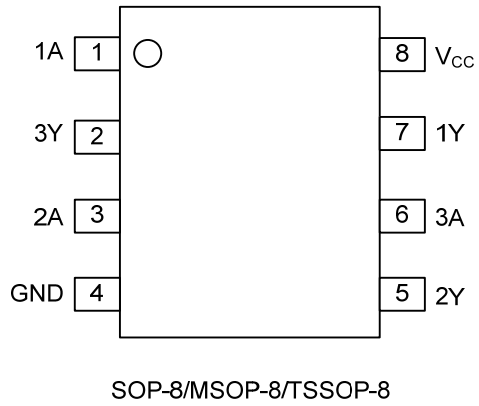
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC3G17L-S08-R	U74LVC3G17G-S08-R	SOP-8	Tape Reel
U74LVC3G17L-SM1-R	U74LVC3G17G-SM1-R	MSOP-8	Tape Reel
U74LVC3G17L-P08-R	U74LVC3G17G-P08-R	TSSOP-8	Tape Reel
U74LVC3G17L-CK08-2030-R	U74LVC3G17G-CK08-2030-R	CDFN2030-8	Tape Reel

<p>U74LVC3G17G-S08-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) S08: SOP-8, SM1: MSOP-8, P08: TSSOP-8 CK08-2030: CDFN2030-8 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING

SOP-8 / MSOP-8	TSSOP-8	CDFN2030-8
<p>8 7 6 5 → Date Code UTC □ □ □ □ L: Lead Free G: Halogen Free □ □ → Lot Code 1 2 3 4</p>	<p>8 → Date Code 1 2 3 4 • UTC □ □ □ □ L: Lead Free G: Halogen Free □ □ → Lot Code 5 6 7</p>	<p>LVC 3G17 • □ □ □ → Date Code</p>

■ PIN CONFIGURATION

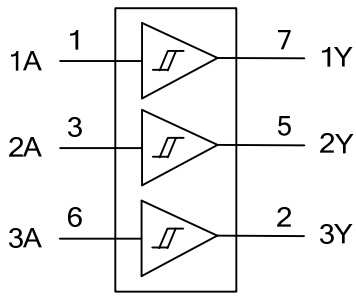


■ FUNCTION TABLE

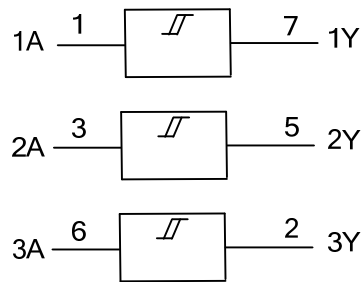
INPUT(A)	OUTPUT(Y)
L	L
H	H

Note: H: High voltage level; L: Low voltage level.

■ LOGIC DIAGRAM (positive logic)



Logic symbol



IEC logic symbol

■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ +6.5	V
Input Voltage	V _{IN}		-0.5 ~ +6.5	V
Output Voltage	V _{OUT}	Output in the high or low state	-0.5 ~ + V _{CC} +0.5	V
		Output in the power-off state	-0.5 ~ +6.5	V
Continuous V _{CC} or GND Current	I _{CC}		±100	mA
Continuous Output Current	I _{OUT}	V _{OUT} =0V ~ V _{CC}	±50	mA
Input Clamp Current	I _{IK}	V _{IN} <0V	-50	mA
Output Clamp Current	I _{OK}	V _{OUT} >V _{CC} or V _{OUT} <0V	-50	mA
Storage Temperature Range	T _{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		1.65		5.5	V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}	High or low state	0		V _{CC}	V
Operating Temperature (Note)	T _A		-40		+125	°C

Note: This condition is only determined from design. It can't be 100% tested in mass production.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V _{T+}	V _{CC} =1.65V	0.79		1.16	V
		V _{CC} =2.3V	1.11		1.56	V
		V _{CC} =3V	1.5		1.87	V
		V _{CC} =4.5V	2.16		2.74	V
		V _{CC} =5.5V	2.61		3.33	V
Negative-Going Input Threshold Voltage	V _{T-}	V _{CC} =1.65V	0.39		0.7	V
		V _{CC} =2.3V	0.58		1.1	V
		V _{CC} =3V	0.84		1.3	V
		V _{CC} =4.5V	1.41		2	V
		V _{CC} =5.5V	1.87		2.5	V
Hysteresis Voltage (V _{T+} -V _{T-})	ΔV _T	V _{CC} =1.65V	0.3		0.62	V
		V _{CC} =2.3V	0.4		0.77	V
		V _{CC} =3V	0.4		0.87	V
		V _{CC} =4.5V	0.6		1.04	V
		V _{CC} =5.5V	0.7		1.11	V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65 \sim 5.5V, I_{OH}=-100\mu A$	$V_{CC}-0.1$			V	
		$V_{CC}=1.65V, I_{OH}=-4mA$	1.2			V	
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.9			V	
		$V_{CC}=3V$	$I_{OH}=-16mA$	2.4			V
			$I_{OH}=-24mA$	2.3			V
		$V_{CC}=4.5V, I_{OH}=-32mA$	3.8			V	
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65 \sim 5.5V, I_{OL}=100\mu A$			0.1	V	
		$V_{CC}=1.65V, I_{OL}=4mA$			0.45	V	
		$V_{CC}=2.3V, I_{OL}=8mA$			0.3	V	
		$V_{CC}=3V$	$I_{OL}=16mA$			0.4	V
			$I_{OL}=24mA$			0.55	V
		$V_{CC}=4.5V, I_{OL}=32mA$			0.55	V	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0 \sim 5.5V, V_{IN}=5.5V$ or GND			± 5	μA	
Power OFF Leakage Current	I_{OFF}	$V_{CC}=0V, V_{IN}$ or $V_{OUT}=5.5V$			± 10	μA	
Quiescent Supply Current	I_{CC}	$V_{CC}=1.65 \sim 5.5V, V_{IN}=5.5V$ or GND, $I_{OUT}=0A$			10	μA	
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=3 \sim 5.5V$, One input at $V_{CC}-0.6V$, Other inputs at V_{CC} or GND			500	μA	
Input Capacitance	C_I	$V_{CC}=3.3V, V_{IN}=V_{CC}$ or GND		4		pF	

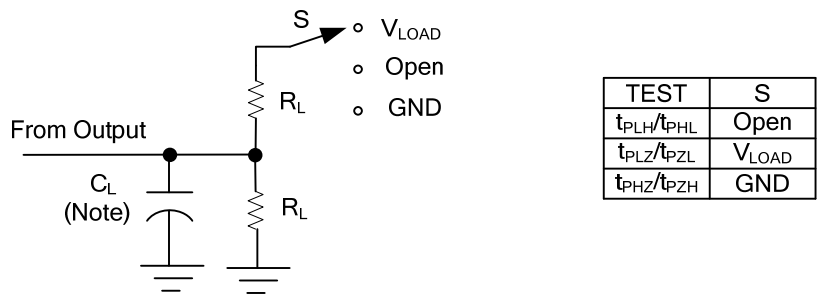
■ DYNAMIC CHARACTERISTICS ($T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From input (A) to output(Y)	t_{PD}	$V_{CC}=1.8\pm 0.15V, C_L=30pF, R_L=1k\Omega$	4.3		9.2	ns
		$V_{CC}=2.5\pm 0.2V, C_L=30pF, R_L=500\Omega$	2		6.2	ns
		$V_{CC}=3.3\pm 0.3V, C_L=50pF, R_L=500\Omega$	1.2		5.4	ns
		$V_{CC}=5\pm 0.5V, C_L=50pF, R_L=500\Omega$	1		4.1	ns

■ OPERATING CHARACTERISTICS ($f=10MHz, T_A=25^\circ C$, unless otherwise specified)

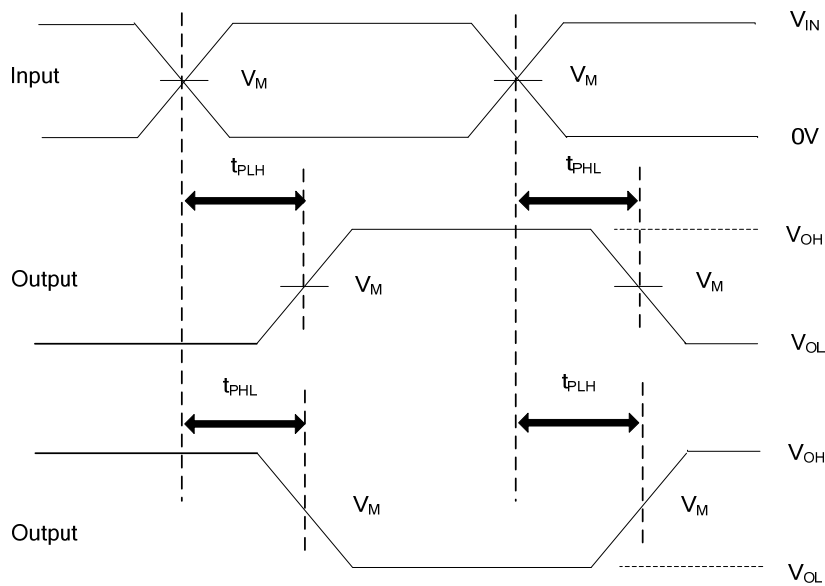
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=1.8V$		18		pF
		$V_{CC}=2.5V$		19		pF
		$V_{CC}=3.3V$		19		pF
		$V_{CC}=5V$		22		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance.

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_{IN}	t_r, t_f					
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	1M Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	1M Ω	0.15V
$3.3V \pm 0.3V$	3V	$\leq 2.5ns$	1.5V	6V	15pF	1M Ω	0.3V
$5V \pm 0.5V$	V_{CC}	$\leq 2.5ns$	$V_{CC}/2$	$2 \times V_{CC}$	15pF	1M Ω	0.3V



PROPAGATION DELAY TIMES

- Notes: 1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10MHz$, $Z_o = 50\Omega$.

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