



U74LV164

CMOS IC

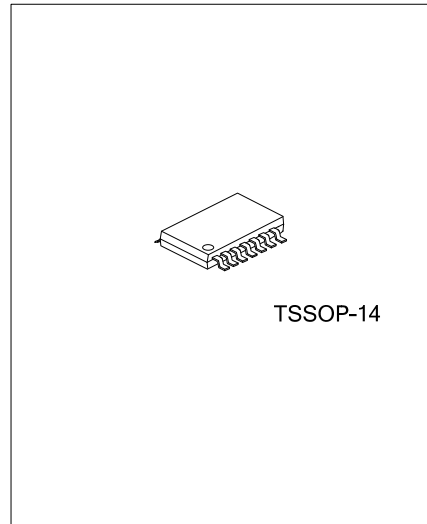
8-BIT SERIAL-IN/ PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The **U74LV164** is an 8-bit serial-in/parallel-out shift register. The logical AND of the A and B enters into Qn and shifts one place to right on each LOW-to-HIGH transition of the clock (CLK). A low level on the reset (\overline{CLR}) input clears all the register asynchronously and force all output LOW.

FEATURES

- * Wide supply voltage range from 2V to 5.5V
- * Inputs accept voltages up to 5.5V
- * Low static power consumption; $I_{CC}=20\mu A$ (Max.)
- * Optimized for 3.3V Operation
- * Support Mixed-Mode Voltage Operation on All Ports

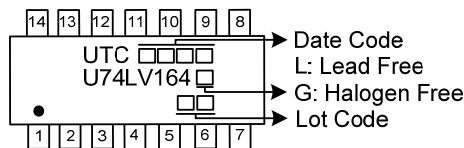


ORDERING INFORMATION

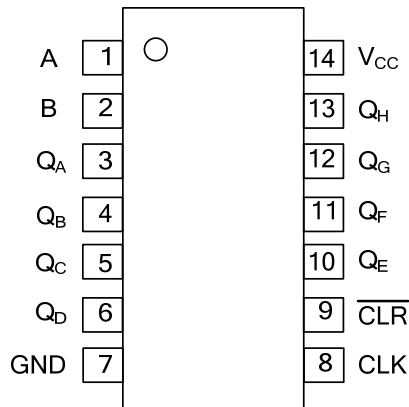
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LV164L-P14-R	U74LV164G-P14-R	TSSOP-14	Tape Reel

<p>U74LV164G-P14-R</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>	<p>(1) R: Tape Reel (2) P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free</p>
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MARKING



■ PIN CONFIGURATION

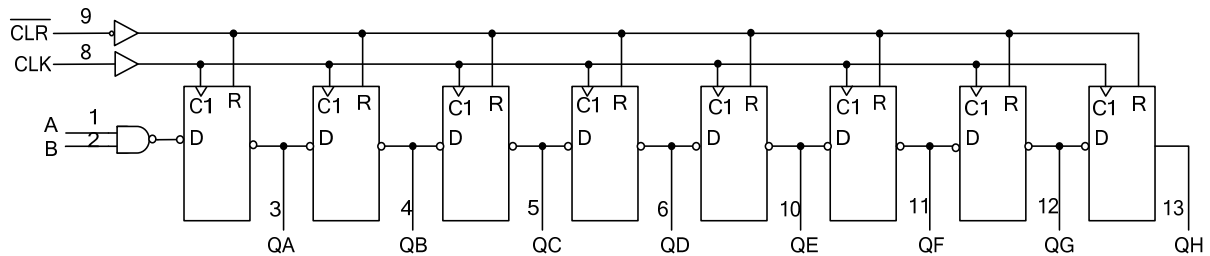


■ FUNCTION TABLE (each gate)

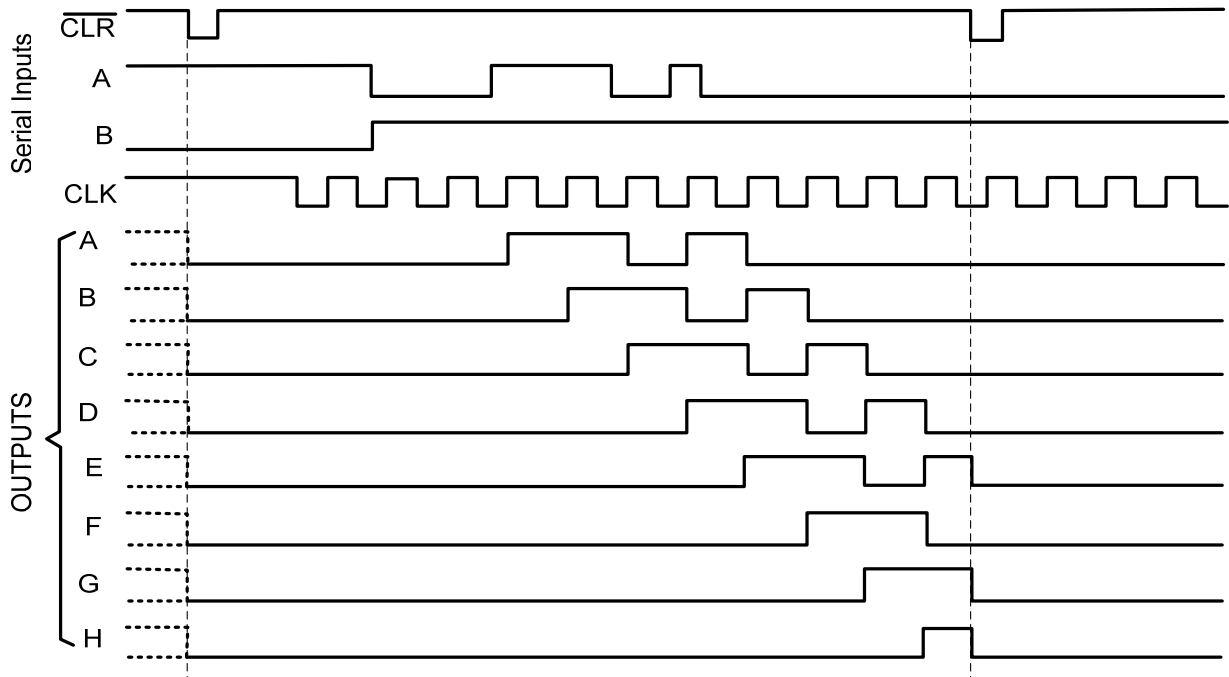
INPUTS				OUTPUTS		
$\overline{\text{CLR}}$	CLK	A	B	Q _A	Q _B	Q _H
L	X	X	X	L	L	L
H	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	↑	H	H	H	Q _{An}	Q _{Gn}
H	↑	L	X	L	Q _{An}	Q _{Gn}
H	↑	X	L	L	Q _{An}	Q _{Gn}

H = High voltage level ; L = Low voltage level ; X = Don't care

■ LOGIC DIAGRAM (positive gate)



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ +7.0	V
Input Voltage (Note 2)	V_{IN}		-0.5 ~ +7.0	V
Output Voltage	V_{OUT}		-0.5 ~ +7.0	V
Continuous Output Current	I_{OUT}	$V_{OUT}=0V \sim V_{CC}$	±25	mA
Input Clamp Current	I_{IK}	$V_{IN} < 0$ or $V_{IN} > V_{CC}$	±20	mA
Output Clamp Current	I_{OK}	$V_{OUT} < 0$ or $V_{OUT} > V_{CC}$	±50	mA
Continuous Current Through V_{CC} or GND	I_{CC}		±50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	$V_{CC}=2.5V\pm 0.2V$			200	ns/V
		$V_{CC}=3.3V\pm 0.3V$			100	ns/V
		$V_{CC}=5.0V\pm 0.5V$			20	ns/V
Operating Temperature	T_A		-40		+85	°C

■ ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High Level Input Voltage	V_{IH}	$V_{CC}=2V$	1.5			V
		$V_{CC}=2.5V\pm 0.2V$	$0.7\times V_{CC}$			V
		$V_{CC}=3.3V\pm 0.3V$	$0.7\times V_{CC}$			V
		$V_{CC}=5.0V\pm 0.5V$	$0.7\times V_{CC}$			V
Low Level Input Voltage	V_{IL}	$V_{CC}=2.0V$			0.5	V
		$V_{CC}=2.5V\pm 0.2V$			$0.3\times V_{CC}$	V
		$V_{CC}=3.3V\pm 0.3V$			$0.3\times V_{CC}$	V
		$V_{CC}=5.0V\pm 0.5V$			$0.3\times V_{CC}$	V
High-Level Output Voltage	V_{OH}	$V_{CC}=2V \sim 5.5V, I_{OH}=-50\mu A$	$V_{CC}-0.1$			V
		$V_{CC}=2.3V, I_{OH}=-2mA$	2			V
		$V_{CC}=3V, I_{OH}=-6mA$	2.48			V
		$V_{CC}=4.5V, I_{OH}=-12mA$	3.8			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=2V \sim 5.5V, I_{OL}=50\mu A$			0.1	V
		$V_{CC}=2.3V, I_{OL}=2mA$			0.4	V
		$V_{CC}=3V, I_{OL}=6mA$			0.44	V
		$V_{CC}=4.5V, I_{OL}=12mA$			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0\sim 5.5V, V_{IN}=V_{CC}$ or GND			±1	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0A$			20	μA
Additional Quiescent Supply Current Per Input Pin	ΔI_{CC}	$V_{CC}=5.5V$, One input at 0.6V, Other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_I	$V_{CC}=3.3V, V_{IN}=V_{CC}$ or GND		2.2		pF

■ TIMING REQUIREMENTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pulse duration CLK High or Low	t_w	$V_{CC}=2.5\pm0.2V$	6			ns
		$V_{CC}=3.3\pm0.3V$	5			ns
		$V_{CC}=5\pm0.5V$	5			ns
Pulse duration CLR Low	t_w	$V_{CC}=2.5\pm0.2V$	6.5			ns
		$V_{CC}=3.3\pm0.3V$	5			ns
		$V_{CC}=5\pm0.5V$	5			ns
Setup Time A and B to CLK \uparrow	t_{su}	$V_{CC}=2.5\pm0.2V$	6.5			ns
		$V_{CC}=3.3\pm0.3V$	5			ns
		$V_{CC}=5\pm0.5V$	4.5			ns
Setup Time CLR inactive	t_{su}	$V_{CC}=2.5\pm0.2V$	3			ns
		$V_{CC}=3.3\pm0.3V$	2.5			ns
		$V_{CC}=5\pm0.5V$	2.5			ns
Hold Time A and B to CLK \uparrow	t_h	$V_{CC}=2.5\pm0.2V$	-0.5			ns
		$V_{CC}=3.3\pm0.3V$	0			ns
		$V_{CC}=5\pm0.5V$	1			ns

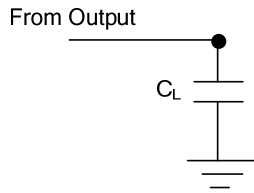
■ SWITCHING CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Maximum frequency	f_{MAX}	$C_L=15pF$, $R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$	55	105		ns
			$V_{CC}=3.3\pm0.3V$	80	155		ns
			$V_{CC}=5\pm0.5V$	125	220		ns
		$C_L=50pF$, $R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$	45	85		ns
			$V_{CC}=3.3\pm0.3V$	50	120		ns
			$V_{CC}=5\pm0.5V$	85	165		ns
Propagation delay from input (CLK) to output(Q)	t_{PD}	$C_L=15pF$, $R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		9.2	17.6	ns
			$V_{CC}=3.3\pm0.3V$		6.4	12.8	ns
			$V_{CC}=5\pm0.5V$		4.5	9	ns
		$C_L=50pF$, $R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		11.5	21.1	ns
			$V_{CC}=3.3\pm0.3V$		8.3	16.3	ns
			$V_{CC}=5\pm0.5V$		6	11	ns
Propagation delay from input (CLR) to output(Q)	t_{PHL}	$C_L=15pF$, $R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		8.6	16	ns
			$V_{CC}=3.3\pm0.3V$		6	12.8	ns
			$V_{CC}=5\pm0.5V$		4.2	8.6	ns
		$C_L=50pF$, $R_L=1M\Omega$	$V_{CC}=2.5\pm0.2V$		10.8	19.5	ns
			$V_{CC}=3.3\pm0.3V$		7.9	16.3	ns
			$V_{CC}=5\pm0.5V$		5.8	10.6	ns

■ OPERATING CHARACTERISTICS ($T_A = 25^\circ C$, unless otherwise specified)

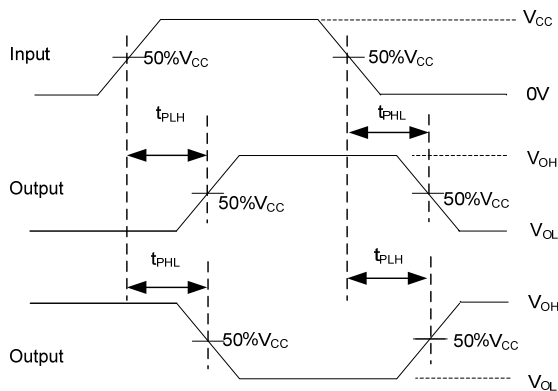
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{CC}=3.3V$, $f=10MHz$		48		pF

■ TEST CIRCUIT AND WAVEFORMS

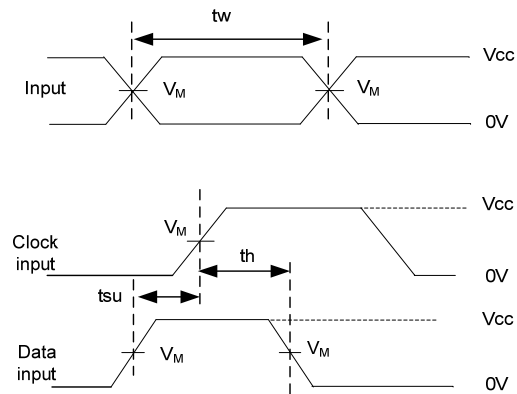


TEST CIRCUIT

Note : C_L includes probe and jig capacitance.



PROPAGATION DELAY TIMES



PROPAGATION DELAY FROM INPUT TO OUTPUT AND INPUT VOLTAGE WAVEFORMS.

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{MHz}$, $Z_O = 50\Omega$.

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