

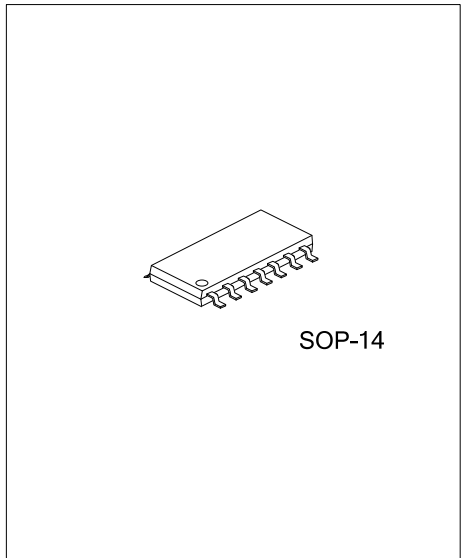


U74AHC132

Advance

CMOS IC

QUADRUPLE POSITIVE-NAND GATES WITH SCHMITT-TRIGGER INPUTS



SOP-14

DESCRIPTION

The **U74AHC132** is a device is a quadruple positive NAND gate designed for 2V to 5.5V V_{CC} operation. This device performs the Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A + B}$ in positive logic.

FEATURES

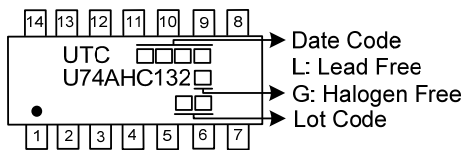
- * Operate from 2V to 5.5V
- * Operation form very slow input transitions
- * Temperature-Compensated threshold levels
- * Balanced propagation delays

ORDERING INFORMATION

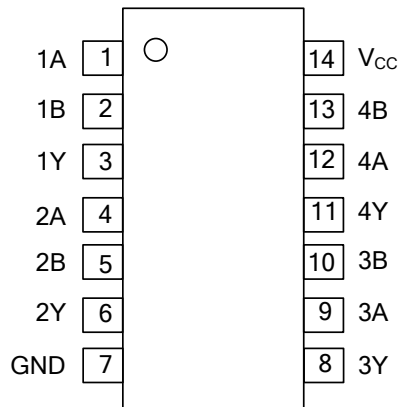
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHC132L-S14-R	U74AHC132G-S14-R	SOP-14	Tape Reel

<p>U74AHC132G-S14-R</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package 	<ul style="list-style-type: none"> (1) R: Tape Reel (2) S14: SOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ PIN CONFIGURATION

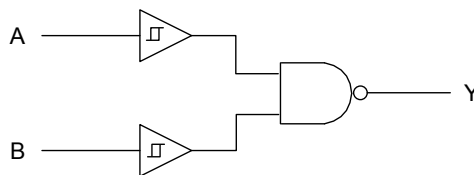


■ FUNCTION TABLE

INPUT(A)	INPUT(B)	OUTPUT(Y)
H	H	L
L	X	H
X	L	H

H = High voltage level ; L = Low voltage level ; X = Don't care

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V _{CC}		-0.5 ~ 7	V
Input Voltage	V _{IN}	V _{OUT} <0 or V _{OUT} >V _{CC}	-0.5 ~ 7	V
Output Voltage	V _{OUT}		-0.5 ~ V _{CC} +0.5	V
Continuous Current through V _{CC} or GND	I _{CC}		±50	mA
Input Clamp Current	I _{IK}	V _{IN} <0	-20	mA
Output Clamp Current	I _{OK}	V _{OUT} < 0 or V _{OUT} > V _{CC}	±20	mA
Continuous Output Current	I _{OUT}	V _{OUT} < 0 or V _{CC}	±25	mA
Storage Temperature	T _{STG}		-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}		2		5.5	V
Input Voltage	V _{IN}		0		5.5	V
Output Voltage	V _{OUT}		0		V _{CC}	V
Operating Temperature	T _A		-40		+125	°C

Note: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-Going Input Threshold Voltage	V _{T+}	V _{CC} =3.0V	1.2		2.2	V
		V _{CC} =4.5V	1.75		315	V
		V _{CC} =5.5V	2.15		3.85	V
Negative-Going Input Threshold Voltage	V _{T-}	V _{CC} =3.0V	0.9		1.9	V
		V _{CC} =4.5V	1.35		2.75	V
		V _{CC} =5.5V	1.65		3.35	V
Hysteresis (V _{T+} -V _{T-})	ΔV _T	V _{CC} =3.0V	0.3		1.2	V
		V _{CC} =4.5V	0.4		1.4	V
		V _{CC} =5.5V	0.5		1.6	V
High-Level Output Voltage	V _{OH}	V _{CC} =2V	I _{OH} =-50μA	1.9	2.0	V
		V _{CC} =3V		2.9	3.0	V
		V _{CC} =4.5V		4.4	4.5	V
		V _{CC} =3V, I _{OH} =-4mA	2.58		V	
		V _{CC} =4.5V, I _{OH} =-8mA	3.94		V	
Low-Level Output Voltage	V _{OL}	V _{CC} =2V	I _{OL} =50μA		0.1	V
		V _{CC} =3V			0.1	V
		V _{CC} =4.5V			0.1	V
		V _{CC} =3V, I _{OL} =4mA		0.36	V	
		V _{CC} =4.5V, I _{OL} =8mA		0.36	V	
Input Leakage Current	I _{I(LEAK)}	V _{CC} =0~5.5V, V _{IN} =5.5V or GND			±0.1	μA
Quiescent Supply Current	I _Q	V _{CC} =5.5V, V _{IN} =V _{CC} or GND, I _{OUT} =0A			2	μA
Input Capacitance	C _{IN}	V _{CC} =5.0V, V _{IN} =V _{CC} or GND		1.9	10	pF

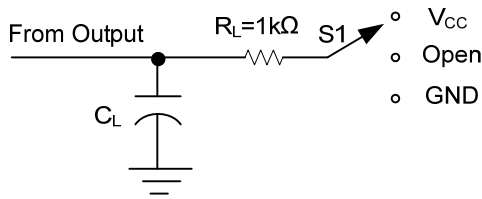
■ SWITCHING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A or B) to Output (Y)	t_{PLH} / t_{PHL}	$V_{CC}=3.3V\pm 0.3V$	$C_L=15\text{pF}$		5.6	11.9	ns
			$C_L=50\text{pF}$		8.8	15.4	ns
		$V_{CC}=5V\pm 0.5V$	$C_L=15\text{pF}$		3.9	7.7	ns
			$C_L=50\text{pF}$		5.2	9.7	ns

■ OPERATING CHARACTERISTICS ($T_A=25^\circ\text{C}$, unless otherwise specified)

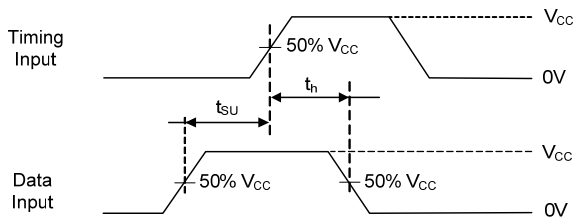
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance Per Flip-Flop	C_{PD}	$V_{CC}=5V$, $f=1\text{MHz}$, No load.		11		pF

■ TEST CIRCUIT AND WAVEFORMS

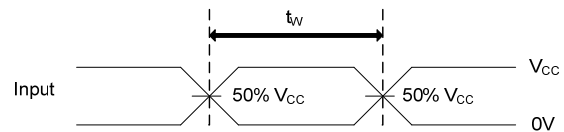


TEST CIRCUIT

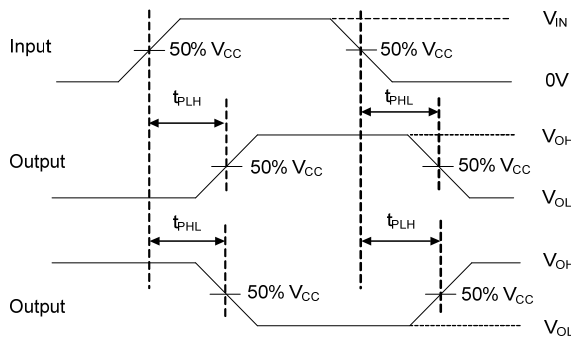
TEST	S1
t_{PLZ}/t_{PZL}	V_{CC}
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



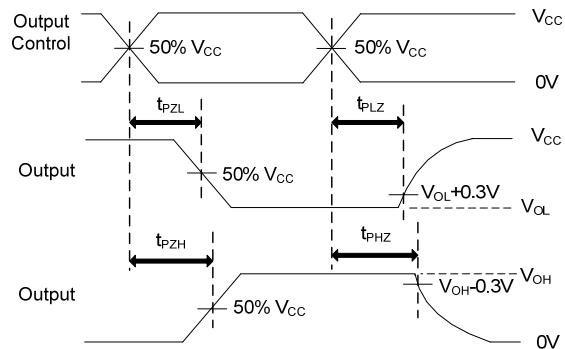
SETUP TIME AND HOLD TIME



PULSE WIDTH



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_o = 50\Omega$,

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